

A Digitally Calibrated 12 bits 25 MS/s Pipelined ADC with a 3 input multiplexer for CALICE Integrated Readout

F. Rarbi ^a, D. Dzahini ^a, L. Gallin-Martell ^a, J-Y Hostachy ^a,

^aIN2P3 – LPSC, 53 rue des Martyrs 38026 Grenoble, France

rarbi@lpsc.in2p3.fr

Abstract

The necessity of full integrated electronics readout for the next ILC ECAL presents many challenges for low power mixed signal design. The analog to digital converter is a critical stage for the system going from the very front-end stages to digital memories. We present here a high speed converter configuration designed to multiplex 3 analog channels through one analog to digital converter. It is a first step for a multiplexed 64 channel design. A CMOS 0.35 μ m process is used. The dynamic range is 2V over a 3.3V power supply, and the total power dissipation at 25 MHz is approximately 40mW. An analog power management is included to allow a fast switching into a standby mode that reduces the DC power dissipation by a ratio of three orders of magnitude (1/1000).

I. INTRODUCTION

For the next International Linear Collider (ILC), the front-end electronics for the electromagnetic calorimeter is really challenging. Mechanical constraints lead to the necessity to integrate in the same chip many different critical stages of the read-out electronics: charge preamplifiers, multi gain shapers, analog memories, ADC, and digital back-end. The average power consumption budget is limited to only 25 μ W per channel. This feature is reachable taking advantage of a power pulsing system with a 1/100 duty cycle, thanks to the beam timing of ILC. The design of the converter must deal with the power dissipation constraint which is one of the main concerns for the electronics. We present here a high speed converter configuration designed to multiplex many analog channels to one ADC as shown in figure 1.

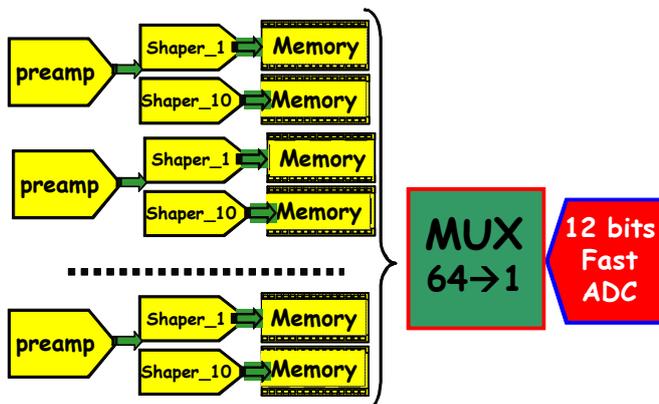


Figure 1: Overview of the front-end read out in the high speed configuration

The chip included a 12 bits ADC and a 3 to 1 analog multiplexer. This design makes the assumption that a high speed converter helps to minimize the total cross talk and the equivalent power dissipation related to each channel. A pipelined architecture is used. For high dynamic converters (more than 10 bit), and high speed (beyond 10 MHz), this architecture is usually considered as a good compromise between the power dissipation and the speed [1]-[4]. An overview block diagram is shown in figure 2.

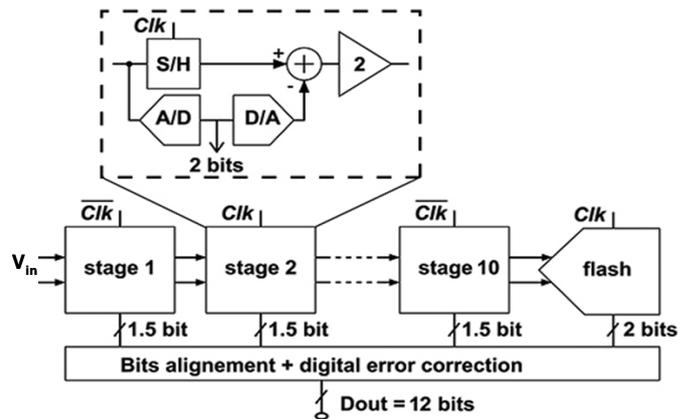


Figure 2: General block diagram of a pipelined converter

The ADC is composed of a set of pipelined stages. Each stage produces a digital estimate of an incoming held signal, then converts this estimate back to the analog, and subtracts the result from the held input. This residue is then amplified before being transferred to the next stage. Eventually the last stage is a full flash converter which determines the least significant bit (LSB). The successive digital results from the pipelined stages are appropriately delayed throughout a bit alignment network. Then a digital correction stage helps to recover the errors due to the offset of the comparators. Therefore, low offset comparators are not necessary and the total power consumption is reduced. The power dissipation is optimized for each stage following a power scaling in the successive pipeline stages.

This paper summarizes hereafter the design of two prototypes of the converter and we present some testing and simulation results. The first chip was implemented without any calibration nor trimming [5]. The second prototype is designed with a 3 to 1 analog multiplexer and includes an ADC with a dynamic element matching algorithm to improve the linearity.

II. THE PIPELINE ADC

A. The 1.5 bit stage

The converter consists of ten 1.5 bit sub-ADC followed by a 2 bit full flash stage (refer to figure 2). In figure 3 is illustrated a very simplified diagram of a 1.5 bit pipeline stage. The actual implementation in our design is differential. The A/D block consists of two non critical comparators. The D/A conversion, subtraction, amplification, and S/H functions are performed by a switched capacitor circuit with a resolution of 1.5 bit per stage and an amplification gain of 2. Hence the transfer function of this stage is: $V_s = 2 * V_{in} - \alpha * V_{ref}$.

α is set to 0 or 1 or -1, depending on the output codes (b0, b1); $\pm V_{ref}$ specifies the dynamic range.

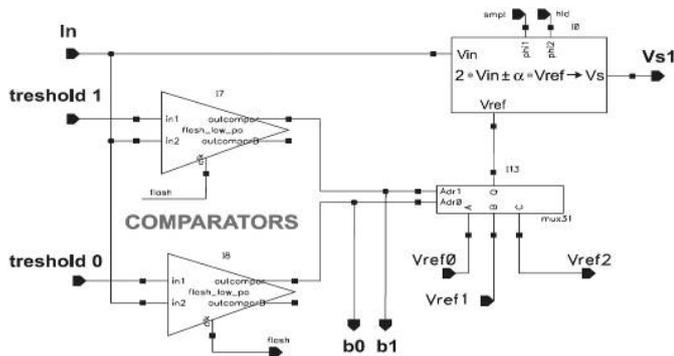


Figure 3: Bloc diagram of a 1.5 bit sub-converter stage.

The prototype has been tested successfully at 25 MHz with a power supply of 3.3 V. The total power consumption was only 37mW.

In figures 4 is shown the output codes for a 2 V peak-to-peak dynamic range with a 1 MHz sine wave input signal.

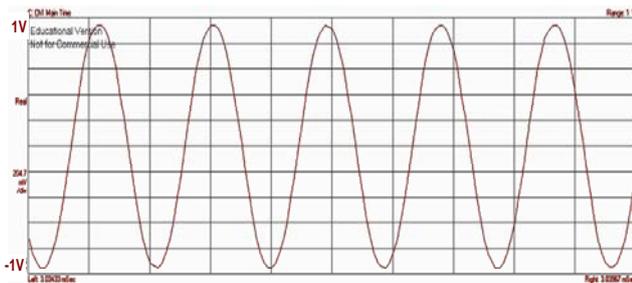


Figure 4: Output codes for an input 2V peak-to-peak sine wave

The Differential Non linearity (DNL) and the Integral Non Linearity (INL) are presented respectively in figure 5 and 6.

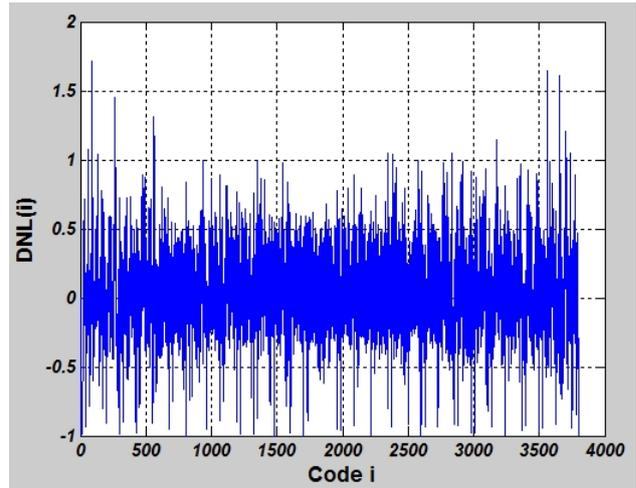


Figure 5: Linearity results (DNL)

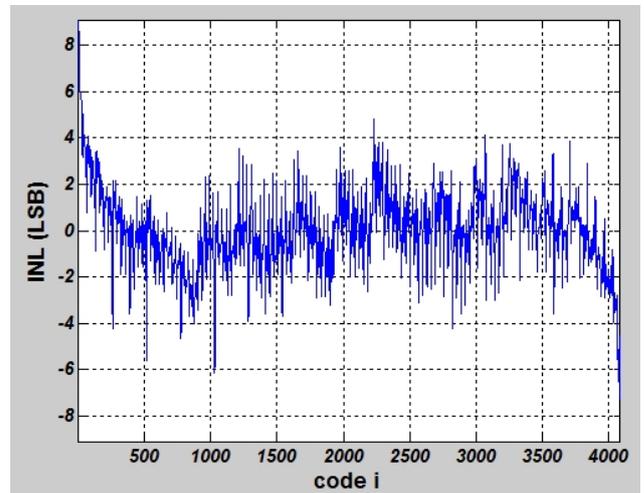


Figure 6: Linearity results (INL)

The DNL is almost ± 1 LSB, and the INL is ± 4 LSB.

This prototype deals with CALICE requirements and it is closed to the capacitors matching limits in this .35 μ m process. One solution to improve further the linearity and the total power consumption is to include a first multi-bit stage. Thus a second prototype was designed. This new version uses 2.5 bits in the first stage followed with seven 1.5 bit stages and a last 3 bits full flash. The architecture of this second prototype is illustrated in figure 7.

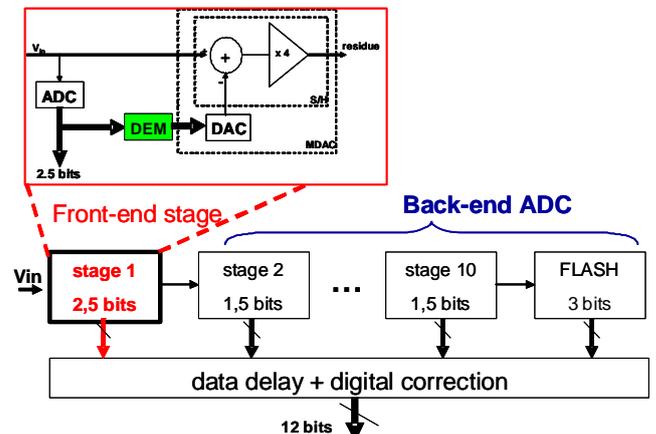


Figure 7: Block diagram of a pipelined converter with a multi-bit stage

B. The 2.5 bit stage

Increasing the number of bits in the front-end stage, relaxes the matching conditions necessary for the back-end; but it makes the amplifier more power consuming to deal with the gain bandwidth product requirements. The gain errors in this first stage are digitally controlled by means of a dynamic element matching (DEM) algorithm for a random choice of the DAC capacitor cells. This algorithm helps to minimize the integral non linearity.

In figure 7 is shown a simplified diagram of a 2.5 bit stage as a front end stage of the pipeline converter. The ADC block consists of six non critical comparators. The DAC conversion, subtraction, amplification, and S/H functions are performed by a switched capacitor structure as one can see in figure 8. This block is the multiplier-DAC (MDAC). It is composed of four capacitors.

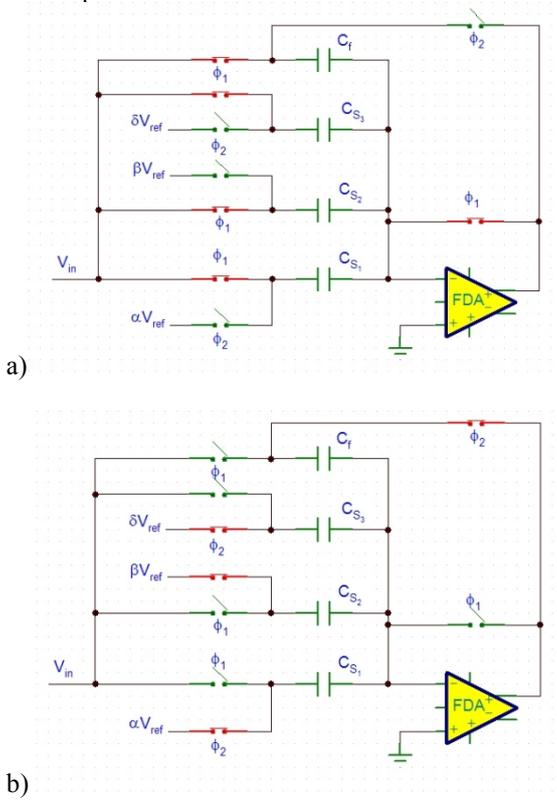


Figure 8: A 2.5 bits MDAC a) sampling phase; b) amplifying

The incoming signal is sampled during phase “Φ1” (figure 8 a). It is amplified by charge redistribution during phase “Φ2” (figure 8 b)). During this amplification phase, one plate of the sampling capacitors (C_{si}) is connected to a reference voltage V_{refi} which will be subtracted from the amplified signal. The residue resulting from this operation is transmitted to the next pipeline stage. The value selected for V_{refi} is respectively 0 or $(-V_{ref})$ or (V_{ref}) depending on the comparators outputs. The amplification gain is 4. Hence the transfer function of this stage is: $V_s = 4 * V_{in} - (\alpha + \beta + \gamma) * V_{ref}$ where α , β and γ are set to 0, -1 or 1, depending on the output codes of the sub-ADC. $\pm V_{ref}$ specifies the dynamic range. The transfer characteristic for a 2.5 bit stage is shown in figure 9.

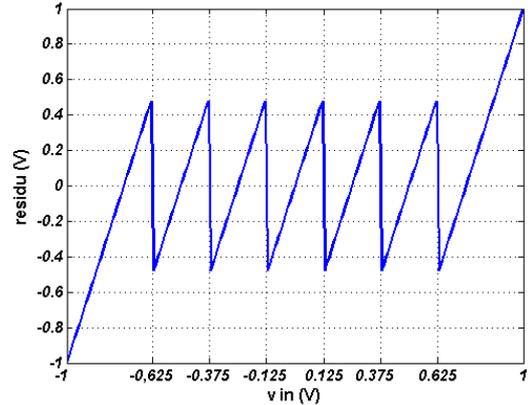


Figure 9: A 2.5 bit residue transfer curve

The expression “2.5 bit” is used to emphasize that only 7 combinations out of the 8 are acceptable for the output codes. The code (1, 1, 1) is avoided, thereby the amplifier will not saturate and this leaves room for the digital error correction.

The sub-ADC is composed of 6 low offset and low power dynamic comparators. The simplified schematic of the comparator is shown in figure 10.

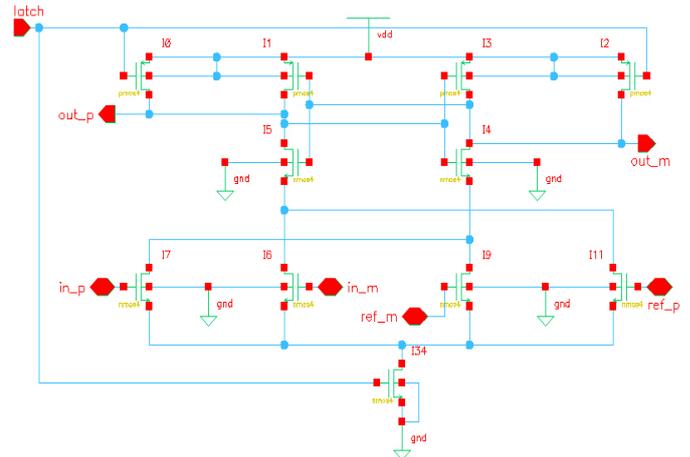


Figure 10: The dynamic comparator

The maximum offset of these comparators must be limited to $V_{ref}/8$, where $\pm V_{ref}$ is the full dynamic range. Our Monte Carlo simulation of the comparator’s offset is shown in figure 11 where one can notice a value less than $\pm 40mV$.

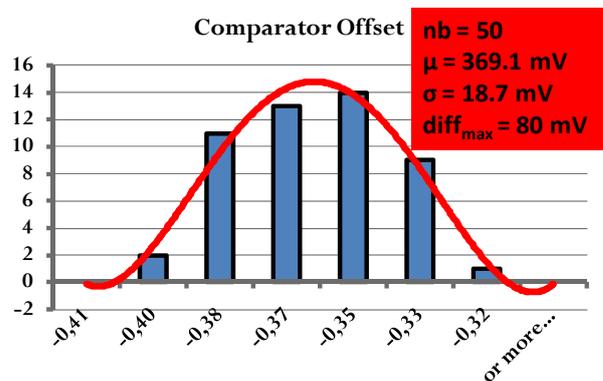


Figure 11: Offset of dynamic comparator (monte carlo simulation with 50 bins)

The output codes from the comparators are used thereafter by the DAC to rebuild the analog residue. A precise amplification by 4 is performed by four equivalent capacitors as shown in figure 8. The matching of C_f with all C_s is the main issue for this amplification, and it is the main cause of non-linearity for the converter.

To expect a 12 bit resolution feature, the amplifier (OTA) in the first stage must have a high open loop gain (more than 72 dB). The folded-cascode architecture used is shown in figure 12. Auxiliary amplifiers are added to increase the open loop gain [6], at just a little expense of power dissipation. The Bode diagram simulations results are given in figure 13.

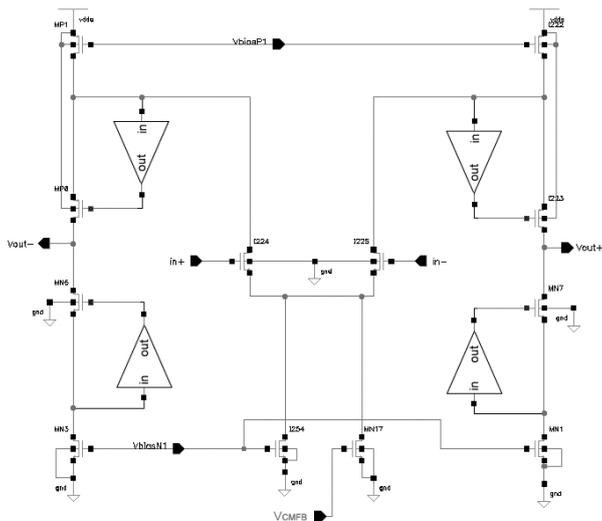


Figure 12: A regulated folded-cascode OTA

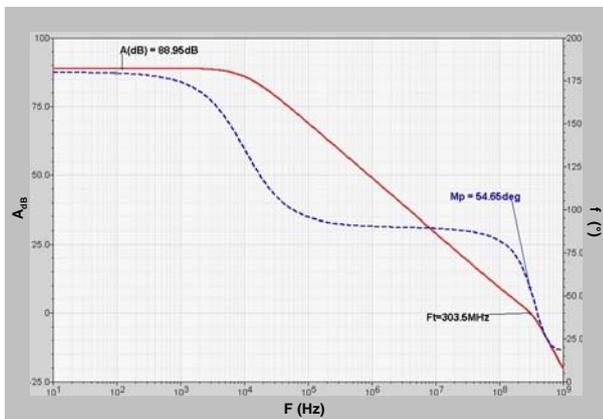
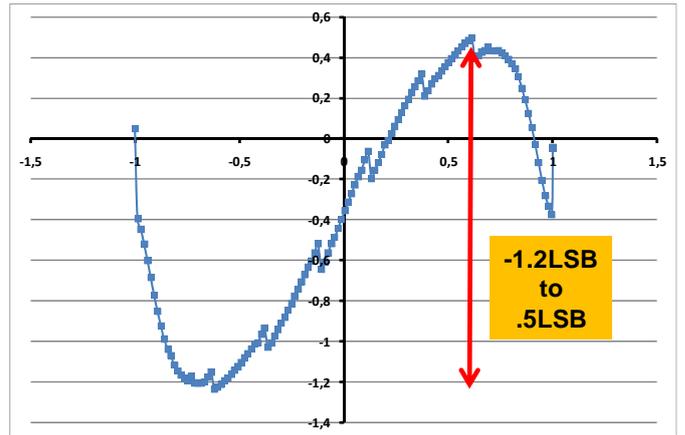


Figure 13: Bode diagram for the OTA on a 4pF load.

As we can see on the Bode diagram (figure 13), the cut off frequency at closed-loop gain of 4 (e.g: 12dB) is approximately 80MHz. Therefore a 25MHz sampling frequency is easily attainable.

The linearity simulations of our first Multiplier and DAC stage are given in Figure 14. One can notice a full range integral non linearity (INL) in the order of 1 LSB.



Multi-bit MDAC linearity (LSB@12bit)

Figure 14: Non linearity of the MDAC 2.5 bit.

C. Dynamic Element Matching (DEM)

Dynamic Element Matching permits to improve linearity of the ADC. In fact, it converts harmonic distortions into noise. The DEM block diagram is shown on figure 15.

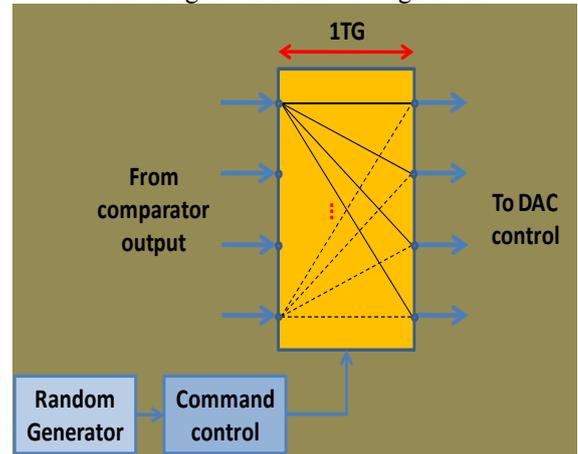


Figure 15: DEM Block diagram.

It consists of a random generator and a command control block which permit both to connect randomly one capacitor as a feedback capacitor on the OTA. The “yellow” block on figure 15 is used to make a link between output comparators to MDAC switches through only one transistor gate to be no sensitive to propagation time.

Matlab simulation results of the DEM principle are shown on figure 16. When DEM is “off” a) we have harmonic distortions which degrade linearity. On figure 16 b) DEM is “on”. We can notice that harmonic distortions are changed into noise. The noise floor are a little bit increased.

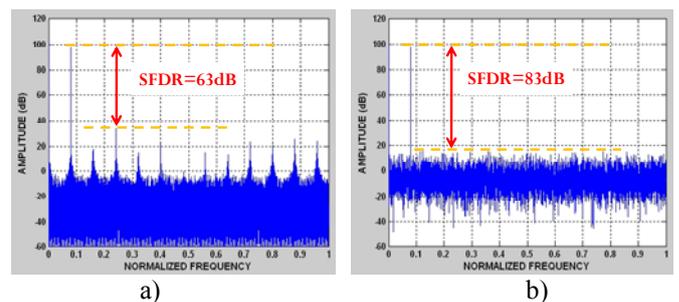


Figure 16: Matlab simulation results a) without DEM, b) with DEM

This design was submitted in a CMOS 0.35 μ process from Austria Micro System. The full layout photograph of the prototype is shown in figure 17. The prototype is composed of an analog multiplexer followed by a 12 bit pipeline ADC with a 2.5 bit first stage. The 3 channel analog multiplexer design and simulation results are presented in the next part.

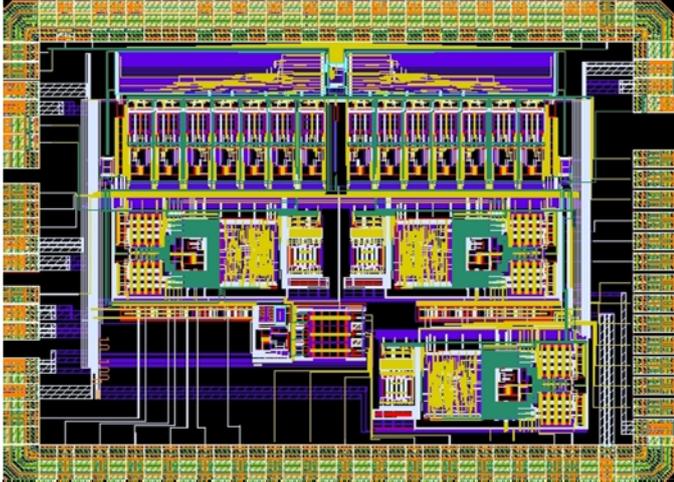


Figure 17: Layout photograph of the full prototype: analog multiplexer+ADC

III. THE 3 INPUTS ANALOG MULTIPLEXER

We present in this section the architecture and some simulation results of the 3 channel analog multiplexer.

A. Analog Multiplexer architecture

The analog multiplexer is designed to transfer successively the signal from the analog memories to the high speed ADC. A pseudo-differential and flip-flop architecture is used to overcome the capacitor's matching problem. A bloc diagram of the multiplexer is shown on figure 18.

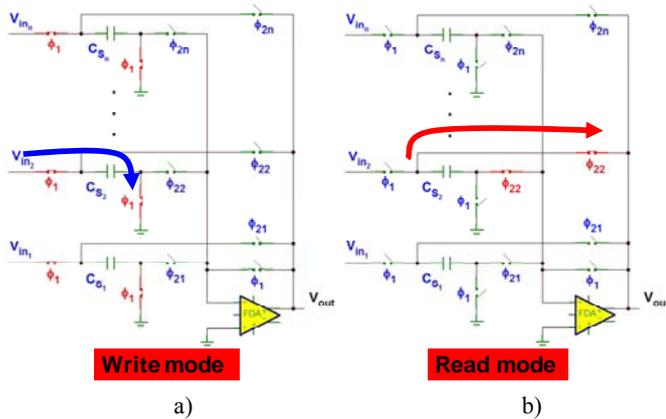


Figure 18: Analog multiplexer schematic in a) write mode, and b) read mode

During the write mode a), input signals are sampled through capacitors C_{si} . After that, each capacitor is connected sequentially as capacitor feedback on the amplifier. The same capacitor is used as sampled and read component: we have then no gain error in the analog multiplexer due to capacitor mismatch.

B. Simulation results

Two full range ramps with opposite slope are set on the external channels while a constant 2mV low signal is put in the middle.

The error found (213 μ V) is less than 1 LSB, and the impact on the low level signal is only 140 μ V.

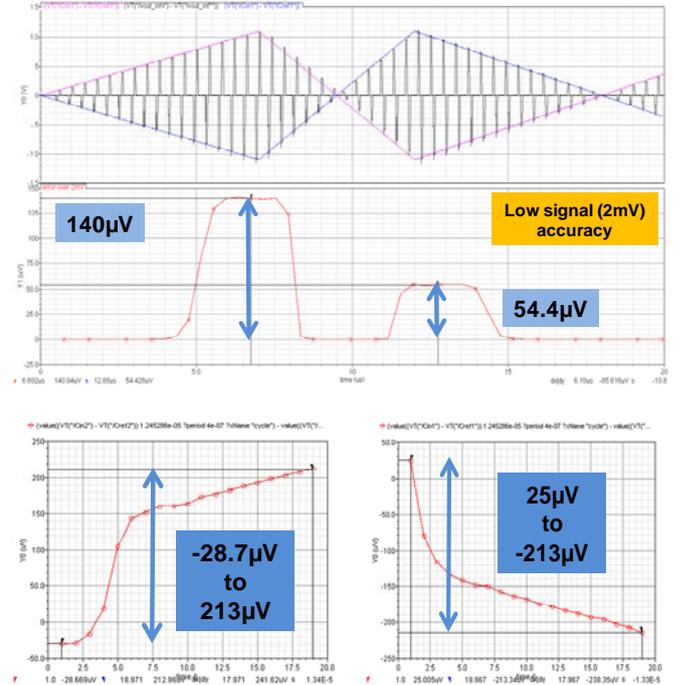


Figure 19: Multiplexer simulation results.

IV. AVERAGE POWER CONSUMPTION

We present in this section some simulation results about power consumption of this chip: the 3 inputs analog multiplexer followed by a 12-bit pipeline A/D converter using 2.5 bits in the first stage.

The total power consumption of the analog multiplexer is around 5.4mW according to our simulations up to 25MHz. This power consumption comes mainly from the amplifier. And the pipeline ADC has a power consumption about 40mW. It means the full chip: analog multiplexer and the ADC dissipates 45.4mW with a sampling frequency of 25MHz.

For the next ILC experiment, we choose to use only one fast ADC per chip. Each chip is composed of 64-channels and the depth of the analog memory will be sixteen. The ADC and multiplexer power consumption per chip is about 4 μ W by using power pulsing concept. This leads to an equivalent power consumption about only 125nW per channel. These results show a power consumption for both the multiplexer and the ADC of only 0.5% of the total power consumption which was estimated to 25 μ W per channel.

V. CONCLUSION

The design of two prototypes of a 12 bit 25MS/s pipelined ADC has been reported: the second one is used with a 3 three inputs analog multiplexer which will be extend to 64 in the

future. The first chip consumes very reasonable power dissipation: only 37mW. A 1.5 bit/stage architecture is used for the converter in a differential configuration. It has almost ± 1 LSB of DNL and ± 4 LSB of INL. This converter is a high speed version for the future International Linear Collider calorimeter detector (CALICE collaboration). The second version has been designed to improve linearity and power dissipation. A 2.5 bits first stage is used in this second chip. A 3 input analog multiplexer was also design to make the connection between 3 channels and the fast ADC. A very efficient fast power pulsing is integrated with this circuit to reduce the total DC power dissipation according to the beam low duty cycle.

REFERENCES

- [1] S. H. Lewis, et al., "10-b 20-Msample/s analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 27, pp.351-358, March 1992.
- [2] T. B. Cho and P. R. Gray, "A 10-bit, 20-MS/s, 35-mW pipeline A/D converter," in Proc. IEEE Custom Integrated Circuits Conf., May 1994, pp23.2.1-23.2.4 .
- [3] B.P. Brandt and J. Lutsky, "A 75-mW, 10-b, 20-MSPS CMOS subranging ADC with 9.5 effective bit at Nyquist" *IEEE Journal of Solid State Circuit* , pp.1788-1795 Dec. 1999.
- [4] Byung-Moo Min, et al "A 69-mW 10 bit 80 MS/s pipelined CMOS ADC" *IEEE Journal of Solid State Circuit* , Vol.38, N°12 Dec. 2003.
- [5] Ryu S.-I., Ray S., Song B.-S., Cho G.-H., Bacrania K. "A 14-b Linear Capacitor Self-Trimming Pipelined ADC", *IEEE J. Solid-State Circuits*, vol. 39, n°11, pp. 2046-2051, November 2004
- [6] Bult K., Govert J. G. M. G., "A Fast-Settling CMOS Op-Amp for SC Circuit with 90-dBDC Gain", *IEEE Journal of Solid State Circuit*, Vol.25, N°6, pp1379-1284, Dec. 1990.