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A Digitally Calibrated 12 bits 35 MS/s Pipelined ADC with a 32 input multiplexer for CALICE Integrated Readout

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The necessity of full integrated electronics readout for the next ILC ECAL presents many challenges for low power mixed signal design. The analog to digital converter is a critical stage for the system going from the very front-end stages to digital memories. We present here a high speed converter configuration designed to multiplex 32 analog channels through one analog to digital converter. A CMOS 0.35µm process is used. The dynamic range is 2V over a 3.3V power supply, and the total power dissipation at 30 MHz is approximately 50mW. An analog power management is included to allow a fast switching into a standby mode that reduces the DC power dissipation by a ratio of three orders of magnitude (1/1000).

Summary

For the next International Linear Collider (ILC), the front-end electronics for the electromagnetic calorimeter is really challenging. Mechanical constraints lead to the necessity to integrate in the same chip many different critical stages of the read-out electronics: charge preamplifiers, multi gain shapers, analog memories, ADC, and digital back-end. The average power consumption budget is limited to only 25µW per channel. This objective is reachable taking advantage of a power pulsing system with a 1/100 duty cycle, thanks to the beam timing of ILC. The design of the converter must deal with the power dissipation constraint which is one of the main concerns for the electronics. We present here a high speed converter configuration designed to multiplex many analog channels to one ADC. The chip is composed by an ADC and a 32 to 1 analog multiplexer. This design makes the assumption that a high speed converter helps to minimize the cross talk and the equivalent power dissipation related to each channel.

The ADC is composed by a set of pipelined stages. Each stage produces a digital estimate of an incoming held signal, then converts this estimate back to the analog, subtracts the result from the held input. This residue is then amplified before being transferred to the next stage. Eventually the last stage is a full flash that determines the least significant bit. The successive digital results from the pipelined stages are appropriately delayed throughout a bit alignment network. Then a digital correction stage helps to recover the errors due to the offset of the comparators. A dynamic comparator is sufficient and the total power consumption is reduced. In this new design, the ADC is composed by a first multi-bit stage followed by a set of 1.5 bit pipelined stages as back-end stage. Increasing the number of bits in the front-end stage, relaxes the matching conditions necessary for the back-end; but it makes the amplifier more power consuming to deal with the gain bandwidth product requirements. The gain errors in this first stage are digitally controlled by means of a butterfly dynamic element matching (DEM) algorithm for a random choice of the DAC capacitors cells. This algorithm helps to minimize the non linearity.

An analog multiplexer is also designed to link the analog channels to the high speed ADC. It uses a pseudo-differential and flip-flop architecture to overcome the capacitor's matching problem. The multiplexer has 12 bits accuracy and a crosstalk between several channels about less 1 LSB. The power consumption of one multiplexer is approximately 7mW according to our simulations up to 30 MHz.

The ADC and multiplexer power consumption per chip is about 4 µW by using power pulsing concept. This leads to an equivalent power consumption about only 125nW per channel. These results show a power consumption for both the multiplexer and the ADC of only 0.5% of the total power consumption which was estimated to 25µW per channel.

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