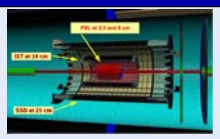
On-chip Phase-Locked Loop (PLL) design for clock multiplier in CMOS Monolithic Active Pixel Sensors (MAPS)

Q.Sun[1,2], K.Jaaskelainen[1], I.Valin[1], G.Claus[1], Ch.Hu-Guo[1], Y.Hu[1]

1 - Institut Pluridisciplinaire Hubert Curien, 23 rue du Loess, 67037 Strasbourg Cedex, France
2 - BeiHang University, Beijing, China

Isabelle.Valin@IReS.in2p3.fr

MAPS are foreseen to equip the vertex detector upgrade of STAR (Solenoidal Tracker at RHIC) experiment at RHIC (Relativistic Heavy Ion Collider). In order to achieve a vertex pointing resolution of about, or better than, 30 µm, two nearly cylindrical MAPS layers with average radii of about 2.5 cm and 8 cm will be inserted in the existing detector. These two layers will consist in 10 inner ladders and 30 outer ladders respectively. The sensor will be composed of a large area pixel array (reticle size) with column-level discriminator, a data sparsification circuit and a serial data transmission on the same substrate. The sensors readout path requires sending data over a 6-8 m LVDS link at a clock frequency of 160 MHz.
Inter sensors data skew and clock jitter have to be controlled precisely in order to ensure sensors synchronization. To reach these requirements, we have proposed to distribute a low frequency clock at 10 MHz which will be multiplied in each sensor by a PLL to 160 MHz. Using a low frequency input clock allows to reduce the problems of electromagnetic compatibility related to the integration density, high speed transmission and coupling with the environment.



STAR tracking upgrade

Ladder with 10 MAPS sensors (~ 2×2 cm each)

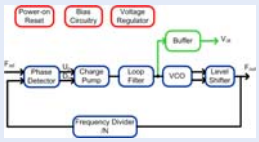
PLL Topology

Our first prototype of PLL was designed and manufactured in a 0.35 µm CMOS process. The PLL for clock multiplier in MAPS requirements are: low noise, low power consumption and small layout area.

Various noise sources within a PLL contribute to the jitter. In MAPS sensor, supply and substrate noise resulting of voltage fluctuations on the lines due to current transients in digital circuitry is a major noise source and should be minimized.

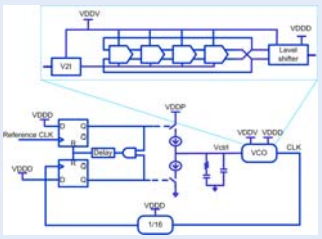
Thus, voltage regulators were implemented to provide stable supply voltages for the analog part.

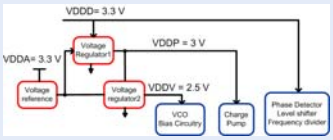
Thermal and shot noise can be minimized in this design. Design architecture less sensitive to supply and substrate noise has been chosen for the Voltage Controlled Oscillator.



Clock multiplier block diagram

Architecture of the PLL core





Power supplies distribution of PLL sub-blocks

Two linear regulators in series doubles the Power Supply Noise Rejection (PSNR)* of the second regulator (if they are identical).
The first regulator with low dropout voltage provides the supply voltage for the charge pump.
The second regulator with high PSNR performance generates the supply voltage for the VCO.

* The PSNR is defined as the ratio of ripple voltage on the output over ripple voltage on the input.

Building Blocks Description

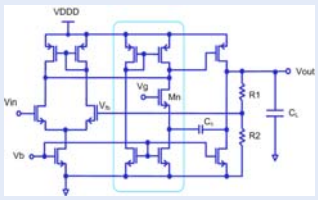
Voltage Regulator

In closed - loop configuration, the output ripple can be estimated by :

$$Vout_R \cong \frac{1}{\beta}\left(VREF_R + \frac{VDDD_R}{PSRR^*}\right)$$

where
β is the feedback factor, $VDDD_R$ and $VREF_R$ are the ripple voltages on the power supply and on the voltage reference respectively.

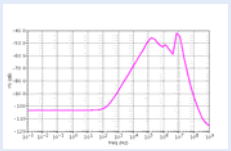
The regulator topology is similar to a two-stage amplifier. The architecture for the regulator uses a current buffer in series to the Miller compensation capacitor to break the forward path and compensate the zero. This compensation scheme is very efficient to improve high frequency PSNR. The disadvantages are a slight increase in complexity, noise and power dissipation.

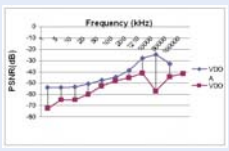


Voltage regulator schematic

Voltage regulator area	0.15 mm²
Static current consumption	780 µA
Maximum output current	14 mA
PSNR	< - 40 dB

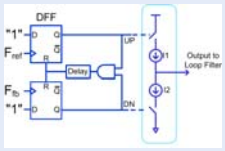
Simulated voltage regulator performance


Simulated PSNR of VCO supply voltage

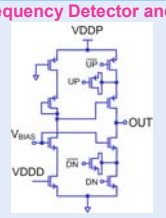


Measured PSNR for VCO and CP

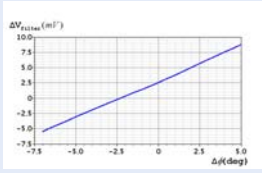
Phase-Frequency Detector and Charge Pump



Phase-fequency detector structure



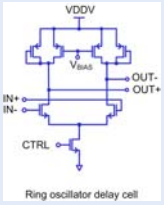
Charge pump schematic



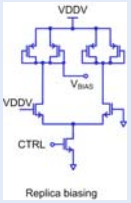
Simulation of Charge pump phase-detector

To avoid the dead-zone around the zero-phase error leading to increased noise, the state where UP and DN pulses are « high » simultaneously is enlarged by inserting a delay in the reset path.
Dummy switch structure in the charge pump compensates the charge injection and clock feedthrough mismatch.

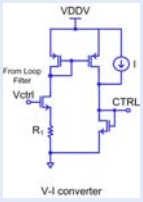
Voltage Controlled Oscillator



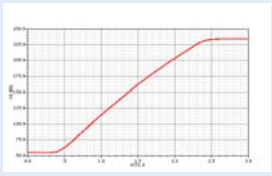
Ring oscillator delay cell



Replica biasing



V-I converter


Simulated VCO tuning range
Freq. (MHz) versus Control Voltage (V)

The VCO topology is a 4 stage differental ring oscillator. The delay cell contains a source coupled pair with symmetric resistive loads. Linear controllable resistors loads are desirable to achieve supply noise rejection in differential structure. By using symmetric loads, the first order noise coupling term are cancelled out, reducing the jitter caused by the common-mode noise present in the supply line. A controllable tail current in the delay cell and in the bias circuit is used to adjust the cell delay. The voltage to current converter provides a first-order linear relationship between the oscillation frequency and the control voltage.

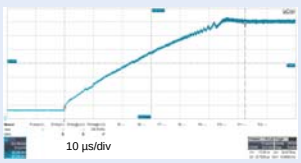
PLL Measurements


Clock multiplier photography

Temperature	Lower limit	Upper limit
0°C	130 MHz	295 MHz
20°C	138 MHz	298 MHz
45°C	140 MHz	297 MHz

PLL locking range as function of the temperature

The frequency shifts of about 80 MHz upwards compared with the simulation results. It may result from the overestimation of parasitic capacitances in the VCO.



PLL locking time (the reference clock jumps from 10 MHz to 16.7 MHz)

Reference freq.(MHz)	9	10	12	14	16	18
PLL clock (MHz)	144	160	192	224	256	288
Period jitter (ps rms)	12.8	13.5	11.6	13.2	11.7	12.2
Period jitter peak to peak (ps)	124	126	113	107	97	111
Cycle to cycle jitter (ps rms)	22.7	22.0	23.1	20.6	21.5	21.5
Cycle to cycle jitter peak to peak at 10^{-12} BER (ps)	323	317	326	293	318	307

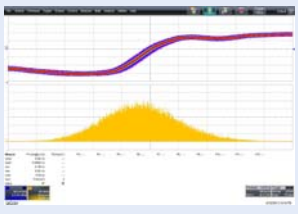
Jitter measurement at 3.3V supply voltage

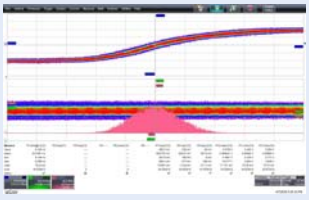
Noise frequency	0.1 kHz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
Period jitter (ps rms)	18.8	18.5	16.2	15.5	15.6	15.3
Period jitter peak to peak (ps)	148	131	140	113	132	127

Measured period jitter with a peak amplitude of 400 mV, square wave on the power supply at 160 MHz nominal frequency

The measured period jitter is 13.5 ps rms with a quiet supply voltage and 16.2 ps rms with noise source on the supply voltage for the 160 MHz output clock.

The regulators area represents about 35% of the PLL area and the power consumption increases of 20%.


Measured period jitter at 3.3 V supply voltage


Measured period jitter with a peak amplitude of 400 mV, 10 kHz square wave on the power supply

PLL performance summary

Technology	0.35 µm CMOS process
PLL die area	0.42 mm²
Multiplication factor	16
Locking range	138 MHz – 298 MHz
Power supply requirement	3.0 – 3.6 V
Power consumption (estimated)	7 mW at 160 MHz
Period jitter	13.5 ps rms
Period jitter with noise*	16.2 ps rms
Locking time	60 µs

* Noise : peak amplitude of 400 mV, 10 kHz square wave on power supply, at room temperature

Conclusion and Perspectives

The measured period jitter is lower than 20 ps rms in a noisy power supply environment. With this performance, the PLL can be used as clock multiplier in MAPS.

In future development, the PLL clock will also equip a serial transmitter block. The values of jitter will be optimized to ensure the acceptable data error rate by characterizing the transmission system with cable connections and receivers .
We plan to design a new prototype to enhance jitter performance by using a programmable loop bandwidth and by optimizing the VCO.