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On-chip Phase Locked Loop (PLL) design for clock multiplier in CMOS Monolithic Active Pixel Sensors (MAPS)

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In a detector system, clock distribution to sensors must be controlled at a level allowing proper sensors synchronisation. In order to reach theses requirements for the HFT (Heavy Flavor Tracker) upgrade at STAR (Solenoidal Tracker at RHIC), it has been proposed to distribute a low frequency clock at 10 MHz which will be multiplied in each sensor by a PLL to 160 MHz. A PLL was designed for low period jitter less than 20 ps rms and low power consumption of 7mW. This paper presents the architecture and the measurement results of the PLL fabricated in a 0.35µm CMOS process.

Summary

CMOS MAPS are foreseen to equip the HFT of the vertex detector upgrade of STAR experiment at RHIC (Relavistic Heavy Ion Collider). In order to achieve a vertex pointing resolution of about, or better than, 30 µm, two nearly cylindrical MAPS layers with average radii of about 2.5 cm and 8 cm will be inserted in the existing detector. These two layers will consist in 10 inner ladders and 30 outer ladders respectively. Every ladder contains 10 sensors of 2 cm x 2 cm each.

The sensor for the HFT final upgrade at STAR named Ultimate will integrate on the same substrate a large area pixel array with column-level discriminator, data sparsification circuit and serial data transmission. The sensors readout path to be used in the HFT upgrade requires sending data over a 6-8 meters LVDS link at a clock rate of 160 MHz. Inter sensors data skew and clock jitter have to be controlled precisely in order to ensure sensors synchronization.

A PLL clock multiplier, which allows generating the 160 MHz clock frequency from a relatively low frequency input clock at 10 MHz, will be implemented on each sensor. Using a low frequency input clock allow to reduce the problems of electromagnetic compatibility (EMC) related to the integration density, high speed transmission and coupling with the environment. The same PLL will also equip an optional 8B/10B data transmission block implemented in Ultimate.

The choice of the 10 MHz input clock results of a compromise between the jitter requirement and the complexity for developing a frequency multiplier. The input clock will be multiplied by 16 on chip.

A first prototype of charge-pump PLL circuit was designed and fabricated in a 0.35µm CMOS process. In order to reduce the PLL jitter coming from supply noise, on-chip voltage regulator is implemented to provide two stable power supplies to the VCO (Voltage controlled oscillator) and the Charge-pump blocks. This technique allows reducing the PLL jitter as long as the voltage regulator has a very good PSNR performance.

The preliminary results show that a period jitter of 13.6 ps rms was measured for the 160 MHz output. The period jitter increases slightly at 16.2 ps rms when the power supply is modulated with 400 mV, 10 kHz square wave. The power dissipation of the PLL including voltage regulator is estimated to 7 mW at 160 MHz.

The contribution to the workshop includes the PLL overview with a focus on the measurement results and future developments.

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