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# Charge Pump Clock Generation PLL for the Data Output Blocks of the Upgraded ATLAS Front-End in 130nm CMOS

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FE-I4 is the 130nm ATLAS pixel IC currently under development for upgraded LHC luminosities. FE-I4 is based on a low-power analog pixel array and digital architecture concepts tuned for higher hit rates. An integrated PLL has been developed that locally generates a clock signal for the 160 Mbit/s output data stream from the 40MHz bunch crossing reference. This block is designed for low-power, low-area and handles high radiation levels. After a general FE-I4 introduction, the presentation will focus on FE-I4 output blocks and a first prototype submitted early 2009.

## Summary

A new ATLAS Front-End chip, FE-I4, is being developed in a 130 nm standard CMOS technology for use for upgraded LHC luminosities, both for the Insertable B-Layer upgrade project and the outer layers of Super-LHC. FE-I4 is based on a low-power analog pixel array and new digital architecture concepts. A general overview on the FE-I4 architecture will be presented with focus on the challenges of the output stages.

In order to handle the expected hit rate, the front-end will stream data out at 160 Mbit/s. A type-II phase-locked loop (PLL) consisting of a phase frequency detector, a charge pump, a loop filter (LF), a voltage-controlled oscillator (VCO), frequency dividers and buffers has been developed to generate the necessary clock signal with a well-defined duty cycle from the available 40 MHz bunch crossing reference clock of the detector.

The PLL core is designed with a low power budget of 3.9 mW and small die area consumption of 255 um by 225 um. The VCO of the PLL is based on a three-stage differential ring oscillator working at a nominal frequency of 640 MHz. The design trade-offs involved with the choice of a ring oscillator in terms of area, noise and locking range are elaborated. Choosing an oscillation frequency higher than the output frequency for the VCO guarantees a lower area consumption of the LF capacitors and a well-defined duty cycle handling at the expense of slightly increased power consumption for the VCO and the four-stage dividing chain. Throughout the design, triple-well NFETs are used in all analog blocks for good isolation of the active devices from substrate noise.

In the ATLAS experiment, the PLL will be placed in a hostile radiation environment. In case of single-event transients due to severe charge injections, a short settling time to recover from a loss of lock is important. The presented PLL recovers from any given upset in less than 3 us.

A stand-alone PLL test chip that has been submitted for fabrication early in 2009 will offer output clocks of both 80 MHz for double data rate transfer and 160 MHz for conventional single-edge data stream out at 160 Mbit/s. The differential clock output lines are driven by integrated LVDS drivers. This test chip is scheduled for intense performance measurements and irradiation tests. For these irradiation tests, the PLL is equipped with an on-chip loss-of-lock detection circuit. Furthermore, the demonstrator includes a built-in test structure for 160 Mbit/s double data rate output streaming, consisting of an 8 bit pseudo random binary sequence generator, an 8 bit to 10 bit coder and a serializer.

In September 2009 simulation results will be backed-up by first measurement results on the demonstrator.

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