A 12 µm pitch CMOS Pixel Sensor Designed in the 3DIT for the ILC Vertex Detector

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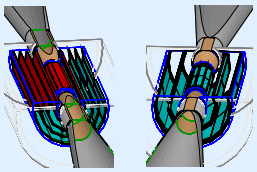
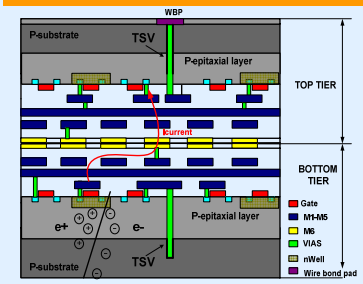
Introduction

CMOS MAPS are foreseen for several applications, ranging from subatomic physics experiments to bio-medical imaging devices. They provide an attractive trade-off between granularity, material budget, read-out speed, radiation tolerance and power consumption. The vertex detector upgrade of the STAR (Solenoidal Tracker at RHIC) experiment and the EUDET beam telescope, an EU R&D program, are the first places where MAPS will be operated in real experimental conditions. Recently, excellent tracking performances with fast read-out speed have been experimentally verified in beam tests. However, the innermost layer of the ILC vertex detector requires pixel sensors with a high single point resolution of 2~3 µm associated to a very demanding read-out speed of a few microseconds per frame only. This makes the design of 2D CMOS MAPS particularly tedious. Based on vertical interconnects between IC tiers, 3D Integrated Technologies allow combining in a single chip several thinned and bonded silicon microcircuits. They provide better electrical performance, low power consumption, highly miniaturised functionalities, improved form factor and lower fabrication cost. They are particularly suited to CMOS MAPS since they integrate different CMOS manufacturing processes, each optimised for a given sequence of the charge generation and signal processing chain.



ILD design: 2 options for the ILC vertex

3D Integrated Technology and Physics Consideration for ILC



The working principle of the 3D MAPS

Vertical integration (3D) technologies :

- Face to face bonding (metal 6)
- Cu-Cu thermo-compression bond
- Via first approach
- Multiple strata of planar devices are stacked and interconnected using through silicon vias (TSV)

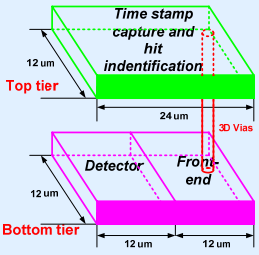
The 3D MAPS is based on the same working principle as standard MAPS, the charge generated by the impinging particle is collected by the n-well/p-epi diode, created by the floating n-well implantation reaching the epitaxial layer. The charge collection is chiefly thermal diffusion driven. As compared to the standard 2D MAPS, each pixel of 3D MAPS may be connected directly to a complex readout chain distributed over the different tiers.

Physics consideration:

1. **From Physics simulations, it shows that 15 hits /cm² /BX should be considered, in the innermost layer, due to the beamstrahlung background.**
2. **Due to thermal diffusion, the signal charges will be shared among neighbouring pixels, named a cluster, in the epitaxial layer. The number of pixels per cluster passing the threshold can safely be estimated to 6 in a standard CMOS technology with low resistivity epitaxial.**

Try to choose a 12µm pitch pixel, motivated by:

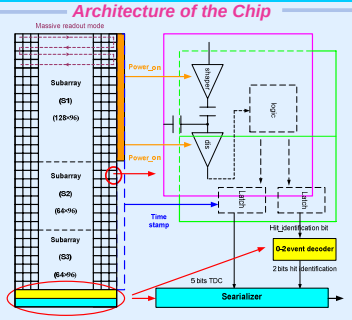
- **The probability of a single cell being hit twice in a bunch train is about 5.25 % for 12 µm pitch pixels. Moreover, it is negligible to have a pixel firing three times per train for 12 µm pitch pixels because the probability is around 0.62 %.Therefore an overflow bit displaying whether the pixel has been fired a second time or not should be sufficient.**
- **Single point resolution < 3 µm with binary output**



The unit of the pixel cell

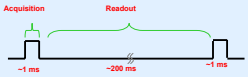
Circuits and System

Architecture of the Chip



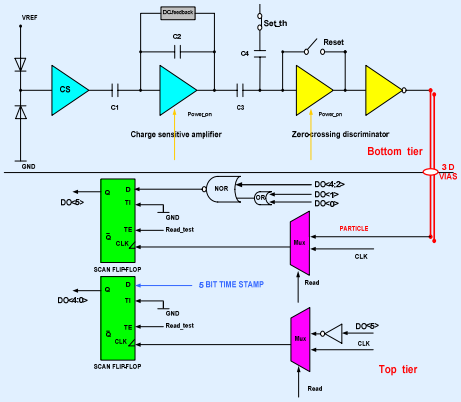
The architecture of the chip

- 256 x 96 pixels with a 12µm pitch pixel
- 0-2 event decoder
- Time stamp generator
- PLL and 8b-10b serializer
- Bias generator in each row

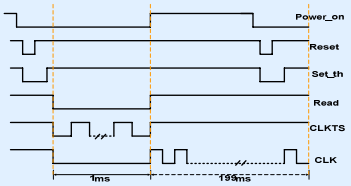


ILC bunch structure

1. A 5-bits TDC includes the time stamp generator and time stamp capture circuit, which converts the arrival time information of the first hit into its equivalent digital representation in the digital cell. The detection of potential second hit is shown by the overflow bit. The time resolution is generated by a 5-bits time stamp generator on the perimeter with clock period of 30 µs.
2. During the data acquisition, a corresponding output code in each cell is readout on the same 6-bits bus to 0-2 event decoder by the CLK at 200 KHz. The massive readout is performed row by row and one by one. And then the data sends into the 8b-10b transmitter to generate the serial signal.

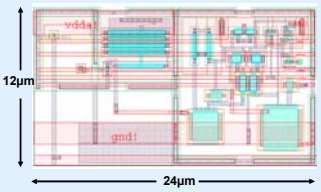


The schematic of each pixel cell

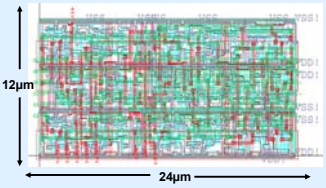


Timing programme

Pixel Cell



The pixel cell layout of bottom tier



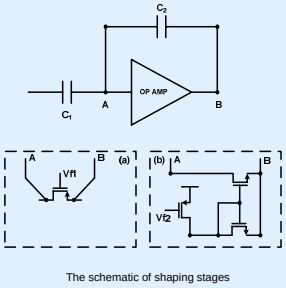
The pixel cell layout of top tier

- Tier-1: A: sensing diode & amplifier, B: shaper & discriminator
- Tier-2: time stamp (5 bits) + overflow bit & delayed readout

The innermost layer of the ILC vertex detector needs 7-bits time stamp accuracy during each train (1ms). However due to the constraint of the chosen technology (0.13µm) only 5-bits time stamp associated with a second hit flag is implemented in a 12µm x 24µm pitch cell. Therefore, the detector and front-end circuits are also placed together in the same size on the top tier.

Simulation Results and Conclusion

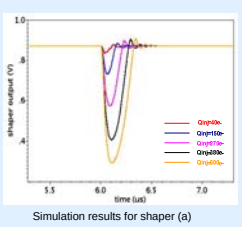
Shaper stages



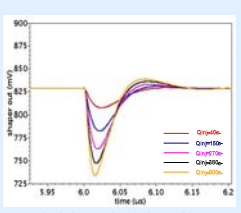
The schematic of shaping stages

Front-end circuits performances summary

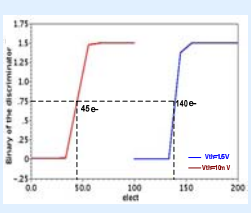
Technology	0.13µm CMOS process
Static power consumption	7.5 µW
Charge sensitivity	800mV/fC
ENC	15 e-
The area of the layout	12 µm x 12 µm
Ajustable threshold voltage	10 mV~1.5 V



Simulation results for shaper (a)

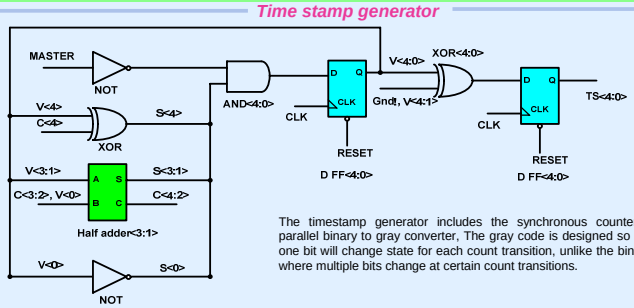


Simulation results for shaper (b)



Tran response of front-end circuits at the different threshold voltage

Time stamp generator



The timestamp generator includes the synchronous counter and a parallel binary to gray converter, The gray code is designed so that only one bit will change state for each count transition, unlike the binary code where multiple bits change at certain count transitions.

Conclusion and Perspectives

1.3D CMOS MAPS adapted to inter layers of ILC vertex detector is designed, in a 12 µm pitch, with delayed readout circuits

2.Split the signal collection and processing functionnalities, single point resolution < 3 µm with binary output.

3.Future development :
Tier-1: Charge collection system
Tier-2: CMOS process adapted to analog & mixed signal processing
Tier-3: Digital process