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A 12 µm pitch CMOS Pixel Sensor Designed in the 3DIT for the ILC Vertex Detector

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CMOS Monolithic Active Pixel Sensors (MAPS) combined with 3D Integrated Technologies (3DIT) offer new opportunities to meet the challenging requirements of the next generation pixel technologies. This paper presents a 3D CMOS pixel sensor design adapted to the innermost layer of the ILC vertex detector. It contains a matrix of 96x256 pixels; each integrating, in a 12µm pitch, a sensing element, a preamplifier, a shaper, a discriminator, a 5-bit Time-to-Digital-Converter (TDC) and a delayed readout microcircuit. It was realised in a commercial CMOS-130nm technology. The paper describes its architecture and expected advantages with respect to the 2D CMOS MAPS.

Summary

2D CMOS MAPS are foreseen for several applications, ranging from subatomic physics experiments to biomedical imaging devices. They provide an attractive trade-off between granularity, material budget, readout speed, radiation tolerance and power consumption. The vertex detector upgrade of the STAR (Solenoidal Tracker At RHIC) experiment and the EUDET beam telescope, an EU R&D program, are the first places where MAPS will be operated in real experimental conditions. However, the innermost layer of the ILC vertex detector requires pixel sensors with a high single point resolution of 2-3 µm associated to a very demanding readout speed of a few microseconds per frame only. This makes the design of 2D CMOS MAPS particularly tedious. Based on vertical interconnects between IC layers, 3DIT allow combining in a single chip several thinned and bonded silicon microcircuits. They provide better electrical performance, low power consumption, highly miniaturised functionalities, improved form factor and lower fabrication cost. They are particularly well suited to CMOS MAPS since they integrate different CMOS manufacturing processes, each optimised for a given sequence of the charge generation and signal processing chain.

The general idea consists in reproducing a pixel matrix in three IC layers (called tiers). In the bottom tier, each pixel contains a sensing element and a preamplifier. In the intermediate tier, it is composed of an amplifier, a shaper and a discriminator. The top tier is a digital circuit layer, which performs, in each pixel, a time to digital conversion for the first hit detected with a time resolution of about 30 µs and flags a potential second hit. For the sake of power consumption, the tier features a delayed readout, adapted to the ILC beam time structure. All these parts should be integrated in a 12 µm pixel pitch.

For the first prototyping step, the circuits foreseen to be integrated in the bottom and middle tiers are laid out in a single tier. The design features a matrix of 96 x 256 pixels, with a 12 µm pixel pitch. Aside of the pixel matrix, the chip hosts test auxiliary blocks such as PLL and 8b-10b encoder to serialize and transmit data out of the chip at a rate of 25 MHz.

The contribution to the workshop will expose prominent design features of the 3D chip architecture and will provide simulation results illustrating its expected operation performances, and highlight its benefits as compared to 2D pixel sensors.

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