Replacing full custom DAQ test system by COTS DAQ components on example of ATLAS SCT readout

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Abstract

A test system developed for ABCN-25 for ATLAS Inner Detector Upgrade is presented. The system is based on commercial off the shelf DAQ components by National Instruments and foreseen to aid in chip characterization and hybrid/module development complementing full custom VME based setups.

The key differences from the point of software development are presented, together with guidelines for developing high performance LabVIEW code. Some real-world benchmarks will also be presented together with chip test results.

The presented tests show good agreement of test results between the test setups used in different sites, as well as agreement with design specifications of the chip.

I. Introduction

The building blocks of a modern high energy physics experiment are complex structures, often built with minimum material budget in order to maintain required performance, which implies stringent limitations on the components' assembly way. In the later stages of operating the detector, radiation fields may further increase the effort needed for repairs and maintenance.

Due to the above requirements, the electronic components (in particular ASICs) for HEP experiments require careful testing of the chosen components, with the whole system including many self-test scenarios.

Characterisation of the prototype ASICs from first wafers as well as semi-mass testing of production wafers need robust test systems, including both fast digital communication as well as intrincate analogue measurements. Analogue measurements are performed predominantly in R&D phase of the component design, with test scope enveloping more and more complicated scenarios of digital testing in further design life cycle stages, including system level tests of completed detector assemblies. The key property of the system changes fluently from flexibility and fast startup times in the first test stages to speed and reliability for the commisioned collaboration approved test system in later stages.

Previous generation of chips to be used in LHC was usually tested with state-of-the-art custom systems built specifically for this particular purpose, with significant fraction of total project work-hours being devoted to building accompanying electronics. When developing test systems for components being currently installed in the LHC experiments there were no readily available commercial DAQ components with performance sufficient for extensive testing of component at 40 MHz (and beyond, because for many components performance margins were checked with e.g. 50 MHz main clock frequency to account for radiation effects). VME bus was in common use for previous generation setups.

Using commercially available DAQ components for digital communication with device under test is now possible with relative ease when using digital communication between the test system and device with frequencies well above forementioned base LHC frequency of 40 MHz. The electronics designed for the upgrade of ATLAS experiment SCT is foreseen to transmit data with up to quadruple data rate of 160 Mbps (single data rate).

This paper describes the system (ABCNIDAQ) developed for testing first batches of ABCN (Atlas Binary Chip Next) integrated circuits with help of National Instruments high speed digital input-output card (NI-PCI or NI-PXI 6562) within LabVIEW environment. The system is fit for measurements of various components, including single chips mounted on prototype PCBs as well as chip assemblies used for exercising the various powering schemes and prototype module hybrids. Further extension of the system for tests performed at detector stave level is foreseen.

II. Components to be tested by presented setup

A. ABCN-25 readout chip

Current Atlas Binary Chip Next (ABCN) prototype flavour (ABCN-25) is a 128 channel ASIC implemented in 0.25 μm CMOS technology, for use with semiconductor strip sensors intended for upgrade of the ATLAS Inner Detector. The block diagram of this chip is presented on Figure 1. The chip inherits large part of its architecture from ABCD chips build for current ATLAS Silicon Tracker (SCT). Those chips were built in 0.8 μm Bi-CMOS DMILL technology [1]. The main functionality differences between the two mentioned chips are presented below.

ABCN-25 implements a slightly modified communication protocol compared to ABCD, which required modifications in the already existing test systems. Furthermore, the crucial components of the setups used for testing ABCD chips are no longer available for new users, providing the need to implement a new

family of systems based on commercial DAQ components. National Instruments LabVIEW environment has been chosen for ease of programming and interfacing to selected NI hardware presented in section III..

Later prototypes of ABCN developed in either 130 nm or 90 nm are foreseen to maintain backward compatibility needed to operate them with the system described in [2].

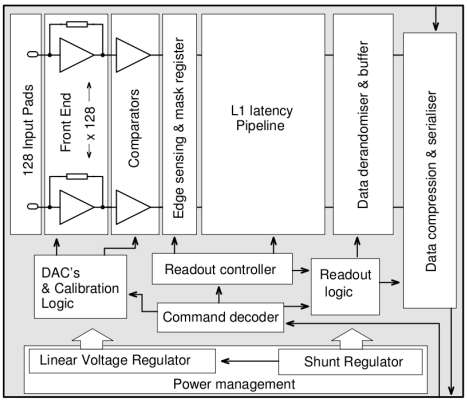

Figure 1: ABCN-25 block diagram

ABCN preamplifier architecture is designed to work with input signals of both polarities (coming from both p or n type strips), as well as with different strip lengths [4].

Large foreseen increase in the channel count, as well as sensor granularity of the future upgraded ATLAS Inner Detector requires novel approach to the problem of power distribution within detector volume. The document [3] describes various powering schemes to be tested in order to keep the power consumed reasonable. In order to test the feasability of various powering schemes of digital and analogue parts of the chip, on-chip regulator circuitry was added.

Single Event Upset detection and correction circuits in crucial areas were also added. All but the Mask registers inside the chip are of write/read type to provide means of checking if the chips' configuration is consistent with the required one. In total, there's 13 different on-chip registers compared to 6 in the current ABCD. To facilitate the identification of chips and decrease the amount of possible mapping errors in the larger system, each chip is provided with a 16-bit fuse register with non-changeable ID number.

The ABCD-25 chip may operate in "single clock mode" with single 40 MHz clock (just as ABCD), or in "double clock mode" where there's additional 80 MHz clock signal provided for driving the data link from the chip to the outside world with doubled speed. In such scenario chip input data rate is 40 Mbps, and output data rate is 80 Mbps.

B. Readout chain architecture

At present, there is no final chosen design of the detector module nor any higher level structures. Nevertheless, the readout chain architecture seems already frozen. Most probably, the chips will be assembled on a flex hybrid with two columns, each consisting enough chips to process signals from between 1000 and 2000 strips (final channel count per chip is not yet decided). The diagrams on figures 2 and 3 show the two possible readout scenarios.

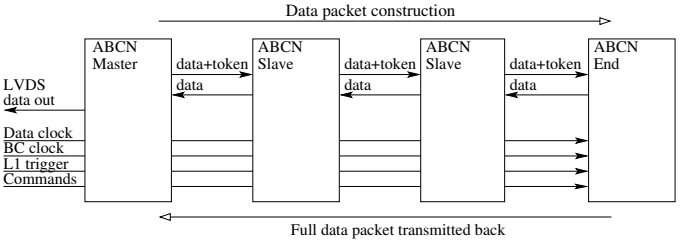

Figure 2: Readout chain diagram in standalone mode

In the standalone readout mode, very similar to the ABCD readout, the Master chip, upon receiving the trigger from the higher level DAQ sends the header, L1 trigger and beam crossing clock (BC clock) counter values, its own data and token to the next chip in the chain, which adds its own data and passes the packet and the token to the next chip. The End chip (typically at the end of the 10 chip column) also adds a specific trailer to mark the end of data and the data is succesively passed back to the Master chip to be transmitted out.

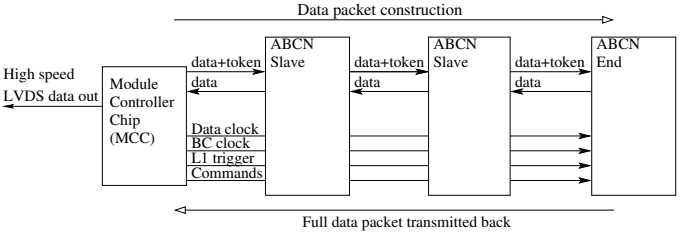

Figure 3: Readout chain diagram in Module Controller mode

In the module controller mode, there is no Master chip in the chain, all the chip but the End one are Slave chips. The local Module Controller Chips (MCC) will transmit triggers to the group of readout columns, gathering the data back and combining the packages to be transmitted out at 160 Mbps rate. For brevity, figure 3 shows only one column of three ABCN chip connected to MC.

Both the standalone chains and future MC chains may be exercised using the same presented setup, for ABCN chips operating either in single or double clock mode.

III. Test systems used

A. SCTDAQ test system

The most important from DAQ point of view part of the systems used for testing the ABCDs as well as hybrids and mod-

ules used for building the ATLAS SCT was the Multichannel Silicon Tracker ABCD Readout Device (MuSTARD). It was a custom-built FPGA based VME module meant for operating 12 datastreams received from ABCD chips. It's onboard circuitry receives, decodes and stores the received data, with possibility of realtime histogramming of the incoming events and transmitting the results to the host PC via VME interface. The hardware based data handling enables the possibility of issuing consecutive triggers at maximum rate, with triggers send immediately upon detecting a trailer from the previous trigger data package. The description of the whole VME system used may be found in [7].

B. ABCNIDAQ test system

ABCNIDAQ test system consists of a set of LabVIEW developed procedures running on the host PC, with actual generation and acquisition of data using the National Instruments 6562 cards in either PCI or PXI flavour, complemented in different scenarios with various other equipment. In particular, for single chip test PCBs the NI-USB 6509 card (static 96 TTL I/O lines) is used for providing logic levels used for configuring the ABCN-25 chip (settings like chip address, readout/clock mode configuration, operation of the built in analogue multiplexer for DAC testing and so on). Other equipment used were the GPIB controlled generator for performing clock frequency sweeps and a multimeter used for DAC measurements (for details see [9] and [10]).

The heart of the system is NI6562 PCI/PXI module being in principle high speed, 200 MHz (up to 400 Mbps per channel in DDR mode) 16 channel digital LVDS-standard board. The device provides hardware timed, synchronous, generation and acquisition of LVDS signals, compatible with signals used by ABCN-25 chip . One readout chain as described above requires one output channel (Command on figure 2) and one input channel (LVDS data out, same figure) for data acquisition. In single clock mode BC clock is exported on a dedicated CLK line provided on the board, in double clock readout mode the faster data clock is there, with BC clock being generated on one of the output channels of NI-6562. Thus, a 16 channel card may serve up to 8 readout chains in single clock mode or up to 7 in double clock mode. The trigger lines present on the device (PFI), together with the so-called "scripted generation" provide the flexibility needed to perform fast, hardware timed tests. Scripted generation uses defined waveforms as building blocks for tests . The commands configuring the chips, followed by a series of L1 triggers are sent in one burst, with acquisition trigger issued upon generation of each L1. Thus, only the interesting part of the chip response is gathered for further analysis, with separate events being stored in different acquired records.

Unfortunately, real-time data decoding is not possible so the acquired records may be significantly longer than the real incoming data package. This is a drawback of this system, which could be overcome by using the directly accessible FPGA product from Reconfigurable I/O (RIO) family of National Instrument products, which didn't have all the necesary components readily available at the time of starting the development of the presented setup (late 2008). Such limitation may slow down significantly the tests performed for measuring the intrinsic noise characteristics of a component.

IV. Example ABCNIDAQ results

The system described above was used for the part of characterization and functionality verification of the first engineering run ABCN-25 chips. In particular, the presented system was the first to confirm correct operation of the chip in double clock scheme, which shows the fast startup time of the approach based on a well tested and supported commercial DAQ component. To demonstrate the flexibility of the presented system, few example results are shown below - so called three point scan showing analogue parameters calculated from digital scans for a single chip test board, an example of a threshold DAC linearity measurement, and an example of a test showing usable range of calibration pulse delay for the two data links, each reading out a column of 10 chips on a prototype hybrid. More results performed with both ABCNIDAQ and modified SCTDAQ setups may be found in [6]. In general, the results obtained are consistent with each other and no measurement artifacts have been observed.

A. Three point gain

Three point gain scan is performed by a threshold scan for 3 different input calibration charges. For each scan, the value of threshold corresponding to 50 % occupancy is found and a straight line fit is made to calculate the value of gain and offset for each charge. Output noise sigma in mV is recalculated to obtain equivalent input noise charge.

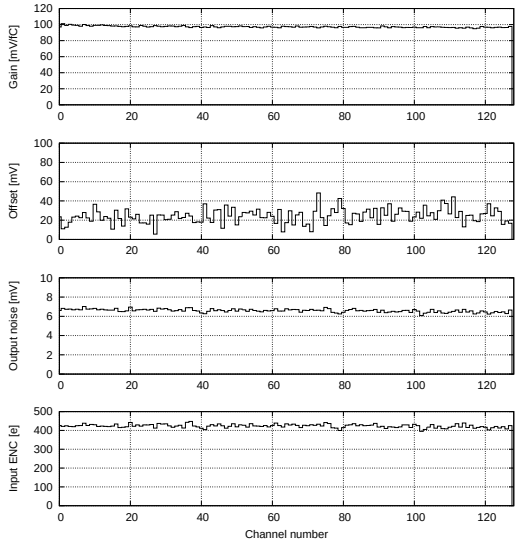

Figure 4: Three point gain scan for 1.0, 1.5 and 2.0 fC, 1000 triggers per point

The figure 4 shows the results of a three point gain scan matching the required design parameters of the chip (around 100 mV/fC gain and around 400 e input equivalent noise charge).

B. DAC linearity

The figure 5 presents the voltage at the 8-bit threshold DAC output. The on-chip analogue multiplexer was set up to transfer the mentioned DAC output voltage to a test pad connected to a GPIB controlled multimeter, while the ABCNIDAQ setup provided configuration signals for the multiplexer as well as changing the DAC values.

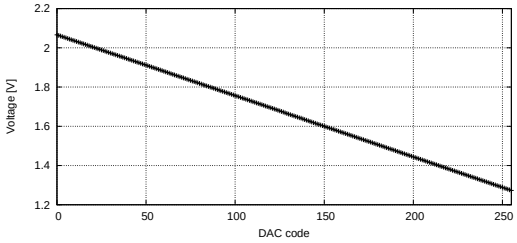

Figure 5: Threshold DAC output voltage vs DAC code.

The range and step of the DAC match the design values of 800 mV and 3.2 mV respectively, and no significant nonlinearity is observed (output voltage varies from 2.066 V for 0 code to 1.272 V for 255 code).

C. Calibration delay scan

The calibration pulses sent via internal calibration circuit to perform scans needed for deriving the analogue frontend parameters need proper timing. Figure 6 shows the dependence of the measured occupancy on the calibration pulse delay setting for each of the channels of the two readout chains mounted on a prototype hybrid described in [8].

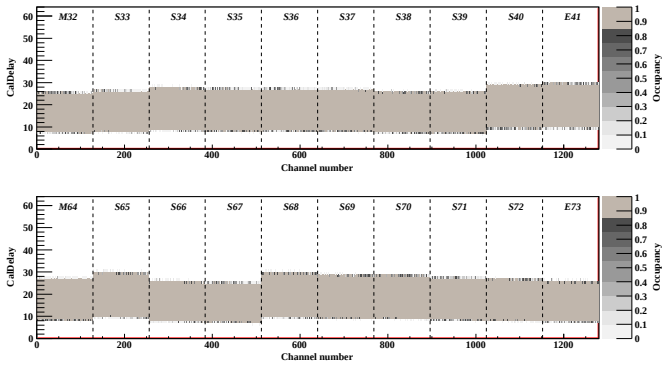

Figure 6: Example Strobe Delay Scan

The calibration pulses sent via internal calibration circuit to perform scans needed for deriving the analogue frontend parameters need proper timing. Figure 6 show dependence of the measured occupancy on the calibration pulse delay setting for each of the channels of the two readout chains mounted on a prototype hybrid described in [8].

The two columns of ten chips each were read out using two different channels of the NI-6562 board at the same time. The results show correct decoding of the multichip data and simultaneous operation of two readout chains at the same time. Some chip to chip variation of the perceived delay range due to process variations is visible, and the overlap region betweeen the chips is sufficient for common setting of the delay for all the chips sharing the same data link. The sharp transition between full occupancy (gray) and zero occupancy (white) regions with virtually no transition area shows good performance of both the calibration circuit and the preamplifier/shaper/discriminator chain in the channel.

V. LabVIEW programming techniques used

The software used in the presented system utilizes LabVIEW Professionnal Development System. XML manipularion libraries are used for handling the configuration classes. The input/output channel assignment, chip addressing, clock config, number of connected hybrids and chips, chip configuration registers are all stored in the XML config files specific to the component tested as well as to the setup location (e.g. different cable lenghts that need to be accounted for in the delay settings). The XML schema provides means of checking the config validity at any given point. The configuration objects are implemented using LabVIEW object oriented programming scheme to keep the source code uncluttered and easy to maintain. The subroutines crucial for application speed (in particular the data decoder) had to be implemented in non-object programming way for speed. As the graphical data driven programming paradigm hides some part of the implementation from view, even the experienced text-based programmers may experience difficulties in getting fast graphical code.

The development of applications running on nowadays multi-core machines with processors lets one speed up the execution speed by splitting the code into multiple threads. In LabVIEW, independent fragments of code (like separate loops) are automatically distributed to run on different CPU cores. Native LabVIEW threads include the Panel Update thread which handles updating the application UI. Care must be taken in order to avoid the performance drop caused but too frequent calls to application Front Panel (User Interface) controls and indicators. Most of the arithmetic functions used in LabVIEW are inherently polymorphic. E.g. simple arithmetic multiplication may be used for operation on two integers, two floats but also for two 1-D vectors or a 2-D array and a constant. Thanks to that, scaling a whole array of double precision data by calibration factor may be done via a single Multiply function call, not element by element. One may also use a set of included in-place array operations to avoid excessive memory usage and data copy overhead.

During the development of the ABCNIDAQ system the benchmarks for array operations in LabVIEW were performed for detecting and avoiding the possible bottlenecks. Comparison was done between dynamic and static array allocation for double precision data types. Both scenarios involve a for loop running given m number of times with each iteration placing

one double precision number in the array at index i. In dynamic case InsertIntoArray function was used, which "inserts an element or subarray into n-dimensional array at the points you specify by index" according to the documentation. For static case, 1D m element array of double precision numbers has been preallocated using InitializeArray function, followed by elements being written to it inside the for loop using the ReplaceArraySubset, which "replaces an element or subarray in an array at the point specified by index". The execution times on a modern, 4 GB memory, double core CPU notebook machine are presented in table 1 The difference comes from an overhead of copying and reallocating the full array needed by InsertIntoArray function, despite its first glance similarity to Replace ArraySubset function.

Table 1: Comparison of execution time between to methods of writing data to array

Number of array elements filled	Time taken InsertIntoArray	Time taken ReplaceArraySubset
100000	14 seconds	20 miliseconds
1000000	56 minutes	50 miliseconds

The analysis of data from binary readout architecture chips (including the ABCN-25) involves fitting the

$$f(V_{th}) = \frac{1}{2} - \frac{1}{2} erf(\frac{occ(V_{th}) - V_{t50}}{\sigma\sqrt{2}})$$

to the threshold scan data, where V_{th} is the threshold voltage value and $occ(V_{th})$ is the hit occupancy for given injected charge, and V_{t50} and σ being the parameters of the fit. Such fits are done multiple times for each channel and their speed is crucial for the overall performance of the developed test system. The fits are done using the Levenberg-Marquardt method, and the same machine was used for benchmarking the two implementations of the test function, with results being presented in table 2. The test function values for each threshold scan datapoint were calculated either via a Mathsript node (LabVIEW way of calling external Matlab libraries) or constructing the cumulative Gaussian distribution function using the built-in arithmetic functions and numerical point by point integration. Native function performance exceeds the external library call method by nearly 3 orders of magnitude.

Table 2: Time taken for fitting the $f(V_{th})$ function to a 200 point threshold scan data

	Mathscript	Built-in arithmetics
Time taken	9 seconds	12 miliseconds

VI. Acknowledgements

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VII. Summary

ABCNIDAQ, the test system to be used in the ATLAS Inner Detector Upgrade programme, based on commercial-off-the-shelf DAQ components from National Instruments and programmed within the LabVIEW environment, was built. The software part of the system proved to be robust and flexible enough to perform a broad range of tests and measurement of prototypes for mentione upgrade programme, including chip functionality verification, chip analogue parameter measurements and despite the lack of hardware-based data processing like FPGA based systems, the system speed and scalability seems sufficient for chip and hybrid level tests. The setup was used for tests ranging from single chip tests to tests of a prototype 20 chip hybrid board, soon to be followed by a 40 chip "half module" and foreseen to be extended to utilise 3 NI 6562 boards in parallel.

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