Contribution ID: **60** Type: **Oral**

Replacing full custom DAQ test system by COTS DAQ components on example of ATLAS SCT readout

Tuesday, 22 September 2009 15:00 (25 minutes)

A test system developed for ABCN-25 for ATLAS Inner Detector Upgrade is presented. The system presented is based on commercial off the shelf DAQ components by NI and foreseen to aid in chip characterization and module/hybrid development complementing full custom VME based setups. The key differences from the point of software development are presented, together with guidelines for developing high performance LabVIEW code. Some real-world benchmarks will also be presented together with chip test results. The presented tests show good agreement of test results between the setups, as well as agreement with design specs of the chip.

Summary

Characterization of the engineering run ASICs from first wafers as well as further testing detector modules need robust test systems, including both fast digital communication as well as intricate analogue measurements (analogue measurements being performed predominantly in R&D phase of the components' design). The key property of the system changes fluently from flexibility in the first test stages to speed and reliability for the commissioned collaboration approved test system in later stages. Previous generations of chips used in the LHC experiments were usually tested with state-of-the-art custom systems built specifically for this particular purpose, with significant fraction of total project work-hours being devoted to building accompanying electronics.

Few years ago there were no readily available commercial DAQ components with performance sufficient for extensive mixed-mode testing of components at 40 MHz. Using commercially available DAQ components for digital communication with device under test is now possible with relative ease with digital communication between the test system and DUT with frequencies well above the mentioned base LHC frequency of 40MHz. The electronics designed for the upgrade of ATLAS Inner Detector Readout is foreseen to transmit data with up to 160Mbps data rate, which is still achievable with relatively affordable off-the-shelf DAQ equipment.

This paper describes the system developed for testing prototype ABCN-25 chips with help of National Instruments high speed digital input-output card within LabVIEW environment. The heart of the system is NI6562 PCI/PXI module being in principle high speed (up to 200/400Mbps per channel SDR/DDR) 16 channel digital communication LVDS-standard board. The device is equipped with 32MB on-board memory and provides hardware timed, synchronous, hardware triggered generation and acquisition of LVDS signals, compatible with signals used by ABCN chip outside world communication. The performance of the NI6562 card is sufficient to test current prototype of ABCN chip with typical 80Mbps data rate (single edge) as well as future electronics (module controller chip) operating at 160 Mbps. Both the generation of stimuli and getting the response is done using the same device, without signal integrity and synchronization problems. The presented system provides base for testing both single chips as well as assemblies of up to 7 bidirectional data links in typical 80 MHz data transmission clock, 40 MHz master BC clock scenario. Each data link may read and drive many readout chains of many chips each, hence the suitability of the system to perform hybrid and module system level checks as well as in various unit test scenarios required (e.g. serial powering scheme testing).

The presented results show usability and flexibility of the COTS DAQ based setup. Agreement between the setups used is shown, as well as some benchmarks showing the pros and cons of COTS and custom based approach.

Primary author: Mr DWUZNIK, Michal (Faculty of Physics and Applied Computer Science AGH Univeristy of Science and Technology)

Co-author: Mr GONZALEZ SEVILLA, Sergio (DPNC, University of Geneva)

Presenter: Mr DWUZNIK, Michal (Faculty of Physics and Applied Computer Science AGH Univeristy of Science and Technology)

Session Classification: Parallel session B2a - Production, testing and reliability

Track Classification: Production, testing and reliability