The GBT-SCA, a radiation tolerant ASIC for detector control applications in SLHC experiments

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Abstract

The GigaBit Transceiver project aims to provide a new chipset to build fast bidirectional optical links between the read-out electronics on a HEP detector system and its counting room. The GBT link and protocol is designed to carry three distinct types of information from and to the detector:

- the data collected from the detector, flowing mostly in the direction of the counting room,

- the fast timing information (clock and trigger) from the counting room to the electronics in the detector,

- the control and monitoring information that flows in both directions.

A typical GBT link system is build around a chipset made of:

- the GBTX chip, i.e. the main controller and serializer/de-serializer of the link

- the GBT-LD and GBT-IA interfacing the serializer to the fast optoelectronic components

- the GBT-SCA interfacing the GBTX to the slow control interfaces as described below;

- in addition, an implementation of the GBT logic is foreseen to be embedded in commercial FPGAs in the counting room, serving as many embedded GBTs as the FPGAs technologies will allow.

The GBT-SCA illustrated in this poster is a rad-tolerant ASIC that is used to connect to a number of popular control oriented interfaces. These interfaces are expected to be implemented in the front-end chips used typically in particle physics detectors. These interfaces are:

- a set of I2C ports

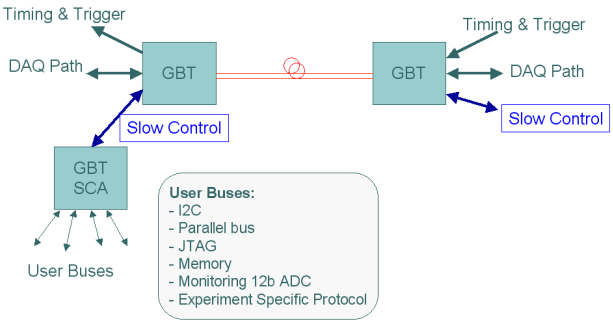
- a parallel bidirectional bus

- a JTAG port

- a number of analog inputs monitored by a 12 bit ADC

- a simple memory-like bus interface.

Slow Control System Architecture

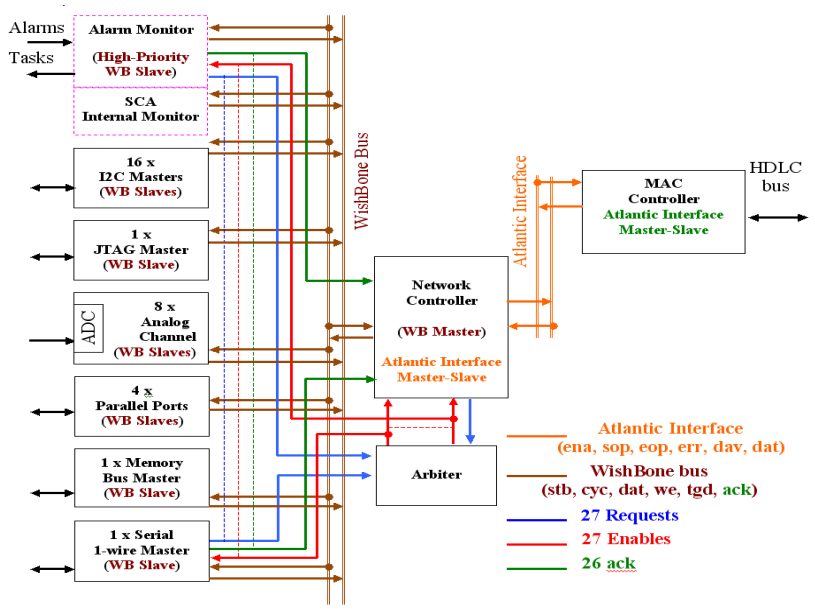


The GBT-SCA translates the transport protocol supported by the GBTX into those of the above-mentioned interfaces in a transparent manner. The interfaces are visible to the software programmer in the counting room as a set of "ports" which are capable of executing commands and reporting status information. For example, the programmer can send to a given SCA controller a command using the GBT transport for reading a given byte from a specified I2C address, or performing an ADC conversion and reporting the result back.

The GBT-SCA utilizes a bandwidth of 80 Mbit/sec from the ~4.8 Gbit/sec carried by the GBT link.

The chip is being designed for implementation in a commercial 130nm CMOS technology with a number of special design techniques for SEU mitigation. Apart from the ADC macro block, realized as a full custom cell, all of the circuitry is implemented using a standard cell library qualified for the LHC environment.

ASIC block diagram



The GBT-SCA contains the following blocks as shown:

On the GBT side

- One MAC Controller

- One Network Controller (NC)

- One SCA Monitor

- One Arbiter based upon Round-Robin technique to enable the user ports, the monitors or the NC, one at a time, to send data backwards towards the GBT upon reply of previous requests.

On the user side there are 24 I/o ports – one copes with 8 analog inputs -:

- 16 I2C master controllers

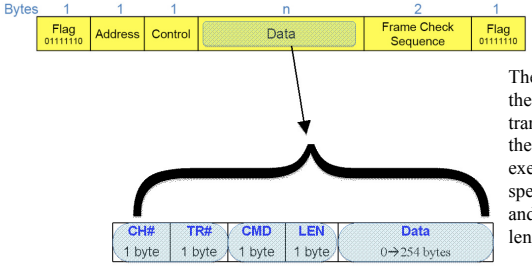
- 1 JTAG master controller

- 1 ADC and is used to monitor up to 8 analog signals in the front-end electronic systems.

- 4 I/O like parallel bus controllers such as the ones used in the Motorola PIA etc

- 1 memory-like bus controller to access devices such as static memories, A/D converters etc

- 1 serial m-wire bus to access simple devices such as temperature sensors and EEPROMS



SCA Packet

The channel number (CH#) identifies the user port to be addressed, the transaction identifier (TR#) facilitates the verification of the command execution, the command type (CMD) specifies the read or write operation, and the lenght (LEN) specifies the length of the Data field.

Summary

The GBT-SCA ASIC aims to provide a universal interface between the counting room and a number of popular interfaces implemented in the embedded electronics in a detector. It uses the physical and logical transport of the GBT link in a transparent manner. The chip is being designed for low-power and small size, thus making its embedding in the typically space constrained front-end electronic cards easier.