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A 5 Gb/s Radiation Tolerant Laser Driver in 0.13 um CMOS technology

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A laser driver for data transmission at 5 Gb/s has been developed as a part of the GigaBit Transceiver (GBT) project. The GigaBit Laser Driver (GBLD) targets High Energy Physics (HEP) applications for which radiation tolerance is mandatory.
The GBLD ASIC can drive both VCSELs and some types of edge emitting lasers. It is essentially composed of two drivers capable of sinking up to 12 mA each from the load at a maximum data rate of 5 Gb/s, and of a current sink for the laser bias current. The laser driver also include pre-emphasis and duty cycle control capabilities.

Summary

The GBT project aims to design a radiation tolerant optical transceiver at 4.8 Gb/s for the future upgrades of the LHC experiments. The GBT will be able to transmit and receive data, trigger signals and control information, thus acting as an interface between the front-end electronics and the data acquisition, trigger and detector control systems.
The GBT chip set will include a laser driver, named GBLD, targeted at driving both VCSELs and some types of edge emitting lasers. The circuit is designed for both single ended and differential connection.
A GBLD prototype has been designed and is currently under test. The prototype is designed for a maximum output data rate of 5 Gb/s and is composed of two drivers and a current sink for the laser bias current. Each driver can sink between 2 and 12 mA from the load with a 50 Ω output impedance. The current sink is controlled by a 6 bits DAC. The two drivers can be connected in parallel, thus doubling the maximum output current and halving the output resistance. The latter configuration is better suited for edge emitting lasers. The laser bias current can be adjusted between 2 and 43 mA via an 8 bit DAC.
Pre and de-emphasis can be independently set on the rising and falling edges of the signal, in order to compensate for the bandwidth limitations of the optoelectronic components and transmission media employed. The emphasis can be adjusted both in height (between 0 and 12 mA) and in width (between 60 and 90 ps) by 4 and 2 bits DACs, respectively. The laser response can also be compensated by a duty cycle control circuit, controlled by a 3 bits DAC. The duty cycle control range is around 20% at 5 Gbps.
The driver architecture is based on a sequence of differential stages with resistive load. For the pre-driver the inductance peaking technique has been used in order to improve the bandwidth. Two 1 nH spiral inductors have been integrated.
The control DACs can be programmed via a I2C digital interface. Seven 8-bits control registers are used to store the configuration parameters. The control logic has been designed in order to be resistant to Single Event Upsets (SEUs) via Triple Modular Redundancy (TMR). An asynchronous correction logic has been adopted in order to provide error correction when the I2C clock is not present.
The chip has been designed in a CMOS 0.13 µm technology. The chip size is 2×2 mm2 and is packaged in a 5×5 mm2 QFN28 package. Double bonding has been used on the supply and high speed signals in order to decrease the bonding wire inductance.
This work describes in detail the operation principles of the GBLD circuits and the experimental results.

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