Upgrade of the Cold Electronics of the ATLAS HEC Calorimeter for sLHC Generic Studies of Radiation Hardness and Temperature Dependence

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Abstract

The front-end electronics (signal amplification and summation) of the ATLAS Hadronic End-cap Calorimeter (HEC) is operated at the circumference of the HEC calorimeter wheels inside the cryostats in liquid argon (LAr). The present electronics is designed to operate at irradiation levels expected for the LHC. For operation at the sLHC the irradiation levels are expected to be a factor ten higher, therefore a new electronic system might be needed. The technological possibilities have been investigated. For different technologies generic studies at the transistor level different have been carried out to understand the radiation hardness during irradiation up to integrated n fluxes of $2{\times}10^{16}\ n/cm^2$ and the behaviour during cool-down to LAr temperatures. An S-parameter technique has been used to monitor the performances during irradiation and cool-down. In addition, DC measurements before and after irradiation have been compared. Results of these investigations are reported. Conclusions are drawn and the viability is assessed of using technologies for carrying out the design of the new HEC cold electronics for the sLHC.

I. Introduction

The LAr system consists of a barrel region and two end-cap / forward regions. As seen from simulation studies, the radiation levels increase with $|\eta|$. From the barrel to the endcap and from the endcap to the forward calorimeters the flux and average energy of the particles from min-bias events increases with the consequent growth of multiplicity and density of shower particles. This results in a power density, and hence radiation flux, deposited in the calorimeter reaching levels not seen in previous collider detectors. The ATLAS calorimeters are designed to cope with the highest luminosity of $\mathcal{L} = 10^{34}$ cm^{-2} s^{-1} foreseen at the LHC.

Under sLHC conditions both the peak and the integrated luminosity collected over an anticipated sLHC lifetime of ten years will typically increase by a factor of ten. One element which might be affected by integrated luminosity is the front-end electronics of the HEC which is located in relatively high radiation fields at the perimeter of the HEC calorimeter wheels. At the position a n fluence of $0.2 \times\ 10^{14}\ n/cm^2$, a γ dose of 5 kGy and a hadronic fluence of $1.2 \times\ 10^{12}\ p/cm^2$ are expected after ten years of LHC operation at highest luminosity.

II. Active pad concept of the HEC cold electronics

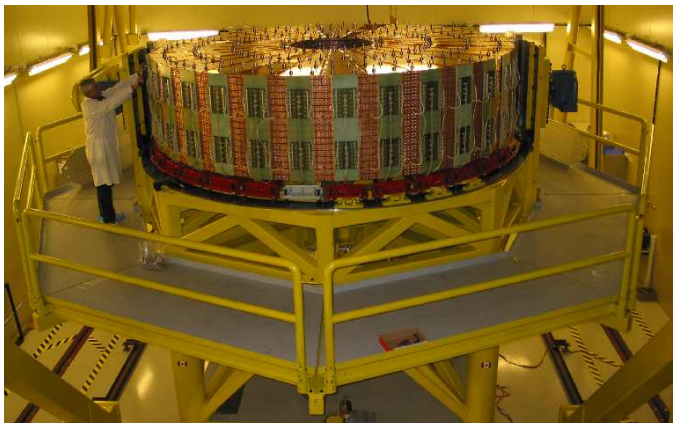

Figure 1: A HEC wheel fully assembled on the assembly table showing the 'active pad' electronics.

The signal processing of the HEC employs the notion of 'active pads' which keeps the detector capacities at the input of the amplifiers small and thereby achieves a fast rise time of the signal [1]. Short coaxial cables are used to send the signals from the read-out pads to preamplifier and summing boards (PSB) located at the perimeter of the wheels inside the LAr. The lateral pad segmentation is $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ up to $\eta = 2.5$ and $\Delta\eta \times \Delta\phi = 0.2 \times 0.2$ for higher η while the longitudinal read-out segmentation is fourfold. The pad capacitance varies from 40 to 400 pF which yields a rise time variation from 5 to 25 ns. The signals from a set of preamplifiers from longitudinally aligned pads (2, 4, or 8 for different regions of the calorimeter) are actively summed inside the chip forming one output signal, which is transmitted to the cryostat feed-through via the PSB's.

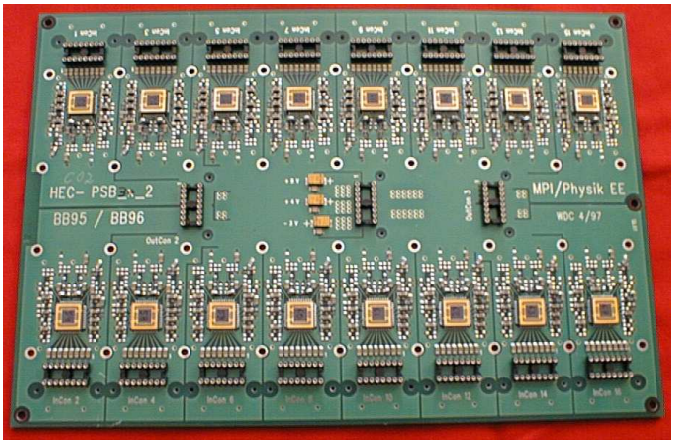

Figure 2: Picture of a PSB board.

The PSB's carry the highly integrated amplifier and summing chips in Gallium-Arsenide (GaAs) MESFET technology. The GaAs TriQuint QED-A 1 μm technology has been selected for the front-end ASIC because it offers excellent high frequency performance, stable operation at cryogenic temperatures and radiation hardness [2]. The front-end chip consists of 8 identical preamplifiers and two drivers. The summing scheme is implemented with external components and interconnections made on the PSB. The Fig.1 shows a fully assembled HEC wheel in the horizontal position on the assembly table with the PSB boards (see Fig.2) at the outer circumference.

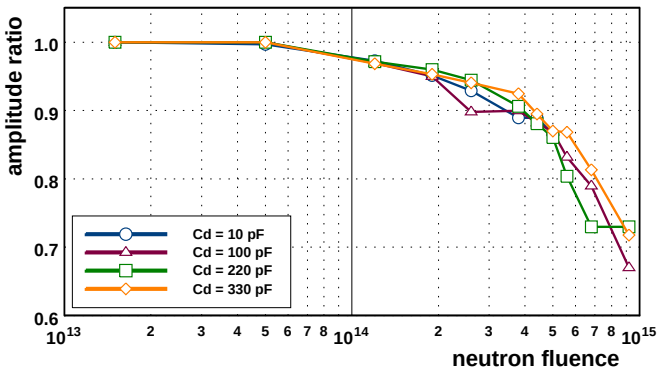

Figure 3: The signal amplitude measured after values of n fluence from 1.5×10^{13} to $9 \times 10^{14} n/cm^2$ for four different detector capacities. Shown is the ratio to the signal amplitude before the irradiation.

It is known that GaAs is a radiation resistant semiconductor. The radiation hardness has been studied at the $IBR-2$ reactor in Dubna, Russia with a set of pre-production chips. Various types of tests have been performed. Seven chips were exposed to a total fluence of fast n of $(1.11 \pm 0.15) \times 10^{15}$ n/cm^2 and an integrated γ dose of 3.5 ± 0.3 kGy. A second set of 8 chips was irradiated with γ's up to a total dose of (55 ± 8) kGy accompanied by a fast n fluence of $(1.1 \pm 0.2) \times 10^{14}$ n/cm^2. In these tests the chips were kept in a cryostat filled with liquid nitrogen. The standard set of characteristics like transfer function, rise time, linearity and equivalent noise current (ENI) of preamplifiers was measured. The measurements show that the preamplifier characteristics start to degrade when the n fluence exceeds approximately 3×10^{14} n/cm^2. The Fig.3 shows the degradation of the amplitude with n irradiation for four different values of input (detector) capacitance.

Similar measurements with γ- irradiation show that the characteristics stay unchanged up to a dose of at least 50 kGy. Both boundary values are well above the radiation levels expected in the final ATLAS environment at LHC.

In summary, the radiation hardness of the cold HEC electronics against all three types of radiation has been studied and compared to ATLAS requirements. It has been found that n irradiation is by far the most dangerous radiation type yielding the smallest safety margin.

Another important aspect of the cold electronics is the heating of the chips that can finally result in bubbling of the liquid argon. The bubbles propagating to a LAr detector gap can cause high voltage discharges. Therefore the power consumption has to be kept low.

III. sLHC Requirements for the HEC cold electronics

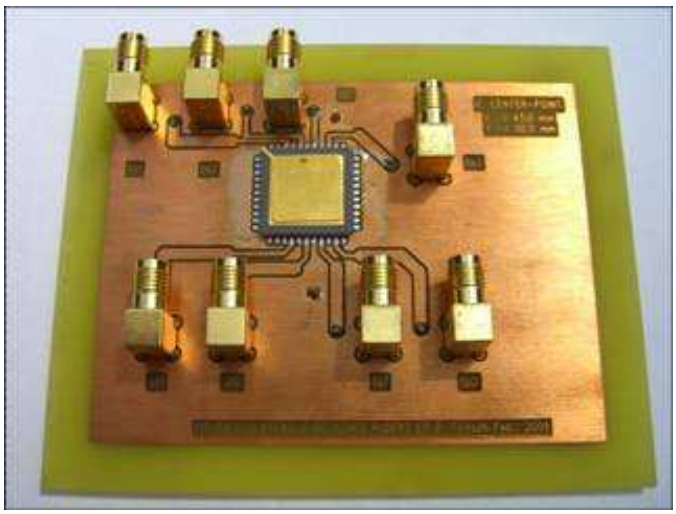

Figure 4: Testboard with IHP transistors with four structures bonded in one ceramic package.

The present ATLAS requirements for the HEC PSB boards have been developped with an LHC design luminosity of $10^{34} cm^{-2} s^{-1}$ corresponding to a n fluence of $2 \cdot 10^{12} n/cm^2$ per year. Assuming an operation of 10 years this yields a safety margin of ~ 15 for the LHC luminosity. Assuming a ten times higher integrated luminosity at sLHC the safety factor is essentially eliminated, i.e. the present HEC cold electronics will be operated at its limit. It is therefore planned to develop a new ASIC that will be ten times more radiation hard against n. If needed, the new chip would be used to replace the present GaAs

chips at the sLHC. For an upgrade the PSB boards at the circumference of the HEC wheel would then be replaced by new, pin compatible PSB boards with more radiation hard IC's. This operation can be done without disassembling the HEC wheels.

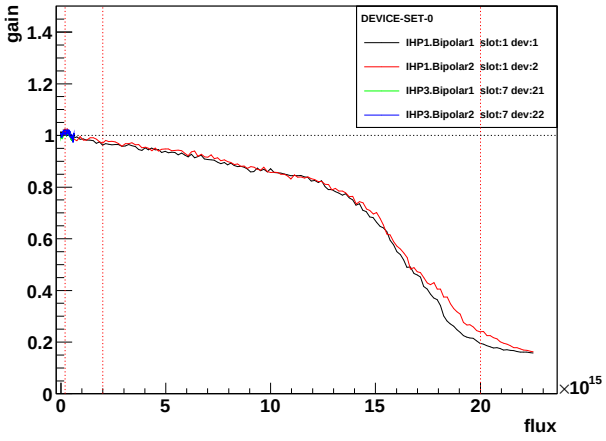

Figure 5: Dependence of the gain of four IHP bipolar transistors on the n flux.

The requirements for the new IC's are:

- radiation hardness for n up to a factor of 10 better, i.e. up to a fluence of a few $10^{15} n/cm^2$;
- low power consumption to stay safely away from the LAr boiling point at the operational Ar pressure and temperature. In consequence, the power consumption should not exceed the present level of $< 0.2\ W$;
- as most of the QC tests have to be done at room temperature, the gain of the pramplifiers and summing amplifiers should not vary by more than a factor of two from room to LAr temperature;
- the noise has to stay low, i.e. it should not exceed the present level 50 nA with 0 pF input load or 100 nA with 200 pF load at each preamplifier input; the maximum signal for one preamplifier input is 250 μA, the dynamic range $\sim 5 \cdot 10^3$;
- as only the full read-out channel, i.e. the summed and not the preamplifier signals, can be electronically calibrated, the gain variation of the individual preamplifiers within the IC has to be below 1 %;
- the IC has to be safe against HV discharges in the gaps of the HEC modules;
- the input impedance has to be $50\ \Omega \pm 2\ \Omega$ to cope with the existing cabling scheme;

IV. Results of technology studies

The radiation hardness against n irradiation has been studied for transistors of SiGe (Table 1), Si and GaAs (Table 2) technologies.

Table 1: SiGe transistors studied for radiation hardness against n irradiation.

Material	SiGe	SiGe	SiGe
Transistor	Bipolar HBT	Bipolar HBT	Bipolar HBT
Foundry	IHP	IBM	AMS
Process	SGB25V	8WLBiCMOS	BiCMOS
	250 nm	130 nm	350 nm
		MB and HB	
Type	npn	npn	npn

Typically four structures have been bonded in one ceramic package, which has been mounted on a small testboard. Up to 8 boards have been aligned in the n beam of the cyclotron at Rez/Prague. Protons of 37 MeV impinging on a D_2O target generate a n flux up to $10^{11}\ n/cm^2/s$. The energy spectrum peaks at low energies (1 MeV) with a steep decline towards higher energies. The flux falls steeply off with the distance from the target. The typical integrated flux obtained was of the order of $\sim 2{\times}10^{16} n/cm^2$ for the closest position relative to the D_2O target. The performance of the transistors has permanently been monitored with a network analyzer recording the full set of S-parameters. In addition DC parameters (voltages and currents) have been recorded as well.

The Fig.4 shows the testboard with IHP transistors with four structures bonded in one ceramic package. Each of the four transistors has an input and output line connected to the network analyzer via switches.

For the four IHP bipolar transistors the Fig.5 shows the dependence of the gain on the n fluence. The two transistors which are in slot one, i.e. closest to the D_2O target, were exposed to a n fluence of $2.2 \times 10^{16} n/cm^2$, the corresponding n fluence for the equivalent transistors located in slot seven being $\sim 10^{15}\ n/cm^2$. The results show that the gain is rather stable in the range required for sLHC, i.e. up to $2 \times 10^{15} n/cm^2$; it is independent of the irradiation density.

Table 2: Si and GaAs technologies (transistors) studied for radiation hardness using n irradiation.

Material	Si	Si	Si	GaAs	GaAs
Transistor	CMOS FET	CMOS FET	CMOS FET	FET	FET
Foundry	IHP	IHP	AMS	Triquint	Sirenza
Process	SGB25V	SGB25V	BiCMOS	CFH800	
	250 nm	250 nm	350 nm	250 nm	250 nm
Type	nmos	pmos	nmos	pHEMT	pHEMT

Table 3: Loss of gain of the transistors studied for a n fluence of $2 \times 10^{15} n/cm^2$ at two different frequencies.

Material	SiGe	SiGe	SiGe	Si	Si	Si	GaAs	GaAs
Transistor	Bipolar	Bipolar	Bipolar	CMOS FET	CMOS FET	CMOS FET	FET	FET
Foundry	IHP	IBM	AMS	IHP	IHP	AMS	Triquint	Sirenza
Type	npn	npn	npn	nmos	pmos	nmos	pHEMT	pHEMT
10 MHz	5%	5%	5%	4%	4%	3%	0%	4%
40 MHz	3%	2%	5%	2%	3%	3%	2%	2%

For two different frequencies Tab. 3 shows the loss of gain for the transistors studied at a n fluence of $2 \times 10^{15} n/cm^2$. The errors are dominated by systematic effects and are at the few percent level. We observe that all technologies only show a small degradation of the gain up to the irradiation level expected for sLHC.

Another important aspect is the variation of the gain with temperature. This dependence has been studied for all technologies in the required range down to liquid N_2 temperatures. All bipolar technologies show a strong dependence of the operation point with temperature, i.e. they require a voltage adjustment when going from room to liquid N_2 temperatures. This is different for the FET's where the gain variation is rather small within the temperature range studied.

V. CONCLUSIONS

Based on these studies, both options, SiGe Bipolar HBT as well as Si CMOS FET, are under further investigation. Presently preamplifiers are being developed for both technologies. The dynamic range and the noise performance are investigated. We plan to irradiate these prototype preamplifiers in cold in the near future. The final technology selection will be based on these results.

REFERENCES

[1] ATLAS Liquid Argon Calorimeter Technical Design Report, CERN/LHCC/96-41 (1996).

[2] J. Ban et al., Cold electronics for the liquid argon hadronic end-cap calorimeter of ATLAS, Nucl. Instr. and Meth. **A556** (2006), 158.