Report from Power Working Group

Philippe Farthouat, CERN

- Meetings since Naxos
- Serial powering developments
- DC-DC developments
- Next steps

A bit of history

- Power distribution in the upgraded trackers is a common issue for ATLAS and CMS

- ATLAS-CMS working group formed to exchange informations and share developments and measurements methods
  - "The scope of this working should not be (at least for the time being) the definition and design of a general common solution but more the circulation of information and the share of common blocks (e.g. blocks for designing an adhoc convertor or regulator). However it was felt that some parts of the activity would benefit a lot from a common definition. These are the activities dealing with the characterization and those dealing with environmental tests. It was felt that a meeting twice a year is the appropriate frequency."

Last meetings

- One during TWEPP08 in Naxos
- One expected end January 09 at the same time as the SLHC-PP meeting
  - SLHC-PP meeting delayed to end of February very close to ACES
  - ACES power session used instead
- One last Wednesday after the power session

Naxos and ACES agenda

Parallel Session B5 - Power (14:15-15:55)

- **Conveners: Farthouat, Philippe**

time	[id] title	presenter
14:15	[19] Custom DC-DC converters for distributing power in SLHC trackers	MICHELIS, Stefano
14:40	[20] System test with DC-DC converters for the upgrade of the CMS silicon strip tracker	Dr. KLEIN, Katja
15:05	[132] Design Considerations for High Step Down Ratio Buck Regulators	Mr. KHANNA, Ramesh
15:30	[67] Serial Powering of Silicon Strip Modules for the ATLAS Tracker Upgrade	Mr. PHILLIPS, Peter

Parallel Session B5 - Power (16:15-17:30)

- **Conveners: Farthouat, Philippe**

time	[id] title	presenter
16:15	[106] The SPI as an integrated power management device for serial powering	TRIMPL, Marcel
16:40	[49] The Power System Detector Control System of the Monitored Drift Tubes of the ATLAS Experiment	ALEXOPOULOS, Theodoros
17:05	[78] Noise Susceptibility Measurements of Front-End Electronics Systems	Mr. BLANCHOT, Georges

POWER WORKING GROUP (17:30-19:30)

- **Conveners: Farthouat, Philippe**

time	[id] title	presenter
17:30	[158] Introduction	FARTHOUAT, Philippe
17:35	[159] Critical areas and ATLAS next steps	WEBER, Marc
17:55	[160] Commercial DC-DC	Dr. DHAWAN, Satish
18:15	[161] Technologies for a DC-DC ASIC	FACCIO, Federico
18:30	[162] Progress on DC/DC Converters Prototypes	MICHELIS, Stefano
18:45	[163] Enpirion radiation test results	Mr. STETTLER, Matt
19:00	[164] Discussion	

Power distribution, low power design, power simulation - Main Auditorium (12:15-12:55)

- **Conveners: Dr. Horisberger, Roland; Weber, Marc**

time	[id] title	presenter
12:15	[7] DC-DC system architecture	BLANCHOT, Georges
12:35	[8] Serial powering system architecture	PHILLIPS, Peter

Power distribution, low power design, power simulation (cont.) - Main Auditorium (14:00-15:40)

- **Conveners: Dr. Horisberger, Roland; Weber, Marc**

time	[id] title	presenter
14:00	[9] Buck DC-DC design and implementation	MICHELIS, Stefano
14:15	[10] Development and system Tests of DC-DC converters for the CMS SLHC Tracker	KARPINSKI, Waclaw
14:30	[11] Embedded switched capacitors DC-DC	Mr. MEIER, Beat
14:45	[12] The serial Power interface chip	TRIMPL, Marcel
15:00	[14] Serial power circuitry in the ABC-Next and FE-I4 chips	DABROWSKI, Wladyslaw
15:20	[16] Discussion	

Paris agenda

Parallel Session B4 - Power, Grounding and Shielding (15:00-15:50)

- **Conveners: Farthouat, Philippe**

time	title	presenter
15:00	Progress on DC-DC converters for SiTracker for SLHC	DHAWAN, Satish
15:25	ASIC buck converter prototypes for LHC upgrades	MICHELIS, Stefano

Parallel Session B4 - Power, Grounding and Shielding (16:15-17:55)

- **Conveners: Godinec, Allain**

time	title	presenter
16:15	Experimental studies towards a DC-DC conversion powering scheme for the CMS silicon strip tracker at SLHC	KLEIN, Katja
16:40	System Integration Issues of DC to DC converters in the sLHC Trackers	BLANCHOT, Georges
17:05	Performance and comparison of custom serial powering regulators and architectures for SLHC silicon trackers	TIC, Tomas

Power WG (17:55-19:30)

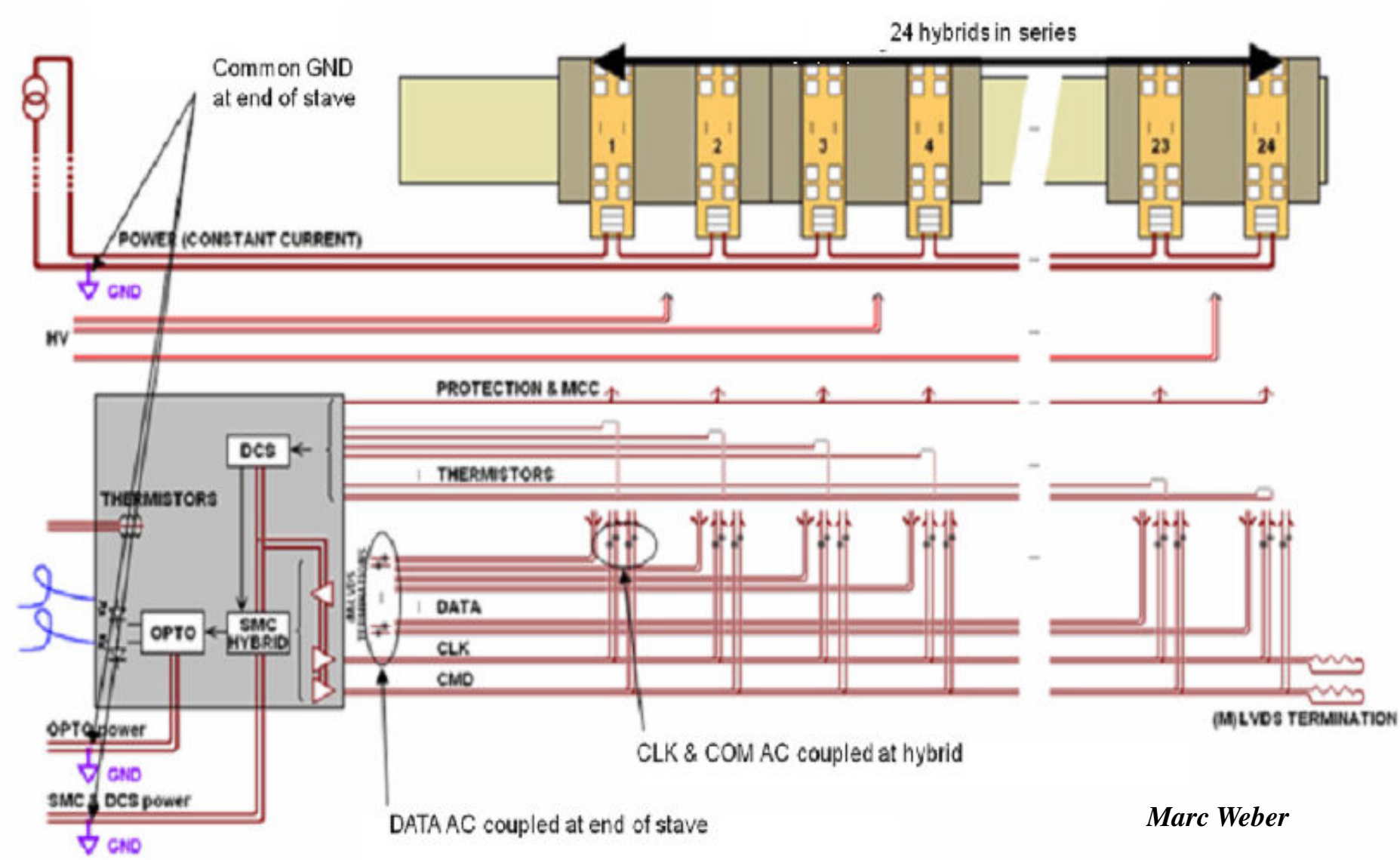
- **Conveners: Farthouat, Philippe**

time	title	presenter
18:00	SPI test results	HOLT, Richard Philip
18:15	Irradiation results of technologies for a custom DCDC converter	FACCIO, Federico
18:30	EMC issues for CMS Tracker Upgrade	ARTECHE, Fernando
18:45	Roadmap for serial powering	WEBER, Marc
19:00	Roadmap for DC-DC	FACCIO, Federico
19:15	Discussion	

Main activities

- Serial power
  - Three options for implementations
- DC-DC converters
  - Study of commercial converters
  - Development of a radiation hard DC-DC
- ATLAS
  - No decision taken yet wrt final implementation
  - A lot of activity in serial power
- CMS
  - DC-DC selected as the baseline solution
  - Serial power as a back-up

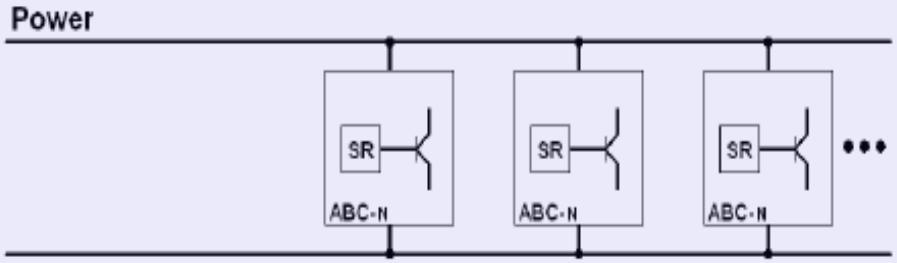
Serial Power



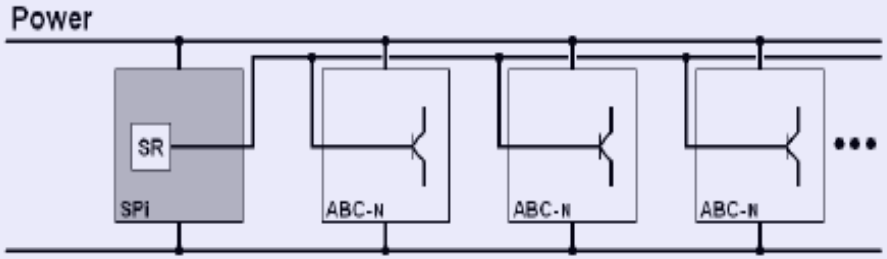
Marc Weber

Serial power: shunt location

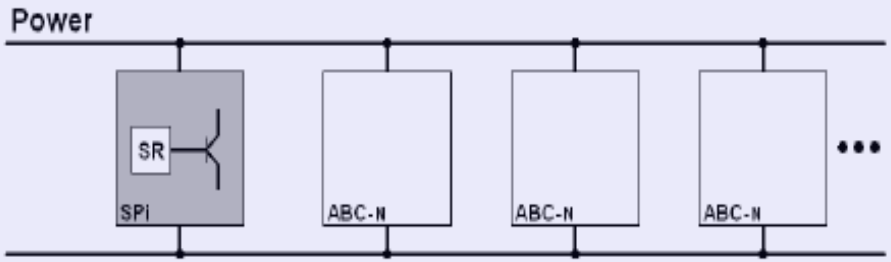
- **"W" scheme**
  - Use each ABCN's integrated shunt regulator
  - Use each ABCN's integrated shunt transistor(s)



- **"M" scheme with SPI**
  - Use one external shunt regulator
  - Use each ABCN's integrated shunt transistor(s)
    - Two (redundant) shunt transistors, 140mA each



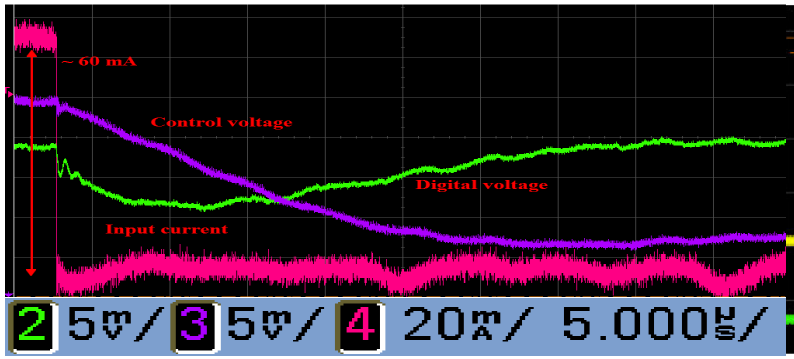
- **External SPI scheme**
  - Use one external shunt regulator
  - Use one external power transistor

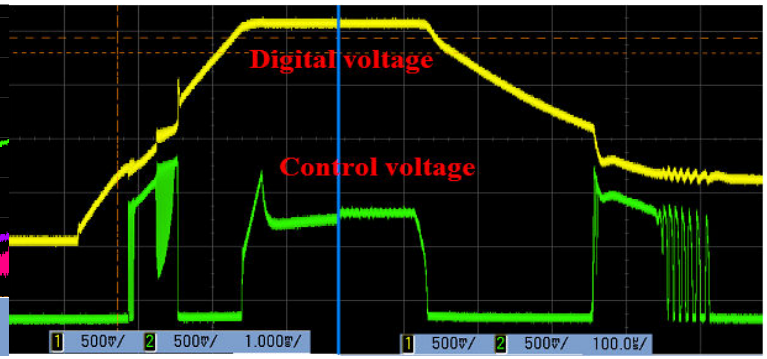


- Studies of the three schemes presented

Tomas Tic

Distributed Shunts

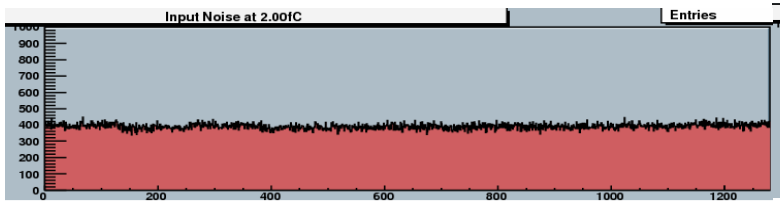


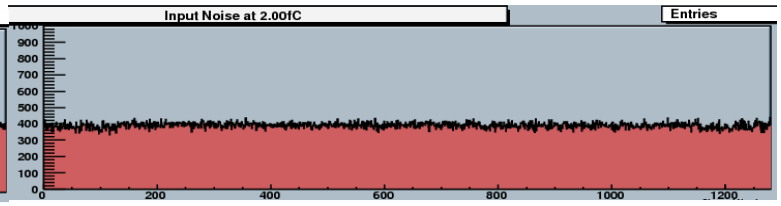


Response to a step in current Start-up and shut-down

- The transient response to a step in current is superior
- The start-up is without difficulty
- ENC is as simulated and same as for independent powering scheme

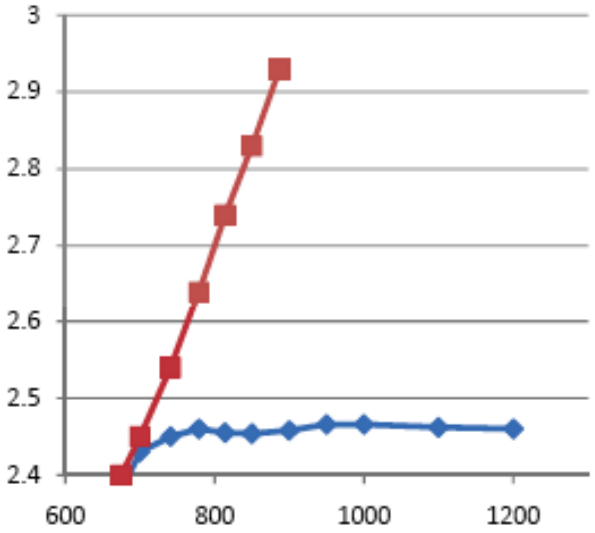
Tomas Tic

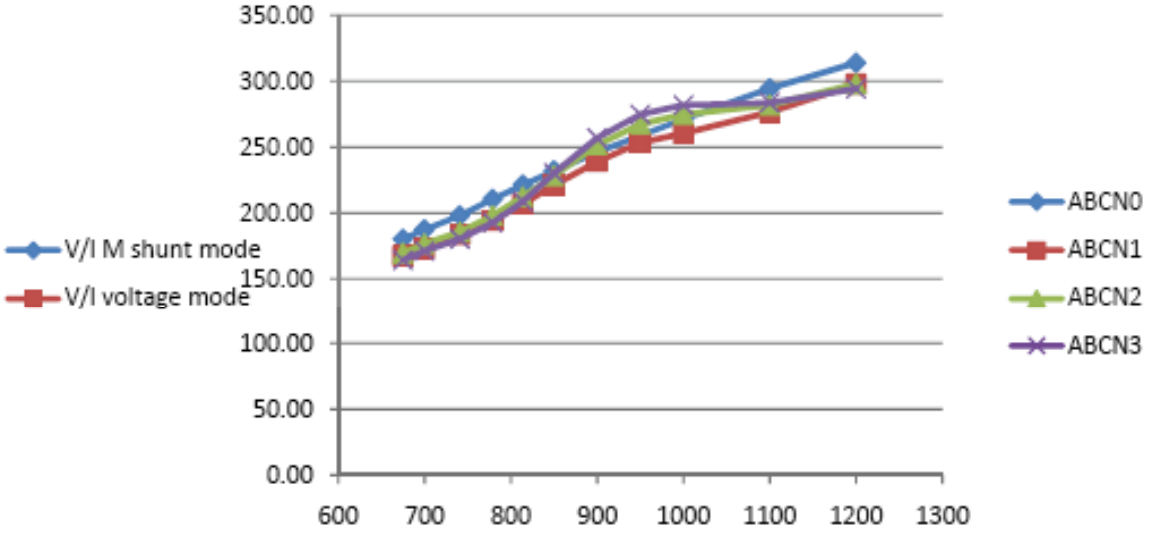




- M version working well
- Tested on an ATLAS hybrid (20 ABCnext chips)

Distributed shunts





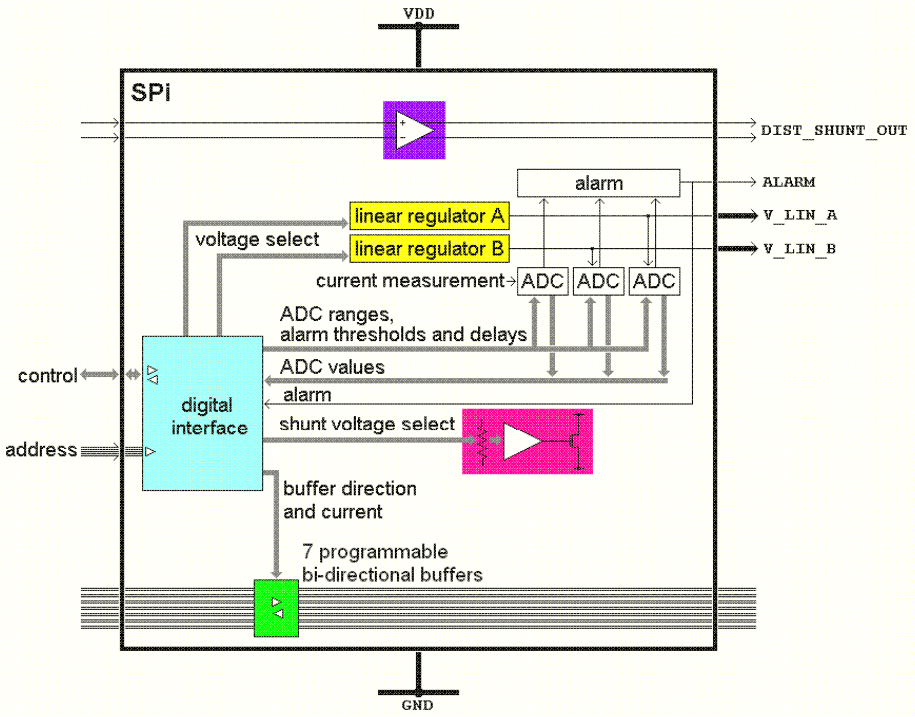
- Shunt regulation and distribution of current per chip

SPI Chip

SPi offers…

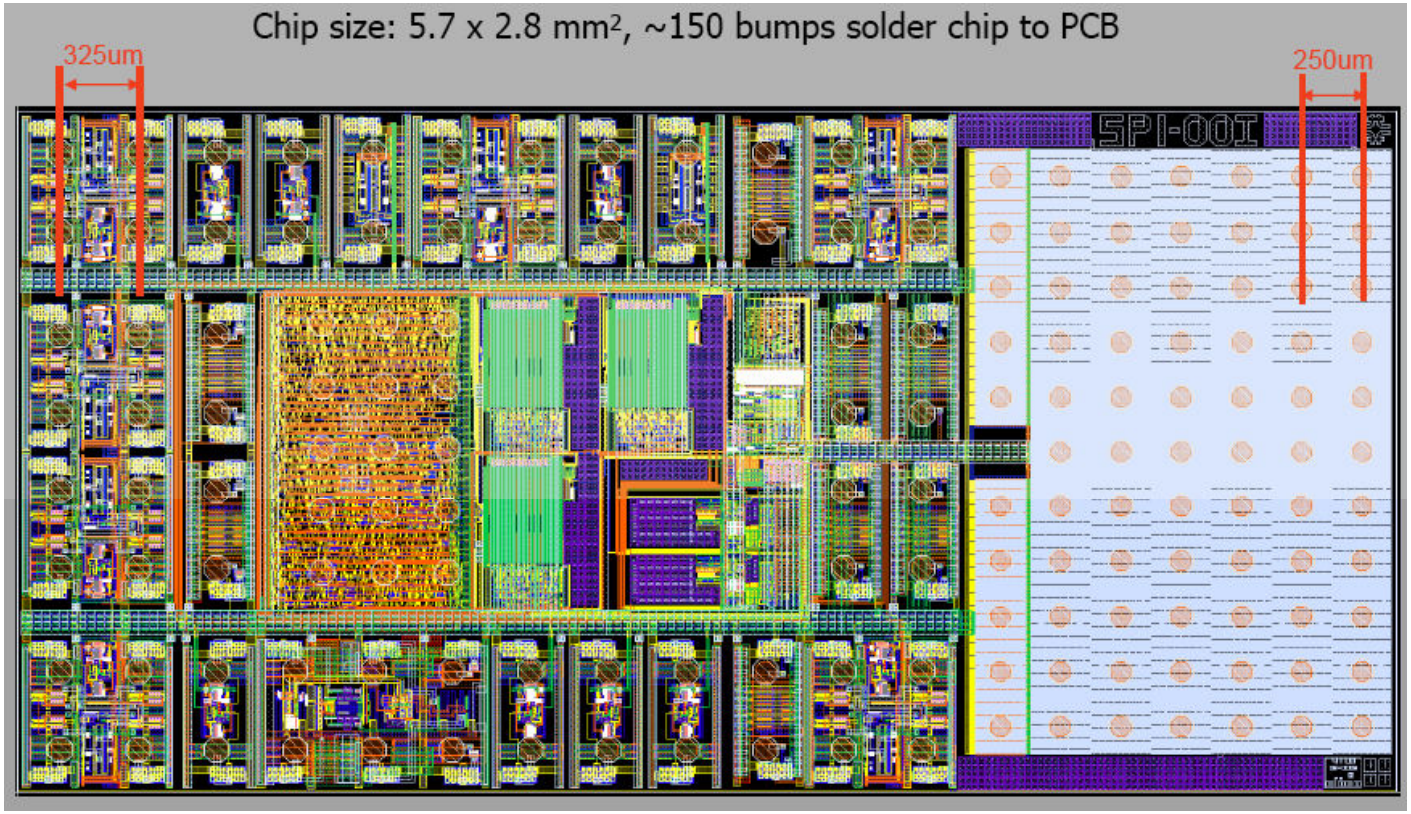
- Shunt regulator schemes
- Data communication
- Power management
- Monitoring/alarms

Designed by
Marcel Trimpl (FNAL)
And
Mitch Newcomer (U Penn)



Richard Holt

SPI chip



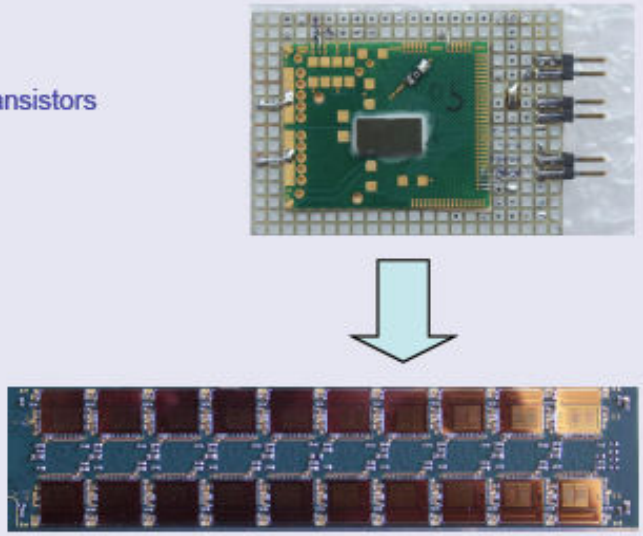
- Fully tested and available
- Will be used to test serial power on an ATLAS stave prototype
  - 24 hybrids of 20 ABCnext

SPI tests with an hybrid

Richard Holt – Rutherford Appleton Laboratory
SPi test results
September 2009

SPi with a hybrid

- **Shunt regulator schemes**
  - √ ABCN with SPi internal shunt regulator
  - √ ABCN with SPi controlling distributed shunt transistors
- **Data communication**
  - √ Data has passed through SPi
- **Power management**
  - √ Shunt current monitoring
  - √ Shunt regulator voltage setting
  - √ Linear regulators voltage setting
  - √ Alarm



√ = tested and working Documentation is available to users

Science & Technology Facilities Council

Serial power: roadmap

- Marc Weber summarised the progress made with serial power components and testing
- Moving from 250nm to 130nm or lower technologies implies some changes
  - Analog power is not dominated anymore
  - Optimised power consumption if shunt regulators distribute the digital Vdd and if step-up switched capacitors DC-DC are included in the FE chips to deliver the analog power
- Prototyping of blocks could start in 130nm
- Very optimistic for the future and had a lot of fun working in the field

DC-DC converters

- Three main activities
  - EMC studies at the level of the system (Aragon)
  - Studies with commercial components (Aachen and Yale)
    - Radiation tolerance
    - EMC issues
  - Development of a radiation hard custom device (CERN)
    - Chip development
    - Technology qualification

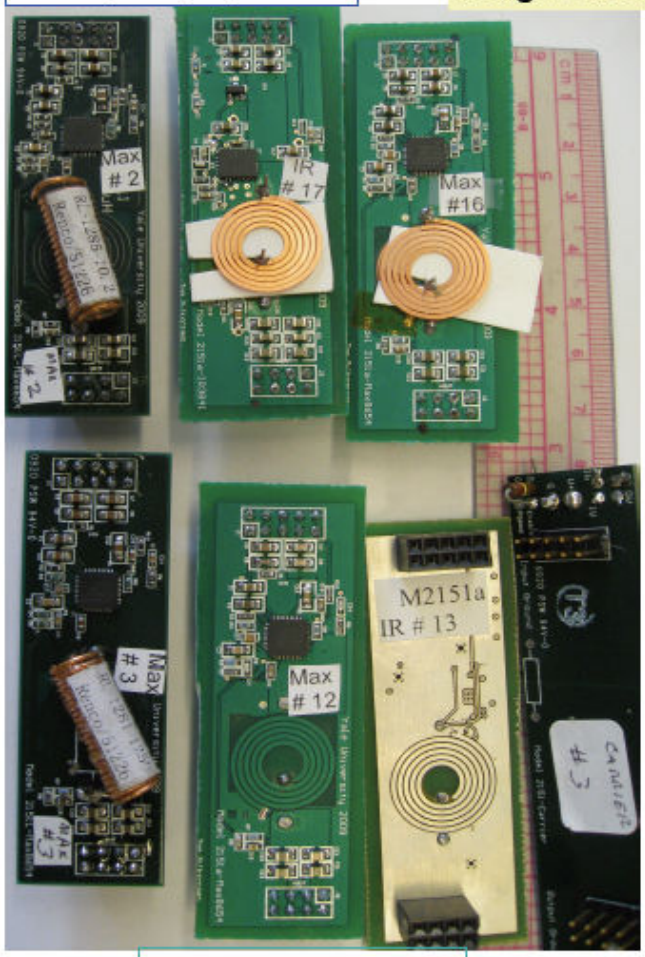
Commercial components(Yale)

- Satish presented irradiation tests of several commercial devices
- Optimistic that some components can be radiation hard enough
- Several devices tested with some ATLAS hybrids
  - No excess of noise

Commercial components (Yale)

Monolithic: 14V, 8A, 1.2MHz
Multichip: 16V, 8A, 1.5MHz

Plug In Card: DC-DC Powering



Yale Model 2151a

2 Different ICs
3 Different Coils

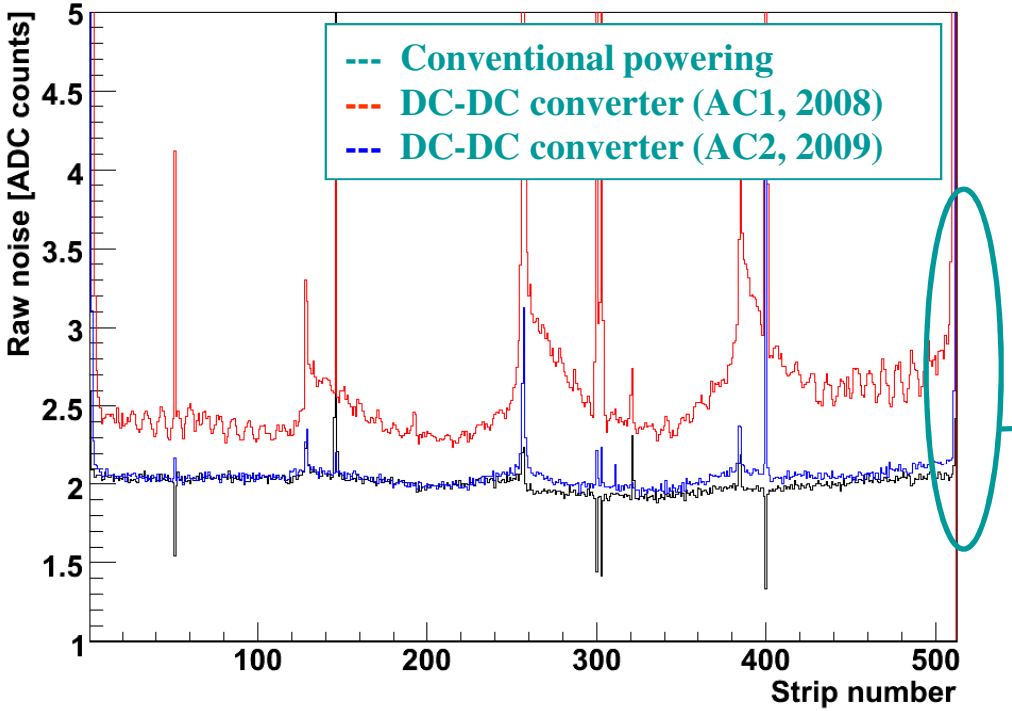
Coil	Board #	Common Mode Choke	Power To Dc_DC	Input Noise Electrons rms
Solenoid	Max # 2	No		881
"	"	"		885
Copper Coil	IR # 17	No	Switching	666
"	"	Yes	"	634
"	"	Yes	Linear	664
Embedded	Max 12	No	Linear	686
"	"	Yes	"	641
	Tests @ Liverpool Sept 17,09		All Channels Trimmed	
"	"	Yes	"	648

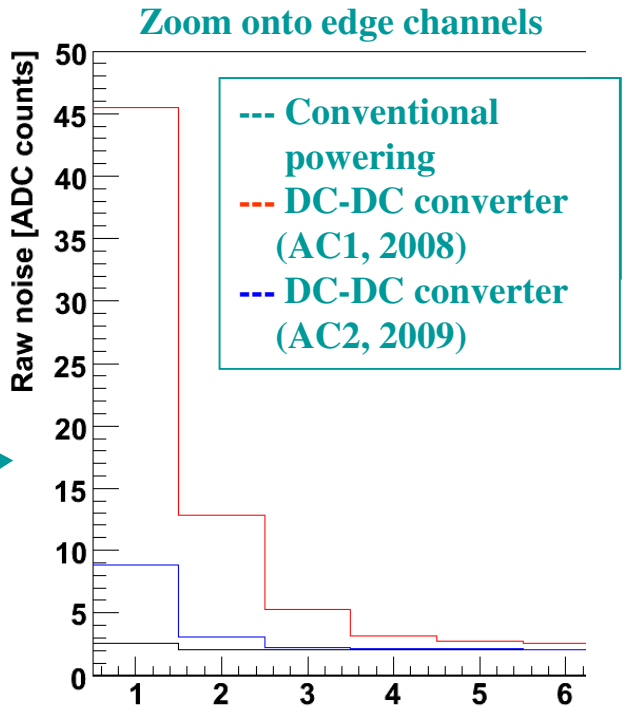
Embedded 3 oz Cu
Etched Cu Foils 0.25 mm
Solenoid without Ferrite

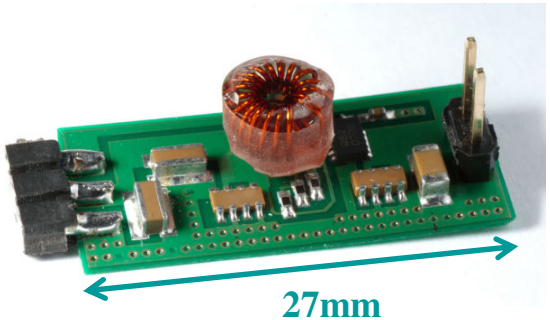
Commercial components (Aachen)

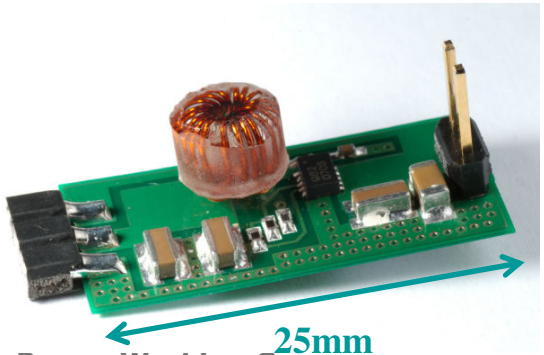
- Katja Klein reminded us that the CMS baseline choice is DC-DC
  - Serial power as a back-up
- Aachen developed several version of DC-DC made with commercial devices to study and understand EMC problems

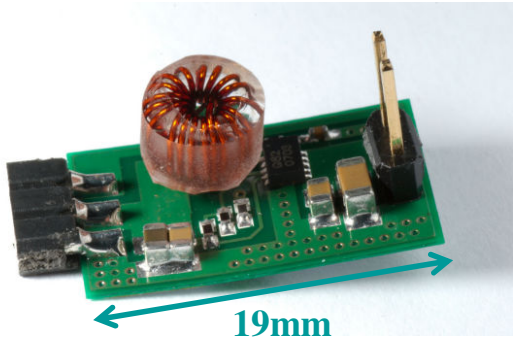
Commercial components (Aachen)



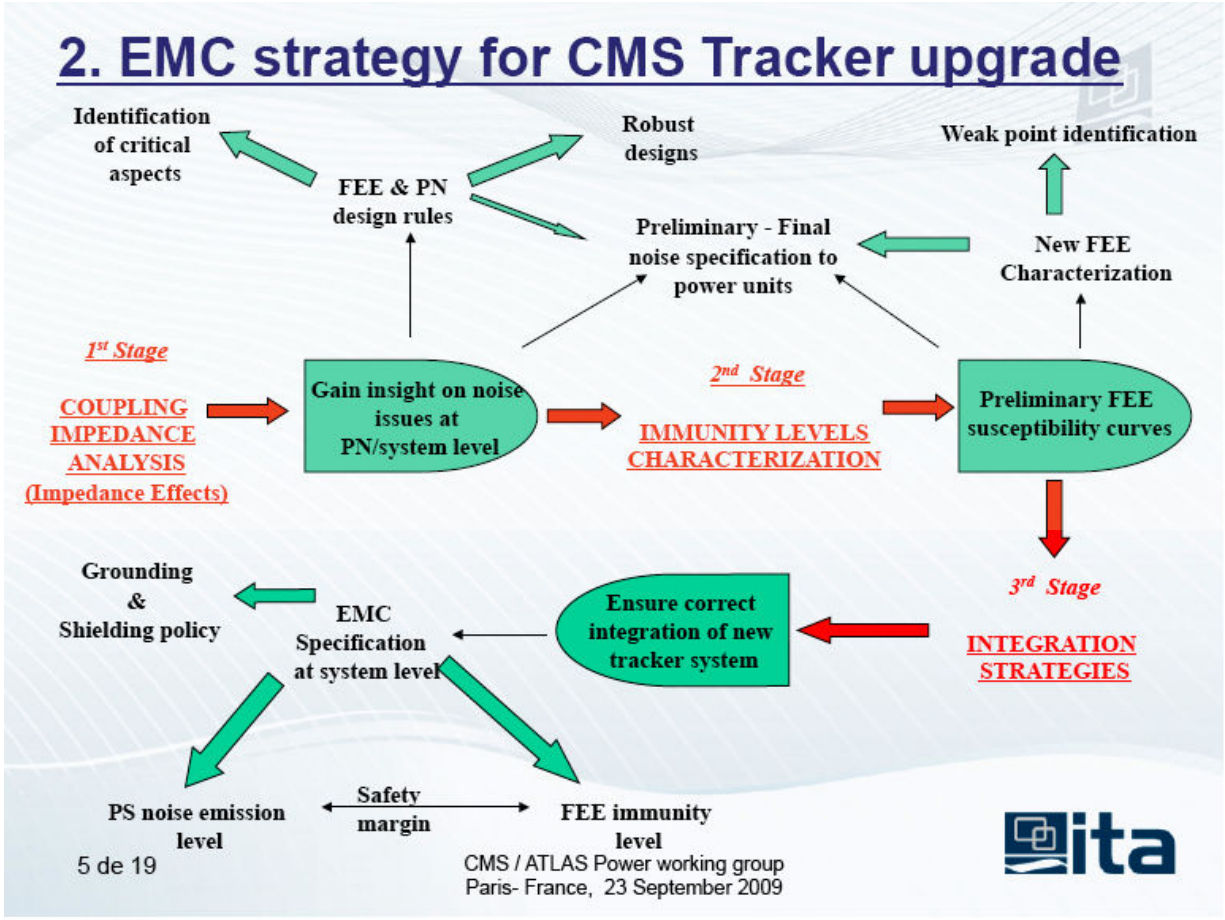








EMC issues for Tracker upgrade



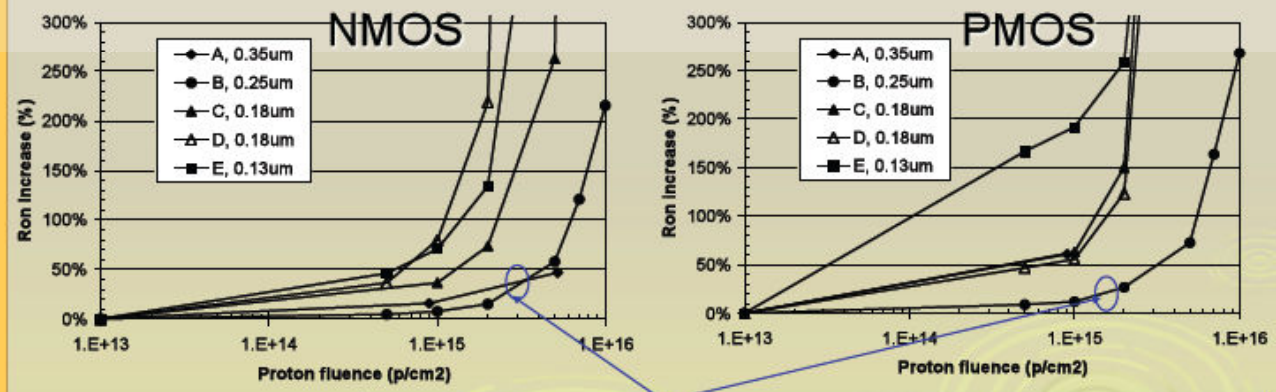
- Fernando Arteche presented a project submitted to CMS in view of dealing properly and early enough with EMC issues

Development of a radiation hard DC-DC

- Identification of suitable technologies
  - Radiation hardness
- Development of an ASIC
- Development of a full DC-DC converter with this ASIC
  - Studies of different air-core inductors
  - Studies of different lay-out

Displacement damage (3)

- On-resistance increase for all technologies (LDMOS)



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- Federico Faccio presented the effect of radiations on different technologies

Radiation issues

Conclusion

- Systematic measurements of TID and displacement damage in high-V transistors in 5 technologies have been made
- TID: results comparable to low-V CMOS
  - Leakage current not directly correlated with technology node, gate oxide thickness, V rating
- Displacement damage: strong effect on channel resistance at large integrated fluence
  - Very different sensitivity in the 5 technologies
- HBD techniques successfully applied
  - They decrease the TID-induced leakage
  - BUT they might have an impact on the high-V capability
- Best technology satisfying our requirements (250Mrd, $2 \cdot 10^{15}$ n/cm^2) is the 0.25um
  - Design of prototypes on-going
- Backup technology is the 0.35um
  - Very good prototype already exists and has been irradiated successfully
  - The design could be completed with relatively small effort (backup)
- We need a more precise requirement on the radiation tolerance!

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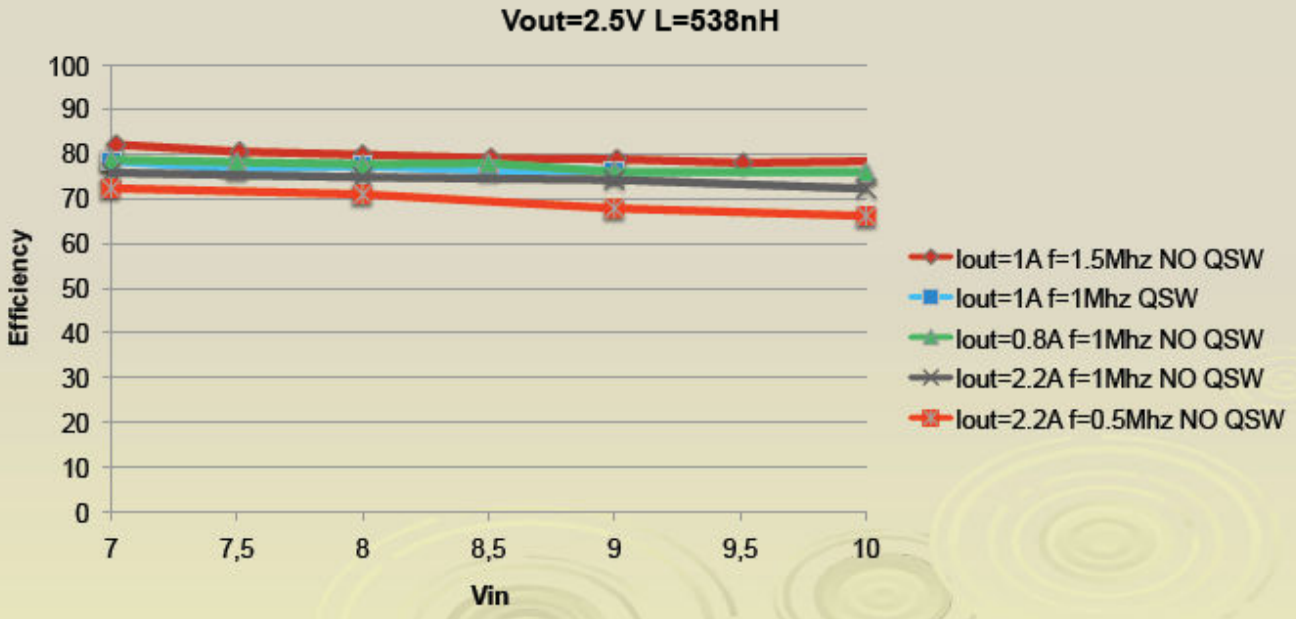
- Very promising results as two technologies seem usable
- SEU still to be measured

Development of a custom ASIC

- Stefano Michelis presented the development of three ASICs
  - Two in 0.35µ technology (tested): AMIS1 and 2
  - One in 0.25µ technology (back from foundry this week)
- Satisfactory results with AMIS2 in terms of efficiency and radiation hardness
  - Although the transistors are not the most hard, the efficiency drops of less than 10% after the total expected dose
  - Efficiency limited by bonding wires resistance

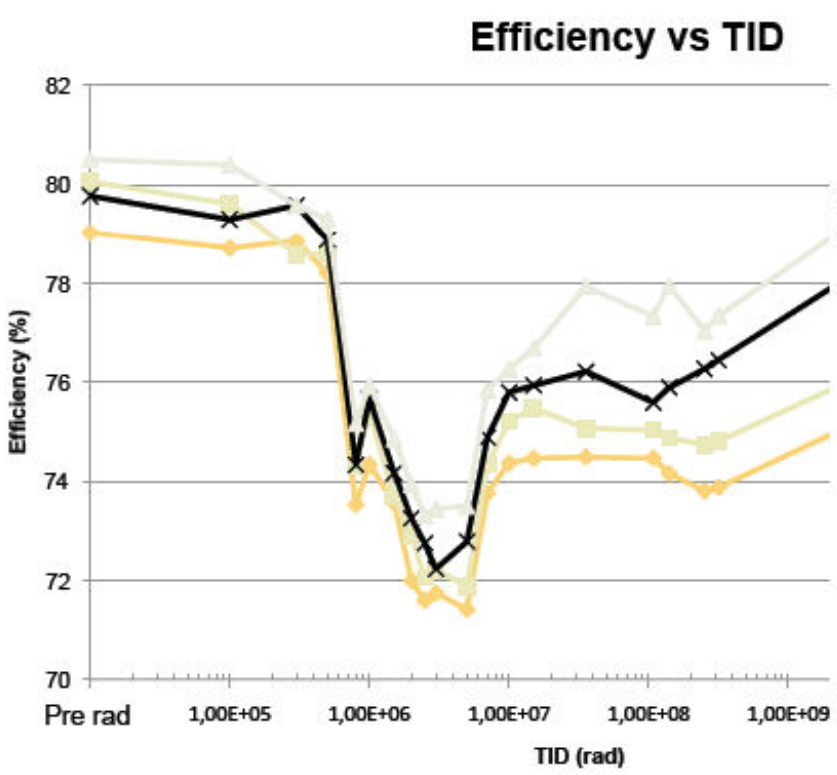
AMIS2 efficiency

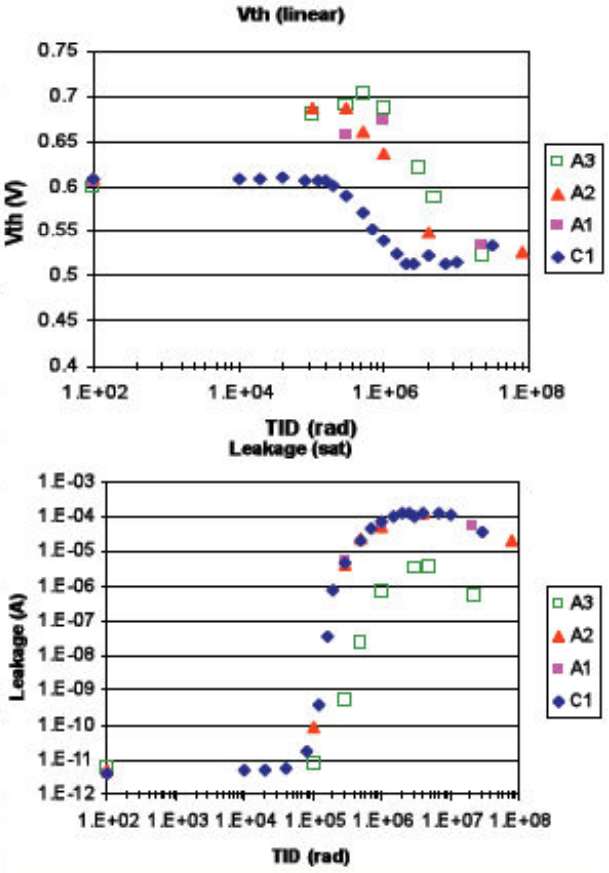
- The measured efficiency goes up to 82%, depending on load current and frequency.
- Conductive losses are the major contribution of inefficiency.
- Resistance along the current path is much higher than the one expected for the power transistors alone. This might be due to on-chip routing, bondings and package.



AMIS2 Radiation results

The X-ray radiation tests shows a decrease of the efficiency mostly due to the radiation induced leakage current , compensated by the threshold voltage shift.



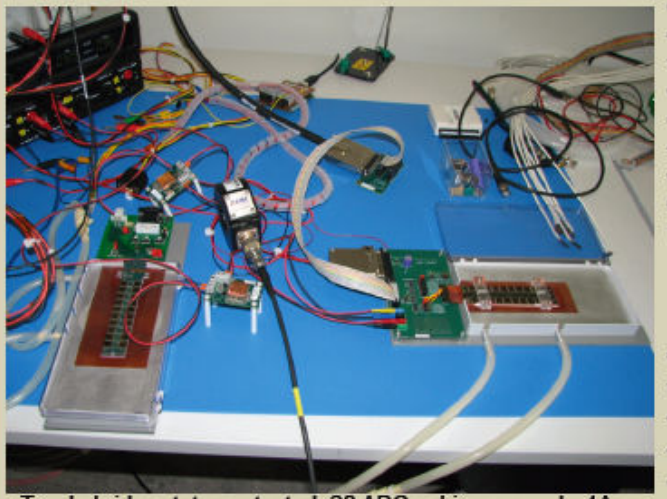


Twepp09, Paris

S.Michelis CERN/PH

Tests with ATLAS modules

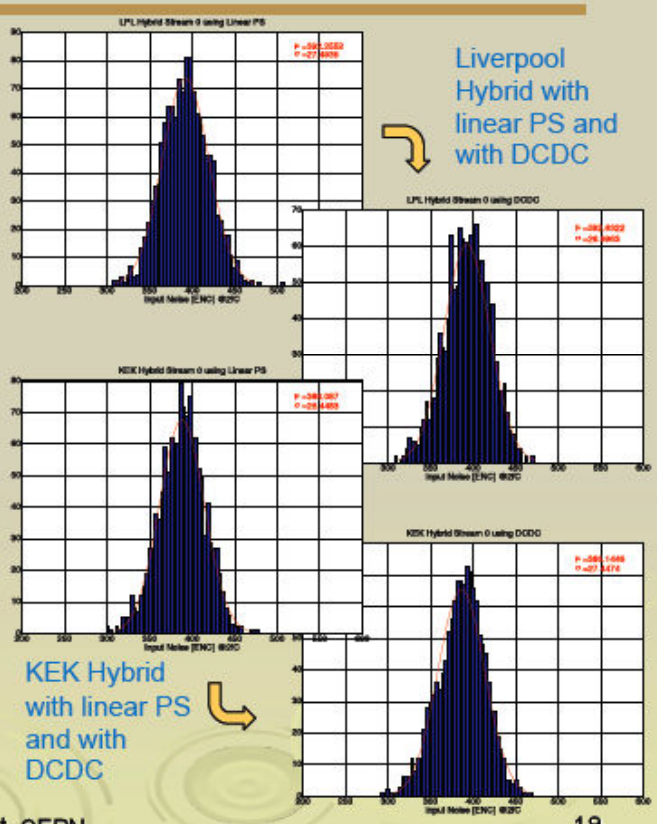
Tests with ABCn w/o strips



Two hybrid prototypes tested, 20 ABCn chips on each, 4A DC, without strips detector mounted:

- Liverpool Hybrid, requires one DCDC or linear PS.
- KEK Hybrids, requires two DCDC or linear PS.
- Noise estimation: Qe*(RMS of fitted scurves)/Gain [ENC].

No noise degradation observed when using the DCDC, even when powering the analog part directly from DCDC (KEK case).



Liverpool Hybrid with linear PS and with DCDC

KEK Hybrid with linear PS and with DCDC

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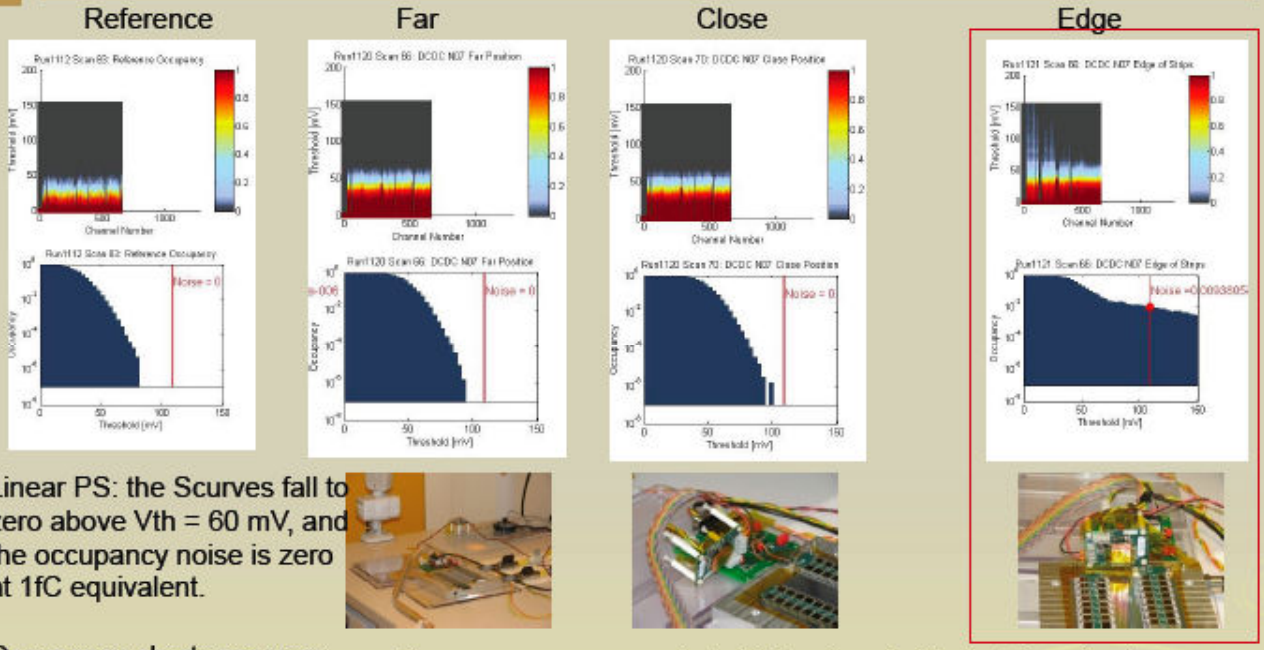
- No excess of noise with two types of hybrids

- Georges Blanchot presented the EMC measurements made with a complete DC-DC made with the custom chips

Tests with ATLAS modules

Tests with ABCn with strips



Linear PS: the Scurves fall to zero above Vth = 60 mV, and the occupancy noise is zero at 1fC equivalent.

Occupancy charts are very sensitive to dead or unstable channels.

The occupancy expands to higher thresholds, but the effect becomes critical only if the coil is facing the strips.

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- Some excess of noise in some channels when the converter is close to the module

- Requires more detailed work but suspicion that there is some coupling through the closed bonding wires

DC-DC roadmap

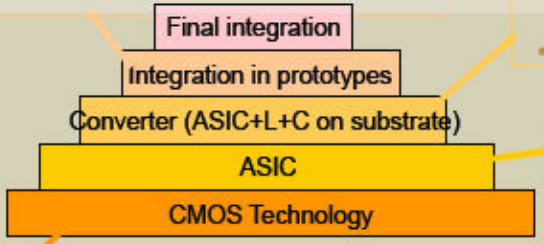
- Federico Faccio summarised the last year work
  - Several technologies tested against radiation
    - Two valid candidates
  - Second prototype in 0.35µ and new prototype in very promising 0.25µ
  - Full DC-DC modules constructed and very good measurements with existing modules and hybrids
    - Radiated noise still to be optimised

DC-DC work program

What needs to be done

- Analyse noise coupling mechanisms
  - On existing systems
  - On new hybrid prototypes
- Study system-level stability
  - DCDC is seen as negative load
  - Drive requirements for the power supplies
- Slowly define requirements for the final integration

- Progress in miniaturization
- Understand noise consequences of design choices (size, position of capacitors, filters)
- Define appropriate value of L
  - Understand limit of PCB technology
  - Explore in depth the possibility to use a custom wrapped L (material, size, cost, shielding)
- Decide a shielding strategy



- Strenghten link with manufacturer
- Measure sensitivity of power transistors to Single Event Effects (SEB, SEGR). With this measurement, the safe operation area can be defined (Vds)
- Monitor regularly the radiation tolerance to verify it
- Keep second source

- Fully test first prototype in chosen 0.25um technology. Verify efficiency gain with special dead time handling
- Integrate additional functions
  - Vbgp, Regulators, Overl protection
  - OverV and overT protection
  - Protection against SEUs
- Choose and prototype appropriate packaging (flip-chip)
- Keep backup ready (AMIS2)

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- CMS willing to use such converters for their phase 1 pixel upgrade

Conclusion (1)

- The two options have made impressive progress during the past year
- Still some work to be done for both to implement all the necessary tools for a safe use on detector
  - Switching on-off
  - Protection
- Both solutions must be validated on a reasonably large scale device
  - The 1.2m long double sided ATLAS stave prototype would be a good test vehicule
- ATLAS will have to select a solution after that stage
  - Performance
  - System issues
  - …

Conclusion (2)

- The working group as a place for information exchange is very useful
  - Having them during larger events (TWEPP or ACES) has interest but we are missing time for discussion
- Necessary to organise a 1-day separate workshop
  - Date to be defined but could be as soon as new relevants results are available
    - Test of an ATLAS stavelet
    - Test of the DC-DC in 0.25