TWEPP-09 Executive Summary

J. Christiansen [a], P. Farthouat [a], A. Gonidec [a], G. Hall [b], M. Hansen [a], K. Kloukinas [a], A. Marchioro [a], L. Musa [a], J. Oliver [c], E. Petrolo [d], W. Smith [e], C. De La Taille [f], F. Vasey [a], T. Wijnands [a], K. Wyllie [a], R. Yarema [g]

[a] CERN, 1211 Geneva 23, Switzerland
[b] Imperial College, London, United Kingdom
[c] Harvard University, Cambridge, USA
[d] INFN, Rome, Italy
[e] University of Wisconsin, Madison, USA
[f] Laboratoire de l'Accélérateur Linéaire, Orsay, France
[g] Fermilab, Batavia, USA

I. Some Statistics

The Topical Workshop on Electronics for Particle Physics (TWEPP-09) took place in Paris, France, from 21 to 25 September 2009. Fourteen invited and 131 contributed papers (63 oral and 68 poster) were presented in 10 plenary and 11 parallel sessions to an audience of approximately 240 participants. Twenty-six of these participants came from the United States and five from Japan, while the majority originated from Europe. Of all presented papers, 25% referred to the LHC project, 43% to the SLHC upgrade programme, and 32% to ILC and other experiments.

II. Session Summaries

Some of the main conclusions from the sessions dedicated to ASICs (A), Packaging and Interconnects (B), Optoelectronics (C), Systems Installation and Commissioning (D), Radiation tolerant components and systems (E), Power (F) Trigger (G), Programmable logic, boards, crates and systems (H) and Posters (I) are summarized in sections A to I below. Owing to space constraints, many contributions had to be omitted from this summary, but the interested reader can find them all at [1].

Invited presentations during the Monday afternoon opening session surveyed the High Energy Physics (HEP) activities of CNRS-IN2P3 & IRFU in France, their microelectronics activities, and the research programme at the Pierre et Marie Curie University (the workshop host). In the second part of the opening session, three major High Energy Physics programmes were reviewed: the LHC programme at CERN, the next generation HEP experiments in Japan, and the ILC-CLIC development challenges.

On the following days, all sessions were introduced by invited plenary talks, as mentioned in the sections below.

A. ASICs

The ASICs sessions were particularly well attended this year, with a very high number of good paper submissions and large turnout. The community is clearly vigorously restarting an R&D phase for chips to be used in future detectors and this was reflected by the large variety of projects presented.

The sessions consisted of 18 oral presentations and two invited talks. The first invited speaker addressed some of the most important issues of designing analog circuits using sub 100 nm technologies. While providing continuous advantages and benefits for digital designers, mainly in terms of size and energy consumption per logic function, these new technologies are not always well received by analog designers due to at least three factors:

- reduced power supplies for deep submicron technologies lead to small signal swing ranges and reduced biasing possibilities;
- process variations at very small size are becoming more important (due to atomic effects) and affect the matching of devices;
- intrinsic transistor gains are becoming significantly worse than with older technologies requiring very tricky solutions to be introduced.

Some interesting and innovative solutions relevant for HEP applications were proposed, often resorting to new circuit topologies and application of digital correction techniques.

The second invited talk covered the very critical issue of low power design for System-On-Chip solutions. With the explosion of the market of portable and battery operated electronic devices, this is perhaps the most important subject in today's large commercial projects. While it becomes easier to add functionality and computational power to large chips (think about the various multi-core processors or very large DSP chips), doing this within an acceptable power budget becomes the overwhelming preoccupation of designers. System architects are using tricks and optimization

techniques at different abstraction levels to contain power dissipation, and have to be knowledgeable and master complexity at all these different levels, from the simple transistor leakage to the interaction and parallelism of many functional units. Some of these techniques are very relevant and educative for designers in HEP, where the development of electronics for future detectors (see for instance the new intelligent trackers or very high granularity calorimeters being discussed in HEP) depends sometimes critically on the capacity of designers to come out with solutions that remain within an acceptable overall power budget.

The Tuesday morning ASICs session was dedicated to pixel electronics and imagers.

Two talks addressed Monolithic Active Pixels (MAPs) which have now reached a very mature state as shown by their use in EUDET telescope or in the vertexing of physics experiments. The large area (2 cm^2) obtained with MIMOSA26 together with zero-suppressed and high speed digital readout illustrate this maturity. The progress in technology with deep P-wells also allows more sophisticated MAPS readout (including the use of PMOS transistors without degrading the collection efficiency) as shown in the FORTIS chip or the TPAC (Tera Pixel Active Calorimeter for the ILC). The SOI process can also be considered as a monolithic pixel sensor, although the charge is not collected by diffusion but in a depleted junction made possible by the process. KEK has been providing MPW access to the OKI 0.2 μm process, which has been further improved to minimize back gate effects. Finally, a fourth type of monolithic pixel sensor is the TFA (thin film on ASIC) proposal, depositing amorphous silicon on the readout chip to form the sensor. The very small signal amplitude necessitates ultra low noise readout which has been designed and tested successfully. The detector leakage current still makes it difficult to clearly identify the MIP.

Hybrid pixel electronics was addressed in two talks. One was dedicated to the PANDA experiment at GSI, where the high rate and lack of trigger necessitate custom developments in 130 nm technology exploiting Time over Threshold information. At the LHC, ABCN, the next generation ABCD chip for ATLAS strip readout has been evaluated. The results presented focused on system aspects to reduce the power dissipated, such as allowing internal serial powering and reducing the digital power.

The Tuesday afternoon ASICs session had presentations on chips for gas-detectors and calorimeters and was followed by a Microelectronics Users Group meeting (MUG) (see the MUG report at the end of this section).

A new 130 nm CMOS pixel chip for micro-pattern gas-detectors was presented. As with several other chips, this was not just a new front-end ASIC, but more functionality was included by incorporating an on-pixel TDC. The on-pixel TDC is capable of doing time measurements already in the pixel element. This functionality was made possible by the higher integration capability of deep submicron technologies.

The electronics being designed for the very high granularity calorimeters at the ILC takes advantage of the particular bunch crossing structure of that machine and relies on powering schemes where the FE electronics is actually turned on with a very low duty cycle. Owing to the demand on dynamic range for these calorimeters, designers find it easier to work with technologies allowing a relatively large power supply voltage and several chips are therefore being developed in a 0.35 μm BiCMOS technology. As an example, the HARDROC ASIC is designed for a very high granularity calorimeter readout where the detector is not only capable of doing energy measurements but also has some fine-granularity capability sufficient to explore the concept of particle-flow in these future calorimeters.

ILC calorimeters also rely on very accurate calibration circuitry, typically requiring high precision DACs. Such a component was presented, also developed in a 0.35 μm process to take advantage of the higher signal voltage swing allowed in this technology.

A more advanced, medium performance 130 nm BiCMOS technology with SiGe transistors was instead used for an upgrade of the ATLAS LAr calorimeter front-end with again the possibility of using large swing signals and relatively large supply voltages. Preliminary measurements on the test chips indicate nice functionality and good matching with the simulation, reassuring us that using a high volume, mature technology is always an extra guarantee of success for all designs.

The Thursday ASICs session hosted several talks about chips designed for neutrino experiments: analog memories, combining different record lengths and speeds for optimum signal analysis and realized in AMS 0.35 μm; a centralized multichannel readout chip PARISROC designed in 0.35 μm SiGe that autotriggers and digitizes both charge and time information to a data-driven readout system; an analog-to-digital converter to be integrated in a readout chip (a low power current driven architecture reaching 10 bits at 25 Ms/s showed good preliminary results and can be used for PET readout systems); and a new high precision and large dynamic range Time-to-digital converter designed in 0.35 μm CMOS.

An exploratory new detector type using an intrinsic weakness of conventional circuits (latchup sensitivity due to parasitic SCR structures) was presented. A simple working test circuit was realized with conventional discrete components while more work will be necessary to realize a working integrated version.

Finally, two chips belonging to the family of components for the GigaBit Transceiver (GBT) system were also presented. A promising prototype of a laser driver optimized for the opto-components specified by the Versatile Link and GBT Projects was designed in 130 nm. This component does not yet fully satisfy the timing specifications, but was functionally fully working. The corresponding receiver component (a transimpedance amplifier to be connected to the receiving pin-diode) was presented; measurements of the prototype devices with real opto-receivers were shown to be fully satisfactory and the designers expressed confidence that the final iteration will contain all functionality that was omitted in this version and will completely qualify the components for the desired system specification.

The Microelectronic User Group (MUG) meeting consisted of three short presentations followed by an open discussion session. The opening presentation summarized the design tools and foundry access services that CERN provides to the HEP electronics designers community. CERN currently supports two technology nodes, a 130 nm node for CMOS and BiCMOS circuits and a CMOS 90 nm node. To increase the design productivity with the 130 nm node, CERN took the initiative of developing a Mixed Signal Design Kit by incorporating the foundry Physical Design Kit (PDK) along with foundry proprietary Digital Standard Cell libraries. The Design Kit supports the new Cadence CAE tools based on the Virtuoso IC6.1 OA (Open Access) and the SOC Encounter 7.1 OA platforms. A significant part of the development work for the Design Kit was subcontracted.

To enhance the functionality of the 130 nm Mixed Signal design kit, a set of customized Methodology Design Workflows were developed. These flows demonstrate the use of the CAE tools and the procedural steps involved in accomplishing specific design tasks aiming to provide standardized design workflows for partners collaborating in common design projects. CERN has organized three training workshop sessions, until the end of 2009, where these Methodology Workflows will be demonstrated. There are also plans to organize more sessions in early 2010 based on the demand.

CERN is providing the HEP community with foundry access services for design prototyping and production runs either directly with the foundry or through the MOSIS MPW service provider. During the period of 2008–2009 there were five MPW runs organized on the 130 nm CMOS8RF node, one MPW run on the 130 nm BiCMOS (SiGe) node and one MPW run on the 90 nm CMOS9LP/RF node. The majority of the designs were fabricated on the 130 nm CMOS node, having 20 designs with a total silicon area of 100 mm^2.

The second presentation was an invited talk on Mixed-Signal Challenges and Solutions for advanced process nodes. The presentation addressed the implementation and verification challenges for mixed signal designs in deep submicron technologies and the impact on the engineering cost of the product. Modern CAE tools solutions were presented, based on the increased interoperability of the front-end (analog full custom) design flow with the back-end (digital) design flow.

The third presentation was a demonstration of the Digital Block Implementation Methodology Workflow based on a digital design example. This workflow is part of the 130 nm Mixed Signal Design Kit and is extensively automated through the use of scripts. All design steps were demonstrated, starting from RTL code synthesis, floor planning, placement, routing, clock-tree generation, timing optimization, timing verification, and physical design verification.

During the open discussion session, technical issues concerning the technical capabilities of the newly developed CMOS 130 nm Mixed Signal design Kit were addressed and organizational issues about the distribution of the kit and the training workshops were discussed. The organization of MUG meetings, outside the context of the TWEPP workshops was suggested. Regular MUG meetings of one or two days duration would provide more effective means for exchanging technical information and experience for the use of new technologies and design techniques within the community and allow designers to stay up to date with ongoing developments.

B. Packaging and Interconnects

Packaging and interconnect technologies are receiving increased attention by the detector and electronics community, as vital and critical contributors to future high-resolution low-mass tracking detectors. The appropriate technologies must offer high interconnect density, low mass, high yield and high reliability at an affordable cost. The silicon detectors (strips and pixels) must be connected to readout chips mounted on appropriate hybrids/modules and must finally be integrated into complex tracker systems with optimally engineered power distribution and cooling systems. The papers presented in this session can be classified in three basic categories:

– Silicon strip detectors with front-end chips mounted on hybrids connected with wire-bonding;
– Interconnects for hybrid pixel detectors;
– 3D interconnect schemes for pixel detectors.

Across these three categories the challenges of using thinned readout chips and detectors plus very light support structures and services (power, cooling) to minimize material are being actively addressed.

Two presentations on silicon strip detectors reported the use of a flex Kapton hybrid technology,

as it offers the required interconnectivity with relatively low mass. Experience from current tracker systems has clearly shown that a significant emphasis needs to be put on manufacturability and reliability of such hybrids to enable large-scale trackers to be produced. Wire bonding between the detector and the readout chip and to the hybrids is extensively used. This is a well known technology with wide experience in the community which covers well the needs of silicon strip detectors. For the ATLAS silicon strip detector upgrade the approach taken is to minimize the actual connections through the hybrid itself. The readout chips are directly connected to the single-sided silicon strip detectors with staggered wire-bonding (without pitch adapters) and readout and control signals are whenever possible connected directly between neighbouring readout chips (20 per hybrid). The complexity of the hybrid itself is thereby significantly reduced (no need for very fine pitch connections and micro vias). The use of wire-bonding to connect the front-end hybrids to the long (1.2 m) power distribution and readout busses running along a detector stave with up to 24 readout hybrids is also being evaluated. The ORIGAMI concept for double-sided silicon strip detectors (BELLE experiment upgrade) uses folded flexible Kapton pitch/routing adaptors to connect strip signals from one side of the detector to a Kapton hybrid on the other side, thereby handling the full readout of both detector sides with a single active hybrid. This requires a complex and delicate mounting, gluing, and wire bonding process that has been demonstrated on prototypes using a well defined assembly sequence with dedicated and optimized tooling. For the ATLAS silicon strip detector upgrade the cooling of the front-end chips is assured through the silicon detector itself to a stave with integrated cooling pipes. The gluing of the hybrid on top of the silicon sensor and the cooling has been verified to work correctly when taking appropriate care of the isolation, shielding and gluing scheme. For the ORIGAMI approach a cooling scheme based on readout chips directly glued to a cooling pipe has shown encouraging results.

For hybrid pixel detectors the community is evaluating multiple fine pitch (< 50 μm) interconnect technologies available commercially or at experimental level (solder-based bump bonding, Solid Liquid Inter Diffusion (SLID), direct metal–metal thermocompression bonding). Such processes must be compatible with sensor and readout chip wafers coming from different manufacturers and their critical parameters are available pitch, yield, and total effective cost. The use of Through Silicon Vias (TSV), mainly based on the via last process, is also being evaluated to implement abuttable detector assemblies, making the I/O signals of the readout chips available on their back side. The use of the SLID connection scheme has shown very encouraging results for an ATLAS pixel upgrade application.

3D interconnect technologies, currently being intensively developed by the microelectronics industry, has received a lot of attention from the HEP pixel community as it can offer unique possibilities for highly integrated pixel detectors. The use of multiple levels of active CMOS layers (Tiers) allows novel pixel architectures to be implemented. Multiple tiers can, for instance, integrate more functions per pixel cell (for a given CMOS technology node) and the sensitive analog part can be implemented on a tier separate from the noisy digital logic. The close integration of the silicon detector and its readout electronics is also a possibility. A large number of groups (17) have joined in a 3D integration consortium to evaluate the possibilities and features of a commercially available 130 nm CMOS technology with via first TSVs and a tiers connection scheme based on direct metal–metal thermocompression bonding. A large number of different circuits have been submitted in a shared two tiers MPW submission using only one mask set. Pixel sensors for use with some of these circuits are also being prepared. The use of 3D integrated circuits bonded to MAPS detectors is also being evaluated by one institute. This large community is eagerly waiting to get its circuits back to make detailed performance, radiation tolerance, and yield analysis of this new 3D technology. Appropriate CAE design, simulation, and checking tools for highly integrated 3D designs is a field that has been found to need improvements if complicated designs are to be handled efficiently and reliably.

The increased attention to modern interconnect and packaging technologies will for sure have a major positive impact on the physics performance (resolution and mass) of future tracking detectors. The vital questions of productivity, reliability, and finally cost will require continued, and when possible coordinated, activities in the HEP community in the coming years.

C. Optoelectronics

Future HEP detectors will make substantial use of optical connectivity for high-speed triggering, data readout, and control. The systems and components will have to comply with very demanding engineering constraints in terms of mass, volume, power dissipation, operational temperature, and radiation tolerance. Five papers were presented in this session, all related to future applications.

Two closely linked projects target the development of 4.8 Gb/s serial links to connect detector front-ends to counting rooms: GBT and the Versatile Link projects. The architecture and transmission protocols of the GBT chipset were presented, together with an extensive progress report spanning a wide range of designs: laser driver, transimpedance amplifer, SerDes,

control/monitoring, all of them in 130 nm CMOS technology. The status of these ASICs was reviewed and the implementation of the link protocol in an FPGA was demonstrated. A project roadmap to 2011 was presented. The Versatile Link project develops the optical physical layer of the link. Reports on the front-end transceiver developments and on the fibre radiation resistance were given. The capability to evaluate the functional performance of transceiver modules up to 10 Gb/s was highlighted, together with initial comparative results of commercial modules. Radiation resistance of lasers and PIN photodiodes operating at 850 nm as well as 1310 nm was discussed with encouraging results shown for neutron fluences well in excess of 10^{15} n/cm^2. Interconnecting the electronics with the optics is a challenge at those data rates, and a path to develop a customized low mass package for a front-end transceiver including ASICs and opto-components was described. The radiation-induced attenuation in two candidate multimode optical fibres was studied up to a total dose of 700 kGy. In line with results published in the literature, the measured attenuation was found to be much more pronounced at -25°C than at room temperature.

VCSEL and PIN diode arrays for an SLHC ATLAS pixel detector will have to be operating at neutron fluences of the order of several 10^{15} n/cm^2. Results from several irradiation runs were presented indicating promising performance, provided VCSEL annealing is taken into account. In the particular case of PIN diodes, the initial response of the diodes was shown to be recoverable after irradiation by increasing the diode reverse bias voltage by an order of magnitude.

Finally, the use of Passive Optical Networks (PONs) for timing distribution applications was demonstrated in a test set-up based on commercial PON transceivers and FPGAs. A full duplex bi-directional data flow with fixed latency was demonstrated using a simplified protocol.

At the end of the session, the Opto Working Group met to discuss the need for further meetings. Participants agreed that despite the emergence of well targeted common projects, a continuing communication forum on the subject is necessary. This need is enhanced further by the long foreseen timescales of the R&D period ahead of us. The working group chairs were thus encouraged to organize on a regular basis mini-workshops with invited and contributed presentations.

D. Systems, Installation and Commissioning

The completion of the commissioning of much of the LHC electronics systems allowed time in this session for presenting non-LHC projects. In these, there was clear evidence of the benefit of experience gained from LHC but also of developments that could be applied to future upgrades.

One very important subject is the noise experience of the LHC experiments in actual operational conditions, since this was hard to predict. CMS has studied and summarised the experience from commissioning its sub-detector systems over more than a year, including substantial periods of cosmic data taking. The results seem to be entirely positive. There is no evidence of much unexpected noise, except for minor issues involving HCAL photodetectors, and background effects traced to high power lights in the cavern, or associated with temporary welding operations. The widespread use of optical fibre transmission is likely to be one reason for this success, but it seems that prior concerns about grounding and shielding may have identified issues early enough for them to be overcome. Next year will be the acid test.

One specific CMS example is the case of the Muon Drift Tube system which was described. The cosmic data collected have been invaluable to study detector performance and it has behaved very efficiently and stably during data-taking. The complexity of its electronics was explained, including readout, trigger functions, services and monitoring. The quality of the DT data was found to be very good and independent of magnetic field with few integrity problems. At present, the DT Trigger has the expected performance and efficiencies and spatial and temporal resolutions are also as expected. The relatively lengthy period of operations has provided further confidence that the system is ready for LHC physics once beam operations resume.

There were two presentations from the newly-installed CMS Preshower detector. The first described the readout system consisting of 9U format boards equipped with optical receivers and FPGAs to carry out data reduction. The large size of the FPGAs required careful testing of their connectivity on the boards and specific test modules were developed to optimise speed and efficiency. The installation and performance of the front-end system of the Preshower were then presented. The detector was installed in a short period of time and first commissioning results indicate that 99% of channels are working with the expected signal-to-noise ratio. A change in the pedestal behaviour with magnetic field has been observed but is not expected to cause problems.

The non-LHC presentations covered several topics. A system for proton imaging was the first, consisting of a tracker of silicon microstrip detectors and a calorimeter of YAG:Ce scintillating crystals. To sustain the necessary event rate of 1 MHz, a data acquisition system was developed based on FPGA technology and parallel processing.

A novel system was presented for acquiring and processing the data from radio-telescopes mapping the distribution of hydrogen gas in the universe. Specific requirements of the system are the large signal frequency range, the difficulties of

transmitting fast timing signals across the large telescope array, and the high data throughput. Fast ADCs are used to convert to the digital domain early in the system. Complex signal processing is carried out in FPGAs and the high bandwidth is supported by Gb/s serial links between the modules. The challenges of precisely timing this system and handling the data bandwidth overlap nicely with requirements for many future developments.

A number of underwater neutrino experiments are running or planned for Mediterranean locations, and the data transmission system for the future KM3NeT project was presented. The emphasis is on a simple and reliable system which requires optical transfer of all data from photomultiplier modules up to 4000 m underwater to the shore. Wavelength division multiplexing will be employed to minimise the number of data fibres. The proposed scheme would use shore-based lasers sending light to passive modulators mounted on the underwater modules. Commercial developments, such as mating connectors that can survive high pressure, are being investigated for this project. The particular constraints on the layout and installation of the system were discussed.

E. Radiation Tolerant Components and Systems

A substantial amount of design effort in the particle detector community is now focusing on new designs for the SLHC, where radiation levels around the interaction points will increase by approximately a factor 10.

The Medipix3 full pixel readout chip, fabricated in 130 nm CMOS technology, was irradiated with X-rays up to 460 Mrad. Results confirm that this technology is a strong candidate for the fabrication of future pixel chips in the SLHC.

The new readout electronics for the ATLAS LAr Calorimeter upgrade is being designed in more radiation hard technology to deal with the expected constraints of SLHC. Current developments are focusing on radiation tolerant ASICs for the analog and digital frontends (both using a 0.13 μm CMOS process), the mixed-signal front-end ADCs, the silicon-on-sapphire serializer ASIC, the high-speed off-detector FPGA based processing units, and the power distribution scheme. First results of the ADC output stage were presented.

In the accelerator community, a considerable effort is made to reduce radiation damage to electronic equipment already installed and operational in the LHC underground areas. In contrast with the electronics located in the tunnel, most of the electronics in the protected alcoves does not rely on radiation tolerant designs. A system test campaign to validate the electronics built for the LHC cryogenic system was described. Whereas the radiation hardness of the signal conditioner cards for the LHC tunnel was once more confirmed in a complete system test, the insulated temperature conditioners and the AC heaters did not operate correctly due to damage from neutrons and from total dose. The short-term solutions currently being investigated are relocation and radiation shielding.

F. Power

Power supplies and power distribution are key issues for current experiments and will be a major challenge for future experiments. A lot of work is being invested in the subject and the number of presentations and posters submitted this year has reached the same high level as last year. There were 6 oral presentations in the dedicated power session, 2 posters and another 5 presentations during the ATLAS-CMS power working group session that followed. All contributions but one were related to the powering of the ATLAS and CMS upgraded trackers for SLHC; all of them dealt with power distribution efficiency.

A presentation of the powering of undersea experiments has shown that for these applications, a unipolar DC distribution together with DC-to-DC converters give the most efficient power distribution scheme.

The two main routes being pursued for the powering of trackers at SLHC (one based on DC-to-DC converters and one based on a serial powering scheme) have made impressive progress in a year.

On the serial powering front, a dedicated Serial Powering Interface (SPI) ASIC has been produced and successfully tested on readout hybrids. This chip contains some power devices (shunt regulator and linear regulators) and also service components such as AC coupled LVDS transceivers. Flip chip packaging techniques have been used to optimize the connection of the ASIC to the hybrid it powers. The capability of distributing the shunt transistors in the readout front-end ASICs was also validated on ATLAS readout hybrids using the available features of the ABCN chip. Some work has been done to optimize the power dissipated by the front-end electronics. With low feature size CMOS technologies (130 nm and below) the power consumption is dominated by the digital part of the readout chips and not anymore by the analog part. To reduce this digital power it is proposed to use two separate power lines, one for the analog part and one for the digital part at a lower voltage. It is then more efficient to have the digital power supply delivered by the shunt regulators and to produce the higher analog voltage with switched capacitors DC-to-DC converters embedded in the front-end ASICs. A design of such a converter has been done in a 130 nm CMOS technology; its efficiency should be about 80%. In the coming year some additional work at the system level is required to include all the control elements needed to implement, for instance, the necessary protection mechanisms as well as

efficient on and off switching of power elements. Prototyping of these elements in 130 nm (or below) technology is foreseen.

On the DC-to-DC converter front two main types of activities have been reported, one related to EMC issues and the second to the design of a radiation-hard converter.

Studies of EMC issues when switching DC-to-DC converters are used close to the detector and its front-end electronics have been carried out. Several tests have been done with different types of converters and different front-end systems (current CMS modules and prototypes of new ATLAS modules). The noise performance has improved a lot thanks to optimization of the layout of those devices and of the shielding of the air-core inductors. In most of the cases, the noise level when using these converters is identical to the one obtained using linear power supplies.

A CMS project aiming at studying and taking into account early enough in the detector system design phase the EMC issues related to the presence of a large number of DC-to-DC converters was presented. Such an approach would avoid the difficult and expensive implementation of late corrections.

The work towards the development of a radiation-hard DC-to-DC converter has been threefold: identification of suitable technologies, design of ASICs in these technologies and design of a complete converter with these components.

Five technologies have been extensively tested with radiation. One 0.25 µm technology has exhibited a very good behaviour and is the baseline for future developments, while a 0.35 µm technology identified last year can be used as backup.

Three ASICs have been designed, two in 0.35 µm technology and one in the newly identified 0.25 µm technology. Only the first two had been tested before the workshop. They work satisfactorily and a complete converter has been designed with one of them. This converter has been used with an ATLAS prototype module and has been irradiated. A small but acceptable loss in efficiency after 5 Mrad has been observed.

As in the case of serial powering, an optimization of the power dissipated in the front-end leads to the distribution of two separate voltages, one for the analog part of the chips and one for the digital part. It is proposed to distribute power at twice the needed voltage and to implement step-down switched capacitor DC-to-DC converters in the front-end ASICs. Such a converter has been designed in 130 nm CMOS technology; simulation shows that up to 90% efficiency can be obtained.

A work programme for the coming year has been presented. It includes the design of a DC-to-DC converter with the newly identified 0.25 µm technology, some optimization of the packaging in order to minimize the size of the converter and the ohmic losses, the integration of protection functions, and some studies at the system level.

CMS has selected the DC-to-DC converter solution as its baseline for powering (with the serial power scheme as fall-back solution) and is planning to use such devices for the first upgrade of their pixel detector. ATLAS is still pursuing the two options in parallel and will make a decision once they have both been tested on a prototype stave.

The very dense agenda of the power sessions and of the ATLAS-CMS power working group has limited the necessary time for fruitful discussion and it was agreed to organize in early 2010 a dedicated one-day workshop in order to go more deeply into results analysis and have more time for discussion.

G. Trigger

The trigger sessions were filled with results from running and commissioning experiments, as well as studies of upgrades to the LHC experiments.

The challenges for the trigger and data acquisition systems for experiments such as NA62 and COMPASS involve processing high data rates without data losses and with high efficiency. Experiments are moving to all-digital systems to allow more complex and flexible logic as well as more comprehensive monitoring.

The present status of important aspects of LHC experiment trigger systems was shown for LHCb, CMS and ATLAS. These presentations were largely focused on the activities of commissioning and the first operations phase of the trigger systems, which were used in data taking, recording cosmic muons for long periods, after the machine stop of autumn 2008. While waiting for the first collisions, activities were mainly concentrated on the development of timing and energy calibration procedures.

Regular data taking runs are preparing the detectors for the restart of the LHC. Strategies for setting the parameters that will be used in colliding beams have been developed. Furthermore, online and offline Data Quality and Monitoring has been set up to provide intensive and precise trigger studies on performance and efficiency.

A large fraction of the work is still dedicated to the development of the software tools, which are essential for system operations and monitoring. Layered software frameworks have been developed in many cases, for configuring, controlling and testing, partial or complete trigger systems.

In the framework of the SLHC upgrade, two proposals for a Level-1 tracking trigger, one from ATLAS and one from CMS, were presented. Studies are required for a detailed understanding of detectors, for pile-up simulations and data reduction techniques. Two key issue are very important, for compatibility with the existing sub-detector systems;

first, the trigger rate must not exceed the present one by much and secondly, the level-1 trigger latency must not increase by more than a few microseconds. Upgrade studies for the SLHC CMS Trigger highlighted new ideas on architectures and tests of newer technologies, such as Advanced Telecommunications Computing Architecture (ATCA), high speed serial links, cross-point switches and large Field Programmable Gate Arrays (FPGAs) with integrated serial links. These offer capabilities and flexibility significantly greater than the present LHC trigger systems in more compact hardware.

H. Programmable Logic, Boards, Crates and Systems

This plenary session consisted of one invited talk and three oral presentations. In fact, several other presentations during the workshop could have qualified for this session but were given elsewhere due to synergy with other sessions.

The invited talk on Recent Advances in Architectures and Tools for Complex FPGA-based Systems presented the expected short and medium term development of FPGA technology. It introduced a set of tools available or under development to help firmware designers to profit from these advances.

The three contributed presentations introduced FPGA based solutions to implement functions that in the past were solved by other means.

The first presentation described a TDC (Time to Digital Converter) implementation based on high frequency oscillators. The second described the FPGA implementation of a high speed serial transceiver, SerDes and CoDec suitable for the counting house side of the GBT based optical link (see sections A and C). The third presentation introduced an FPGA based solution for a Bit Error Rate tester.

All presentations pointed to the fact that the areas where the use of FPGAs may be a valid alternative to ASICs or to expensive instruments for particular tasks is widening rather fast and that the complexity of the firmware development and in particular its verification and testing is increasing rapidly.

I. Posters

The courtyard of the Institut des Cordeliers provided a spacious setting for the TWEPP-2009 Poster Session. Some sixty posters were displayed describing forefront work on ASICs, Radiation Effects, Power, Systems and Triggering to name a few. The display area covered three full walls and allowed viewers full access to the posters over the course of the week. The dedicated poster session was particularly well attended by presenters and viewers alike and the resulting discussions were quite lively and animated. For the first time this year, posters were grouped by topic. By doing this it was easier for attendees to locate posters of interest to them. In addition, each oral session had a separate projector to show where posters related to that session could be found. In general, the grouping of posters appeared to work well and was well received.

III. Conclusion

As confirmed by the large attendance this year, the TWEPP workshop seems to have established itself as a reference European event for the community of electronics designers in High Energy Physics. Even though the currently running machines and experiments will keep us busy for many years to come, a healthy development cycle targeting future applications has started, as highlighted by the majority of the presented contributions.

In a dynamic and rapidly evolving environment, a high quality forum to exchange ideas, collaborate and create synergies is a necessity. This year, the workshop could benefit in Paris from excellent conditions both in terms of venue and organization, thanks to the outstanding preparation and efficiency of the local organizing committee [2].

IV. Links

[1] http://indico.cern.ch/event/twepp09
[2] http://twepp09.lal.in2p3.fr/