Roadmap for power distribution using DCDC converters

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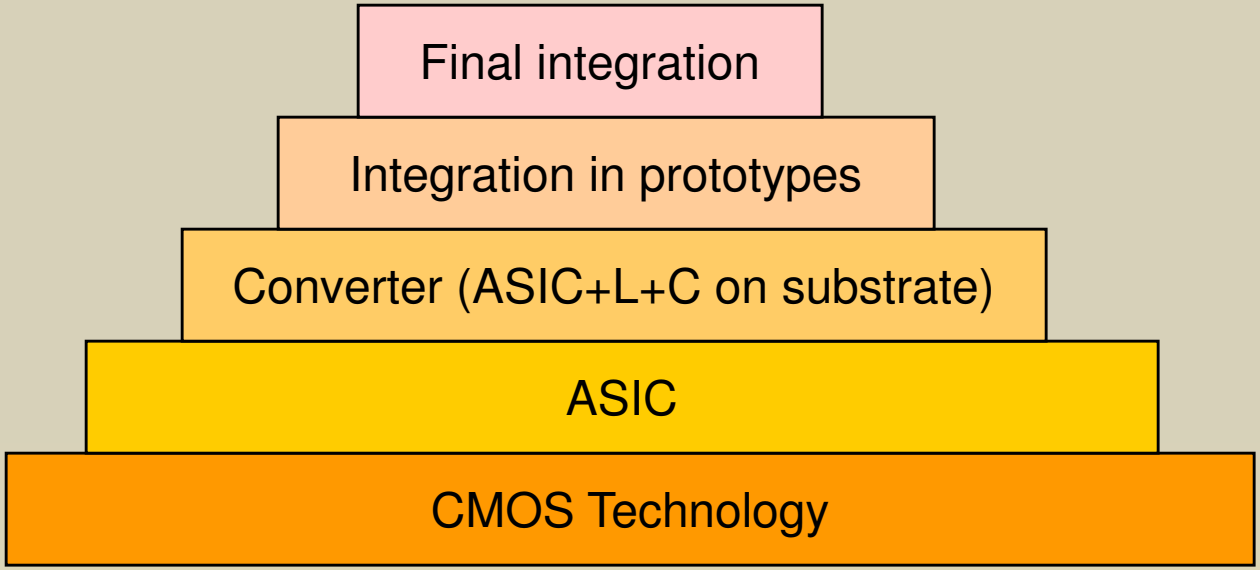
CERN – PH/ESE

Outline

- DCDC inductor-based (first stage)
  - The building layers
  - The past year
  - What needs to be done
- Switched capacitor converter (second stage)
- Conclusion

The building layers

DCDC inductor based (buck)



Technology

- TWEPP08
  - Test in 0.35um only
  - Contacts with another vendor
- TWEPP09
  - Test for TID and displacement in 5 technologies
  - Best technology selected (0.25um), backup available (0.35um, lateral NMOS)

CMOS Technology

ASIC

- TWEPP08
  - First prototype (AMIS1) with only main loop and vertical power transistors
  - Efficiency low
  - Relevant radiation effects
- TWEPP09
  - Second prototype (AMIS2) working well, lacking regulators and protections only
  - Efficiency OK, radiation effects acceptable
  - First prototype in 0.25um delivered this week (main loop with sophisticated handling of dead time)

ASIC

Converter (ASIC+L+C on substrate)

- TWEPP08
  - Large or “noisy” air core inductors
  - Relatively large PCBs with commercial components
  - Conducted noise seemed a problem
- TWEPP09
  - PCB and custom wrapped inductors demonstrated
  - Small PCBs, also with ASICs, produced
  - Conducted noise decreased to almost class B
  - Radiated noise still to be decreased further, but improved
  - Projected final size appealing

Converter (ASIC+L+C on substrate)

Integration in prototypes

- TWEPP08
  - Noise induced by DCDC converters on systems subject of discussion
  - Importance of radiated noise evidenced
  - Contribution of conducted noise subject of discussion
- TWEPP09
  - Contribution of conducted noise not measurable
  - Radiated noise important only in close proximity, and it can be reduced further
  - General feeling that noise issues can be solved

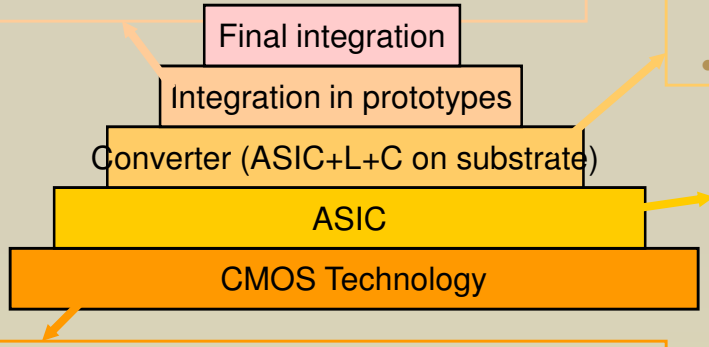
Integration in prototypes

What needs to be done

- Work on all layers can be done in parallel now
  - One-hybrid systems already good for representative measurements
  - Prototype converters already available and very useful to undertsand system-level issues

What needs to be done

- Analyse noise coupling mechanisms
  - On existing systems
  - On new hybrid prototypes
- Study system-level stability
  - DCDC is seen as negative load
  - Drive requirements for the power supplies
- Slowly define requirements for the final integration



- Progress in miniaturization
- Understand noise consequences of design choices (size, position of capacitors, filters)
- Define appropriate value of L
  - Understand limit of PCB technology
  - Explore in depth the possibility to use a custom wrapped L (material, size, cost, shielding)
- Decide a shielding strategy

- Strenghten link with manufacturer
- Measure sensitivity of power transistors to Single Event Effects (SEB, SEGR). With this measurement, the safe operation area can be defined (Vds)
- Monitor regularly the radiation tolerance to verify it
- Keep second source

- Fully test first prototype in chosen 0.25um technology. Verify efficiency gain with special dead time handling
- Integrate additional functions
  - Vbgp, Regulators, OverI protection
  - OverV and overT protection
  - Protection against SEUs
- Choose and prototype appropriate packaging (flip-chip)
- Keep backup ready (AMIS2)

Possible application for phase1

- Interest expressed in use of DCDC for phase1 upgrade (CMS pixels)
  - Is this feasible?
    - Realistic schedule has to be provided – how much delay will LHC safe operation require?
    - Manpower availability to be addressed
  - Excellent opportunity for a first real integration!
  - Requirements and schedule look compatible with planned development

Switched capacitor

- On-chip, conversion ratio ½, 2/3, …
  - Circuit relatively simple
  - Main focus: demonstrate the feasibility of its integration on the FE chips (compatible with noise requirements)
  - A small library of IP blocks with different current capability and conversion ratio will be useful

Conclusion

- Progress has been excellent over the past 12 months on all “layers”
- We have, as a community, built a solid fundation for this development (knowledge, collaboration network, material, test systems)
- We definitely have a good view of the road ahead of us, and are ready to address system-level requirements
- If available resources are confirmed (continuity is needed), DCDC converters will be available for the SLHC upgrades – and for phase 1 if needed