ASIC buck converter prototypes for LHC upgrades

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In the context of a new power distribution scheme for SHLC tracker based on switching DC/DC converter, we are developing a custom converter able to work in the high radiation and high magnetic field environment of the experiments. A new ASIC prototype has been designed and manufactured. Design techniques, functional and radiation tests of the prototypes will be discussed.

I. Introduction

In view of a possible upgrade of LHC trackers where the number of channels will increase and the front end (FE) circuits will probably require larger supply current at lower voltage, it is necessary to evaluate alternative power distribution schemes.

At Twepp 2008 a new power distribution scheme based on DC-DC converters has been presented [1]. It foresees two different conversion stages to obtain the voltages required by the power domains (2.5V for the optoelectronic drivers, 1.2V for the analog circuit and 0.9V for the digital)

The first conversion stage is represented by a buck converter capable of converting 10-12V to 2.5-1.8V with an output current of 1-2A.

Commercial components are not targeted to work in the harsh experiment environment characterized by high radiation (more than 100Mrd in total dose) and high magnetic field (up to 4T). It is therefore necessary to develop a custom inductor-based switching converter where tolerance to radiation and magnetic field are specifically addressed.

Hardness to radiation can be achieved through specific modification of the layout and magnetic tolerance can be attained using air-core inductors (all ferromagnetic cores saturate at 4T), whose value is limited up to 500nH to fit the limitations of space and material budget [2].

As presented at Twepp 2008 a first converter ASIC has been developed in a 0.35µm high voltage technology (HVT).

In the last year a second more mature ASIC has been completed in the same technologyand tested.

The ASIC is a fully integrated buck converter with embedded voltage mode control loop (also with passive components). It includes two lateral high voltage NMOS, an oscillator with programmable frequency up to 3MHz, a voltage reference and a soft-start procedure to avoid large inrush current at the start-up of the converter

Design techniques, functional and radiation tests will be presented in this paper.

II. DC-DC buck converter

The basic scheme of a buck converter with voltage control loop are rappresented in Fig.1. The power stage contains the two power switches that rule the charge and discharge phase of the storage energy element rapresented by the indutor and the capacitor. The control loop senses the output voltage, the error amplifier EA amplifies the difference with a reference voltage and its output is compared with a sowtooth signal to generate the PWM waveform that drives the switches.

The ASIC contains the two power switches (in this paper high and low side will be called SW1 and SW2 respectively) with their drivers, the error amplifier (EA) and the comparator whereas the ramp generator, the voltage reference, the compensation loop's passive components, a soft start circuit and a more advanced logic.

Fig. 1 summarizes the blocks integrated in the new ASIC

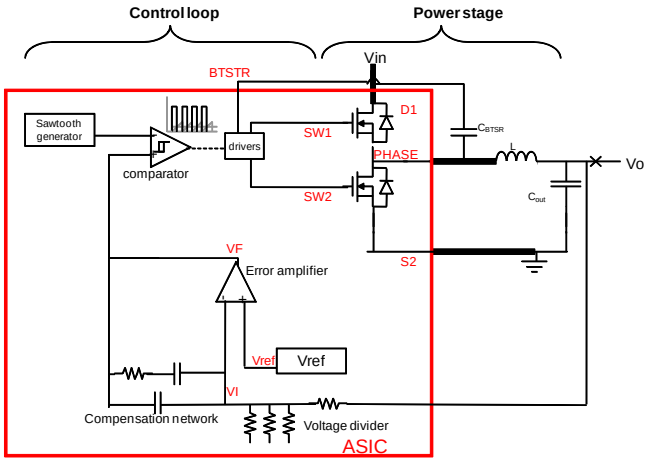

Fig 1: buck DC-DC converter building blocks and their integration in the ASIC

III. Design of the converter

Other than the specifications in terms of input and output voltage and output current, the design of the converter requires that a choice is made in terms of size of the power transistors and switching frequency. These can be chosen to optimise the efficiency that is calculated considering all the conversion losses: conductive (on parasitic resistance), switching (overlap of Ids and Vds during the switching time) and driving losses (charge and discharge of the power transistors' gate). All these losses are strongly technology dependent; therefore a complete parameter extraction of the selected technology was carried out to allow for a meaningful evaluation.

The estimate of all losses can be used to compute the efficiency of the converter for varying frequency and output load and it appears that the best compromise is a frequency in the range 1-3MHz. It appears also that the converter should

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work in an operation mode called quasi-square-wave (QSW). This is a continuous mode with the inductor current that goes slightly negative. Leaving a delay between the gates of the two power switches, the inductive load forces the current circulating in their parasitic diodes. This allows having a low Vds (equal to the forward voltage of the diode (~0.7V), instead of Vds=Vin) during the switch-on of the power transistor, reducing is such a way the on-switching losses. The drawback is a higher rms value of the inductor current that leads to a small increase of the conductive losses.
The design of the converter follows the division of the converter in two main building blocks. The following subsections will explain the design methodology for the power transistors and the control circuit.

A. Power transistors

The power transistors design is one of the crucial parts of the development of the converter. Studies in this direction were already presented [3] together with radiation tolerance results [4].
With respect to the ASIC presented at Twepp 2008 where vertical high voltage transistor has been used, the new ASIC integrates smaller and more radiation tolerant lateral devices. They can stand a Vds up to 14V, value compatible within the input voltage requirements.
As already done for choosing the frequency, it is possible to calculate the efficiency for different dimension of the switches and for different output currents. The best compromise can be reached with a W of 0.3m for SW2 and 0.15m for SW1. The latter can be smaller because the duty cycle is around 25%, therefore the rms value of the SW1 current ($Irms_{SW1}$) is around half of the $Irms_{SW2}$.
The W values brings to a Ron_{SW1}=52 mOhm, Cg_{SW1}= 7.9nF, Ron_{SW2}=26 mOhm and Cg_{SW2}=15.8nF

B. Control circuit

The control section has to be properly studied in order to compensate for the disturbances caused by input line voltage and output load current variations and hence to ensure the stability of the output voltage over a wide frequencies range (bandwidth of the converter control loop). The control circuit design requires a system level model of the converter. This analysis was developed in [5]. The design of the control circuit can be divided in two main tasks: the design of the ASIC blocks (error amplifier, comparator, bandgap, level shifter and bootstrap) and the choice of the passive components for the compensation network. They will now be shortly expanded.

1) Error amplifier

The error amplifier (EA) circuit is a key point in the design of the control loop. It is necessary to design the EA with a bandwidth larger than the one desired for the full control loop, otherwise this last will be reduced. Moreover, the gain has to be very high (at least 70dB) to avoid errors on the value of the output dc voltage [3]. In this design the EA is implemented with a Miller amplifier with a DC gain of 80dB and a bandwidth of 15Mhz. The same design of the EA is used in ASIC1 and ASIC2

2) Comparator

The comparator generates the PWM modulation from the output of the EA and the sawtooth ramp. The latter has very high frequency components, hence the comparator needs to have a very large bandwidth to avoid distortions of the output signal possibly affecting the width of the PWM modulation. The comparator was implemented as a 3 cascaded stages amplifier with a bandwidth of 100Mhz and a dc gain of 50dB. The same comparator is embedded in both ASIC1 and ASIC2.

3) Bandgap

The bandgap has been designed for being radiation tolerant and temperature independent. The used scheme is proposed in Fig.2. Diodes current density and squared shape have been chosen to avoid changes with the induced radiation induced leakage current.

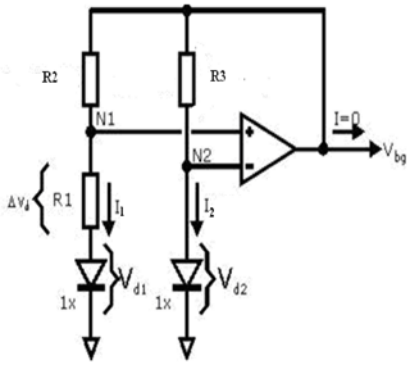

Fig 2: Bandgap scheme

4) Non overlapping driver

The signal provided by the comparator is used to generate the drive signal of the two power switches. It is necessary to avoid any overlap of the two gate control signals to prevent shoot-through between the input node and ground at every cycle which could damage or at least drastically affect the efficiency of the converter. The correct timing of the two gate signals is depicted in Fig.3.
Despite to the too small delay time of the old prototype in this ASIC the delay is internally fixed at 50ns and it is possible to modify it through external pins.
Further development of the converter is foreseen with an adaptive logic that changes the delay accordingly to the state of the circuit.

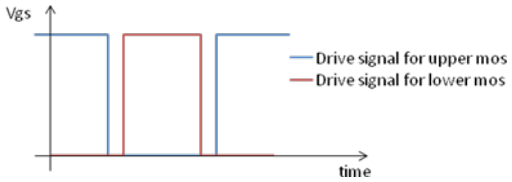

Figure 3: example of non overlapping gate signals

5) Level shifter and bootstrap circuit

The driving of the SW1 is difficult because the source of this transistor is connected to the output node, which is cyclically connected to Vin or ground. A special circuit is needed to shift the signal referred to ground (generated by the non overlapping driver) and refer it to the source potential. This can be done by a level shifter in combination with a bootstrap circuit. The basic scheme is presented in Fig.4. Basically the circuit charges a capacitance (called bootstrap capacitor) to 3.3 V through D1 when the phase voltage is 0 and it connects this capacitance between source and gate of the power MOS (through P2) in the other phase to switch it on (as shown in Fig.5). To switch it off the level shifter circuit connects the gate to the source (node Phase through P3) as shown in Fig 4 and 5. N1 and N2 work like a differential pair to shift the signal to the higher voltage. P1 is used to P2 for the switching on phase.

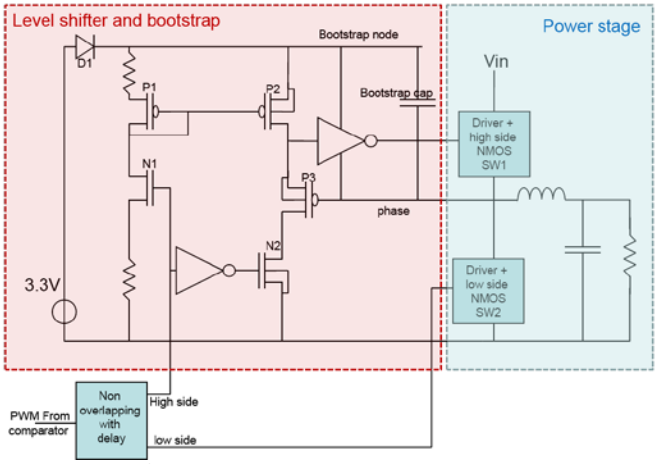

Figure 4: level shifter and bootstrap scheme with the power stage

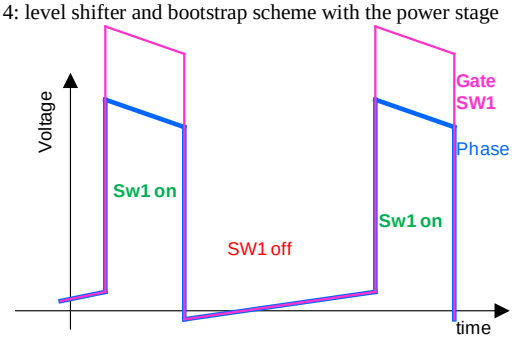

Figure 5: Ideal phase and gate$_{SW1}$ waveform

6) *Drivers of the power transistors*

The driving circuit needs to be able to switch on and off the transistor in few nanoseconds. For that reason the power switches are divided into four parts to better distribute the gate signal. Each part has its own driver that needs to be carefully sized to drive some ampere during the switching period. Hence the last driver stage (an inverter) needs to be big (W_{Pmos}=10mm and W_{Nmos}=4mm). These dimensions leads to losses due to cross conduction of the inverter, therefore it is mandatory to implement a non-overlapping circuit as shown in Fig.6, where two different buffers drive the last inverter and their signals are generated from the PWM with the required delay.

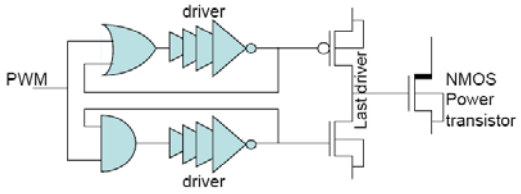

Figure 6: drivers of the power transistors

7) *Passive components for compensation network*

The compensation network is necessary to increase the bandwidth of the control loop and its DC gain. Three different compensation networks are available; they have been explained in [4]. For the ASIC a type 2 compensation network is used in order to achieve a crossover frequency of 20Khz with a phase margin of 70°. The value of these passive components can be found using the equations given in [4].

IV. Circuit Layout

The design of the layout must take into account different issues. First of all the NMOS transistors have to be custom modified to increase their radiation tolerance. Low-voltage NMOS transistors in the control circuit are modified with standard ELT techniques [5][6][7] whilst high-voltage transistors require a slightly modified enclosed topology.

Given the large current flowing (peak up to 4 A) in the power transistors their layout was studied to minimize the resistance between input and output terminals. The layout was also optimized to maintain low gate resistance to achieve short propagation delay of the gate signals.

Multiple unit cells have been used for the design of these large transistors. This allows a more uniform distribution of the current over the different cells, hence a more efficient use of each cell. The external pad needs to be placed in order to decrease parasitic capacitance, resistance and inductance and to simplify the PCB design.

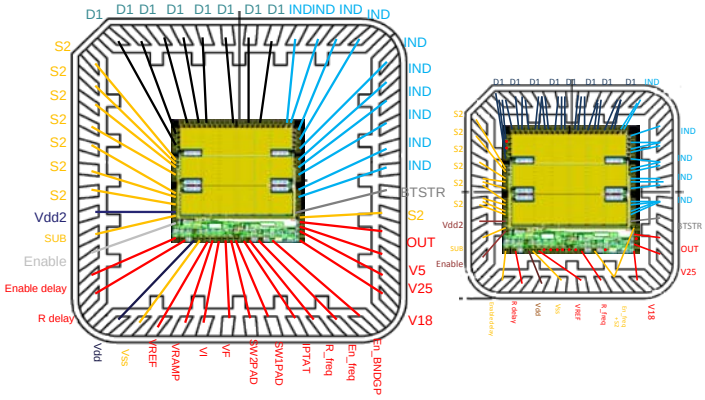

Figure 7: layout of the ASIC within the QFN48 and QFN32 packages

The power transistors switch very fast and the speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device over-voltage stress. To partially decrease the injection of theses spikes to ground a decoupling capacitor can be placed on PCB really close to the ASIC. To facilitate this placement in the layout D1 (connected to Vin) of SW1 (Fig.1 and Fig.7) is placed close to the source S2 of the SW2 which is connected to ground.

Techniques to reduce coupling to substrate noise were adopted. The high and low voltage NMOS are isolated from the substrate with a separated Nwell (triple well NMOS).

The layout of the ASIC is represented in Fig. 7. It has dimension of 3x3 mm^2 , it has been fitted in a QFN48 package for the testing phase and it is currently under packaging in a QFN32 for further system tests.

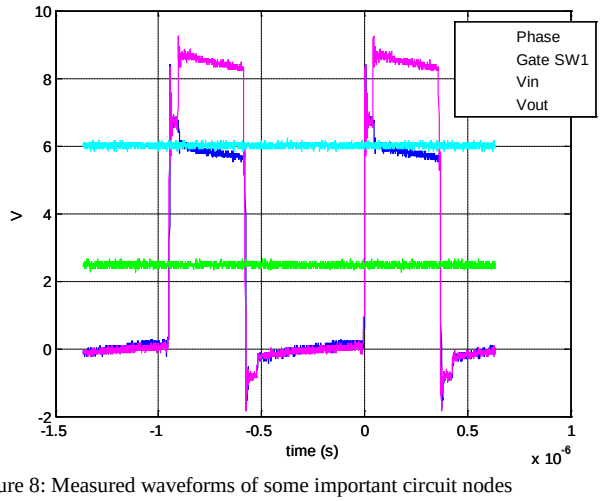

Figure 8: Measured waveforms of some important circuit nodes

V. MEASUREMENT ON THE PROTOTYPE

The ASIC converter was measured to verify its performance in terms of efficiency and radiation tolerance.

The waveforms of input, output, phase and gate SW1 nodes are depicted in Fig. 8. The shapes of the phase and gate SW1 voltages are very similar to the ideal presented in Fig. 5

A. Efficiency measurements

Fig.9 shows the measured efficiency of the buck converter for different loads obtained by the output/input power ratio.

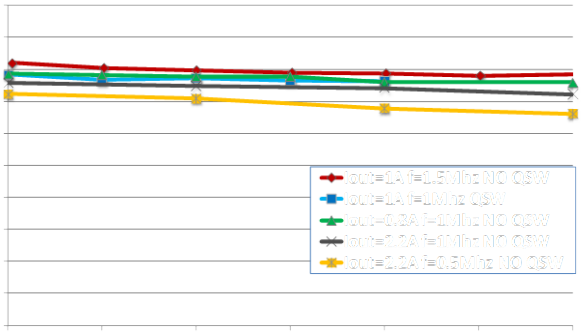

Figure 9: Efficiency vs frequency with Vin=10V,Vout=2.5V and L=538nH

The lowest efficiency values are measured for low frequency operation (0.5Mhz). This can be explained by the fact that at lower frequency the current ripple is higher and therefore the related conducted losses are also more important. For 1Mhz the efficiency is almost equal for different load (0.8-2.2A) and different operation mode (QSW and no QSW). The best efficiency can be reached with a frequency of 1.5Mhz even if the converter doesn't work in QSW. This means that even if the switching losses are not reduced the converter benefit of a higher switching frequency that reduces the current ripple.

This brings to the conclusion that the conductive losses are dominant and that the resistive path of the transistor is much higher than expected.

Measurements of the real resistance of the switches have been carried out and they are depicted in Fig.10

For SW2 the measured resistance of the silicon R_{Si} is around 30mΩ, the on-chip metal routing R_M is 50mΩ and the wire bonding of QFN48 contributes with additional R_{Bond}=80mΩ. The total resistance is 160mΩ, value more than five times R_{Si}. In the new QFN32 the wire bondings are shorter and therefore the R_{Bond} should be smaller. In further development the converter will be bump-bonded and this will drastically reduce R_{Bond}.

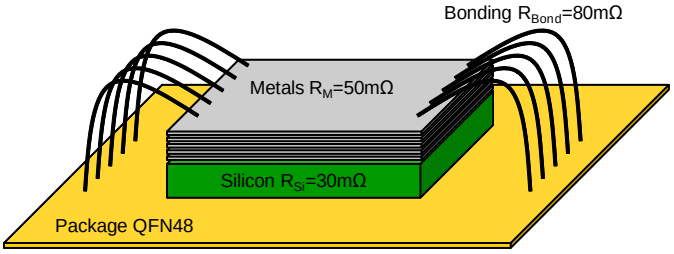

Figure 10: Measured resistance of SW2

B. Radiation measurements

The ASIC was irradiated at room temperature and under working condition (at 1.5Mhz, Vout=2.5V amd Iout=1A) at the SEIFERT RP149 X-ray machine facilities at CERN. The dose rate used was about 77 krd/min, and irradiation was performed in steps up to total ionizing dose (TID) levels of 300 Mrd (SiO2). Fig. 11 shows the efficiency versus the TID for different input voltages. The efficiency ax is limited between 70% and 82% to better appreciate the efficiency shift. The inefficiency peak is located around 4Mrd and that matches with the maximum of the radiation-induced leakage current of the HV NMOS transistors. These measurements have been presented in [8].

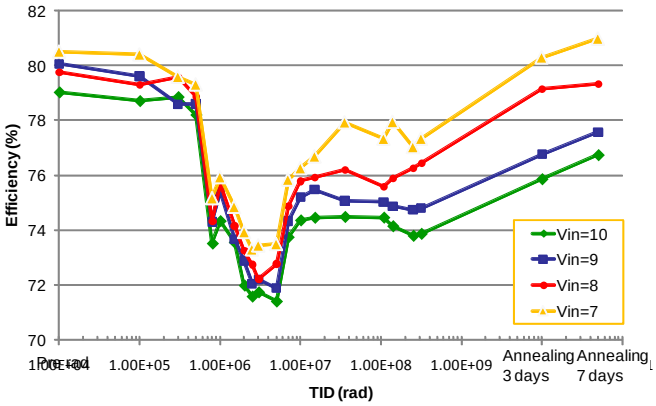

Figure 11: Efficiency vs TID for Vout=2.5V and Iout=1A

VI. CONCLUSIONS

In view of a new power distribution scheme in the SLHC detectors, we have designed two ASIC aiming at the integration a buck converter able to cope with the radiation and magnetic field requirements of the SLHC environment.

Only air-core inductors can operate in the 4T magnetic field. Such components are commercially available and imply an increase of the switching frequency of the converter to some MHz, which is compatible with the performance of the commercial high-voltage technologies available today. Radiation tolerance has been demonstrated up to doses that can cope with SLHC requirements.

Further development will be addressed to a complete integration aiming to a converter composed by an ASIC, few capacitor and the air core inductor with efficiency higher than 80%.

VII. REFERENCES

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