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ASIC buck converter prototypes for LHC upgrades

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In the context of a new power distribution scheme for SHLC tracker based on switching DC/DC converter, we are developing a custom converter able to work in the high radiation and high magnetic field environment of the experiments. Two new ASIC prototypes, in two different technologies, have been designed and manufactured. Design techniques, functional and radiation tests of the prototypes will be discussed.

Summary

In view of an increase of the current required by the front-end (FE) circuits for SLHC trackers, a new power distribution scheme based on DC/DC converters has been proposed at TWEPP 2008. A first converter ASIC developed in the 0.35μm AMIS high voltage technology (HVT) has been presented as well.

We have since completed the design of two more mature converters, one in the same AMIS process and the other in the 0.25μm IHP HVT.

The AMIS prototype is a fully integrated buck converter with embedded voltage mode control loop (also with passive components). It includes two lateral high voltage NMOS with Rdson=20mΩ and 40mΩ (low and high side respectively), an oscillator with programmable frequency up to 3MHz, a voltage reference and a soft-start procedure to avoid large inrush currents at the start-up of the converter. The delay time between the gate signals is by default 50ns and it can be changed with external resistors. The ASIC is mounted in a 7x7mm QFN package, allowing the design of a compact PCB.

After the delivery of this chip, expected for mid-May 2009, tests will be carried out and results will be presented at TWEPP.

While the ASICs engineered in the AMIS process were developed for understanding the design issues of a fully integrated DC/DC converter, a market survey for other available commercial HVTs was held to find one that can be tolerant to radiation, both for total ionizing dose and displacement damage. The 0.25μm IHP technology showed the best radiation tolerance and also electrical performance, therefore we decided to move the design of the converter in this HVT.

In view of the integration of the converter in the system, small converter size (chip and PCB dimensions and number of external components) and high efficiency (above 80%) are specifically addressed in this design. For this purpose a study of different converter topologies and working modes was carried out, showing that the best compromise is a buck converter that works at a frequency of few MHz and in a conduction mode called quasi square wave (QSW). As it will be explained in details in the final paper, this mode ensures a reduction of the switching losses. For the same reason, the internal control loop has been equipped with an adaptive logic circuit, developed on purpose to make the delay between the power MOS gate signals no longer fixed (but always shorter than a pre-selected value).

The ASIC developed in the IHP technology has been included in a shuttle MPW run in May 2009. It embeds two power transistors (a lateral PMOS for the high side with Rdson=25mΩ and a lateral NMOS with Rdson=10mΩ for the low side), the voltage control loop and an oscillator with nominal frequency of 2 MHz that can be changed with external resistors. This chip will also be bonded in a 7x7mm QFN package.

The delivery date of this ASIC is foreseen for July 2009 and test results will be presented at TWEPP together with a detailed description of the chip design.

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