Precise Timing Adjustment for the ATLAS Level1 Endcap Muon Trigger System

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Abstract

The ATLAS level-1 endcap muon trigger system consists of about 4000 Thin Gap Chambers (TGC) with 320,000 input electronics channels in order to find level-1 trigger candidates for muons in both endcap regions. Three TGC stations are deployed with about 1m interval with 15m apart from the interaction point in z-direction on each endcap side and the radius of the station (disc form) is about 25m. Usually hit signals are not timely aligned because of different cable length and different time of muon flight. In order to supply reliable level-1 endcap trigger signals, we must adjust timing of hit signals for all the channels with the precision of $\pm$2.5ns. In the meantime we have to adjust also the bunch crossing phase used in the TGC system with one from LHC. We need, however, actual bunch crossing signals in order to accomplish this. In this paper we discuss strategies for timing alignment of individual channels with the timing adjustment facility embedded in the TGC electronics system and for the adjustment of the phase shift of the bunch crossing signals.

I. Introduction

For supplying the level-1 endcap muon signals, we have installed about 4000 Thin Gap Chambers (TGC) to cover almost full region of both endcaps of the ATLAS detector ($1.05 < |\eta| < 2.4$)[1].

In order to make a trigger signal with various coincidence logic operation, all hit signals from tracks generated at pp collisions in a bunch should be aligned in principle in the same timing, our detected signals will be usually spread in total from 65 to 116 ns owing to

1. the time of flight of particles (45$-$64ns), and
2. the signal propagation delay (9$-$60ns).

Even if we adjust this spread of signal timing for individual channels, we have to identify a bunch in which all the signals are produced. We call this operation the bunch identification. The bunch crossing signals (40 MHz) arrived at the TGC electronics as the basic clock pulses supplied by the TTC system[2] are also delayed and fluctuate among channels within 25ns. We have to adjust the bunch crossing signals in all the channels. We have to synchronize the TGC bunch crossing signal with the one comes from LHC. Since this operation consumes the luminosity, we have to estimate carefully the statics necessary for this operation to minimize the luminosity dedicated for this work.

In the next section, we discuss how to cope the timing spread caused by delay with the time of flight of particles and signal propagation delay in cables. Lining up all the signals in one timing, we then have to adjust a bunch phase with one from LHC. In section III. , we discuss this clock phase adjustment. For smooth and quick scan to find the best adjusted clock phase, we needed to develop a new VME module which is called delay module. This module will be installed in between the ATLS central trigger processor which gives TGC the bunch crossing

signals and the TGC TTC system in order to supply the delay timing of the phase shift to all the channels uniquely at once. In this section we discuss also the role of this module in detail. For doing the clock phase scan, we need actual beam, namely we consume the luminosity. We have to fix carefully a scenario to do this in the most efficient way. We discuss the strategy established and the statistics needed from the simulation study. Finally in section IV., we summarize the work for the precise timing adjustment we have done since the first beam circulation in September 2008, and the outlook for the collision which will be foreseen in the end of 2009 or the beginning of 2010.

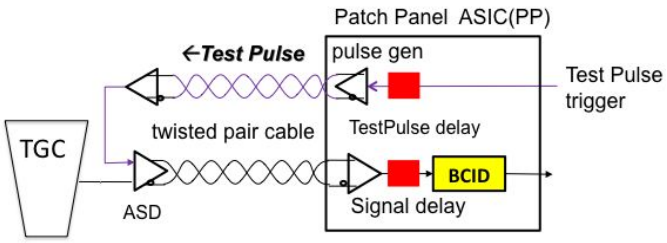

Figure 1: Schematic diagram of test pulse Generation and detection between ASD and PP ASIC chips

II. Adjustment of individual hit signals

The TGC electronics system is divided into the on-detector and off-detector parts. The on-detector part contains several kinds of homemade ASIC chips. The ASD (Amplifier, Shaper and Discriminator) chip and the PP (Patch Panel) ASIC are two of these homemade ASICs. The ASDs are mounted in vicinity of the TGC as a front-end electronics while PP chips are installed in the beginning part of the on-detector part. The PP ASIC has a delay circuit to adjust the timing of a hit signal in 0.83ns step up to 26ns, test pulse generator to check the ASD connectivity, and a synchronization circuit of the hit signal with the bunch crossing signal (clock). All these circuits are installed commonly in each signal channel. A 16-ch ASD board at the TGC side and PP ASIC at the on-detector part are connected with LVDS cables of 834 different types whose lengths vary from 1.8m to 12.5m. The total number of cables used are about 10000. Since coincidence circuits to generate trigger candidates are placed just behind the PP ASIC, one of our important tasks for timing adjustment is to align the timing of signals for all the channels in the PP ASIC.

The test pulse generator in a PP chip is used to simulate the timing (time of flight and the propagation delay) of particles for the ASD. If a test pulse trigger signal arrives at the PP ASIC via the TGC TTC system, a test pulse is generated after a predefined delay interval and is sent to the ASD which sends back the ASD output to the PP chip immediately. The delay interval time can be set in two step modes; a coarse mode with one clock (25ns interval) step from 0 to 7 clocks, and a fine mode with 0.83ns step from 0 to 26ns maximum (the same precision as the signal delay circuit), namely we could set the delay from 0 to 200ns with 0.83ns step. If we set the predefined delay interval as "the cable length$\times$the propagation speed$-$the time of flight", we can simulate a signal generated in a particular channel by muon from the interaction point.

Since the time of flight is known from the geometrical position of TGC region covered by the ASD, we can examine the delay timing caused only by the propagation time of signals in a cable between the ASD and PP ASIC.

In fig. 1, a schematic diagram of the cable connection between two chips and the test pulse generator is shown.

Beside simple measurement for the propagation speed of signals, we must also consider the smearing effect due to the attenuation of signals which pass through long cables. As shown in fig. 2, we can clearly see this effect; longer is a cable, more the effect is enhanced for both the test pulse input at the ASD and the returned ASD signal through LVDS and observed at the PP.

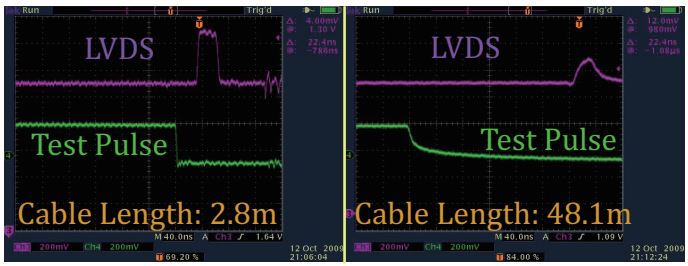

Figure 2: Attenuation effects observed after long propagation in cables of length 2.8m and 48.1m. "LVDS" indicates the ASD output of a TGC signal observed just in front of the PP ASIC while "Test Pulse" is Test pulse generated in PP and observed in front of ASD. The full width (time range) of the both scope pictures is 400ns. It is divided into 10 subunits of 40ns interval.

We have made systematic study of this effect, and found additional delay factors of roughly 0.2ns/m for Test Pulses observed in ASD though the dependence is not linear (we have estimated this additional delay factor with a polynomial function as the cable length). We have included this effect in the precise delay adjustment beside the standard propagation delay unit of 5ns/m.

With this optimization of propagation speed in a cable, we have measured the trigger timing distribution. For the correction of the timing, we must also know the length of all the cables (about 10000). We believed simply the cable length (from 1.8 to 12.5m) from the information given by the cable production company. In this case signals were distributed broadly from -4ns to 10ns with the standard deviation of 1.5 (1.23ns) as shown with the (blue) slashed hatch pattern histogram in fig. 3. As the distribution is unexpectedly broad, we then carefully treat the length of cables. We have measured delay timing of cables with

each type for all 834 types. We have found that the delay timing was fluctuated and its average was shifted from the expected one which comes from the nominal cable length in every type. The shift value depends on the type (cable type dependency). We have incorporated the actual shift values for the cable length estimation for all the types. Histogram with the 25% darkened (red) pattern is the timing distribution corrected with this cable type dependency. Although the distribution has been significantly improved than simple cable length correction, several channels have been corrected insufficiently yet as we see entries outside the $\pm$4ns region in this histogram. We speculated some cables in a particular type have had quite different length rather than nominal length. For all those cables which shows the timing shifts bigger than $\pm$2.5ns (data fallen outside of central 6 bins), we then have measured individually actual lengths (individual cable correction). and used this information for the cable length correction, and finally gotten the timing distribution as indicated in the histogram with 50% darkened (black) pattern. In this ultimate correction of the cable length, we have adjusted the signal timing alignment with $\pm$2.5ns precision as we can see from the figure for all the channels.

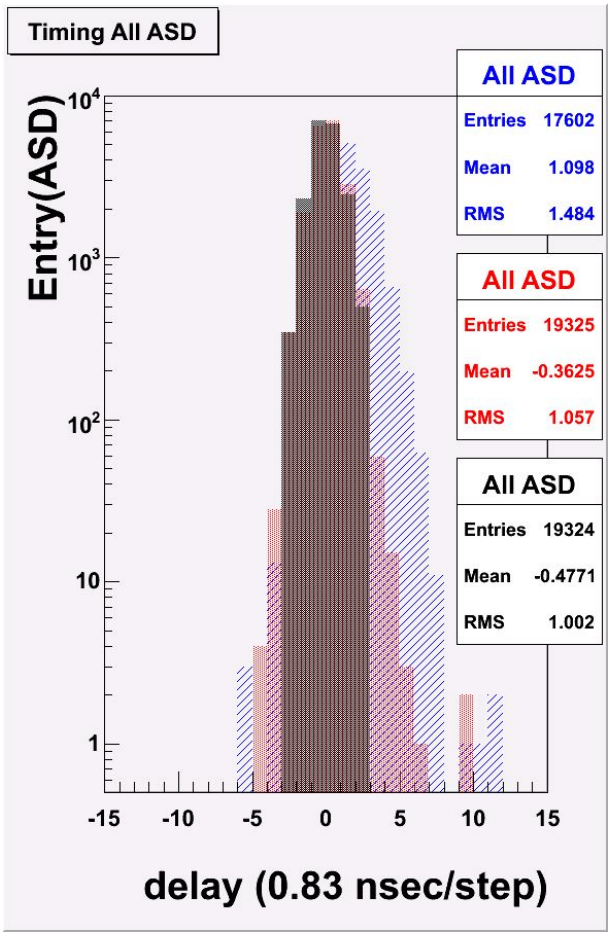

Figure 3: Trigger timing distributions. Three histograms are resulted with three different cable length corrections. See text in detail. The width of one unit on the abscissa is 0.83ns; the smallest PP delay adjustment timing.

III. Bunch Crossing Identification

As shown in fig. 4, TGC signals are intrinsically distributed in 25ns interval. TGC electronics system tries to catch the hit signals if a level-1 trigger is given in a bunch crossing. Some hit signals will be lost easily, however, if the bunch crossing signal in the TGC system is not adjusted correctly to one which the LHC machine produces for a specified level-1 trigger signal.

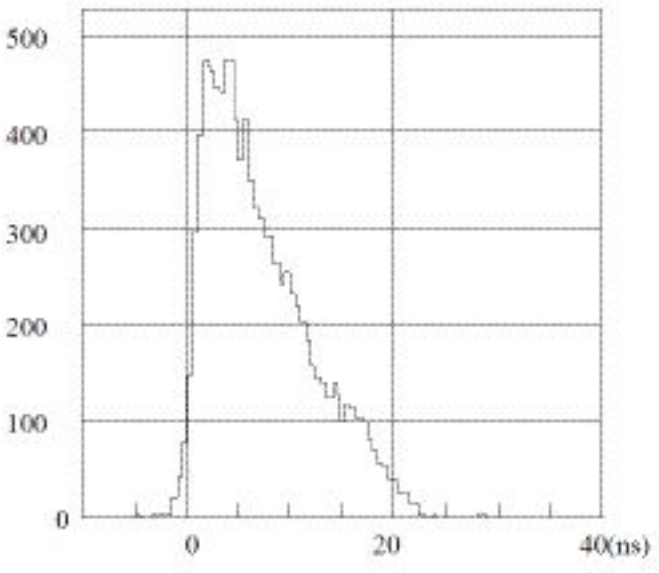

Figure 4: A typical TGC hit distribution[3]

The TGC electronics records always hit signals observed in three contiguous bunches around the triggered bunch (previous, current and following bunches). Number of hit signals observed in the previous or following bunches will not be ignorable if the bunch crossing signal adjustment is made slightly advanced or delayed to one given by LHC. In order to measure the phase shift of the bunch clocks of the TGC system and LHC, therefore, the ratio of the number of hit observed in the triggered bunch to total number of hits observed in all three bunches must be useful quantity. If this phase shift adjustment is correctly done, the number of hits counted in previous and following bunches are in principle zero. It turns out that the timing difference which gives the maximum ratio closest to one must be an actual shift existed between two systems. We can adjust thebunch crossing phase in this way with LHC. Figure 5 shows a simulation result of the dependency of this ratio with the phase shift. While LHC makes stable beam-beam collision, we will be able to find a point of the maximum ratio as demonstrated in the figure if we plot this ratio with changing the TGC bunch clock phase artificially with 1000events per point with 1ns step.

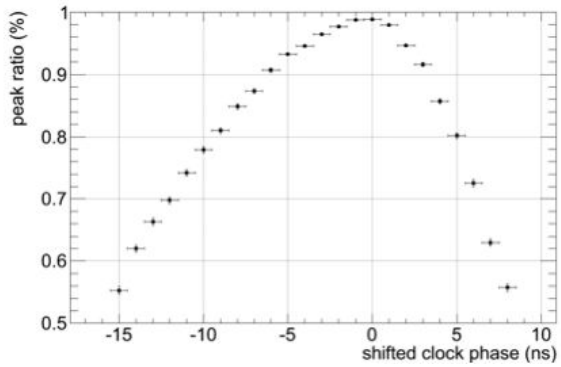

Figure 5: The ratio of the number of hits observed in the triggered bunch to total numbers observed in all three bunches versus the bunch crossing difference between TGC and LHC (simulation)

Figure 6: The delay module we have made to adjust the phase shift between the TGC and LHC bunch crossing signals. The circuit is housed in a VME 6 unit module

The phase shift is just one unique parameter to let whole the TGC system synchronize with the LHC system. As discussed in section II., we have achieved to align the timing of all individual TGC channels in 2.5ns precision. In this process, we have naturally adjusted also the bunch phase for all the channels. One last parameter we have to adjust is, therefore, this phase shift. Since, at the moment to write this manuscript, LHC has not yet supplied any bunch signal, we could not adjust it yet. Our precise timing adjustment will be completed when we optimize this phase shift. We expect the phase shift adjustment will be done smoothly and quickly if LHC works constantly. We had had a problem of how to reflect this unique parameter at once to whole the TGC system. An LHC bunch crossing signal is delivered to the TGC system from the ATLAS Central Trigger Processor (CTP). At the TGC side, TTCvi modules [2] are used to receive this signal, fan-outed and distributed to TTCrx installed in the various parts of the TGC system. Since TTCvi has no facility to delay the received bunch signal before its fan-out, what we have had to do is to build newly a delay module by ourselves to install it between CTP and TTCvi to insert an amount of seconds equal to the phase shift. There has been no such a module prepared in the standard TTC module set. We have made a module for this purpose. It can insert a delay span in 0.5ns step precision with total 64 steps (0-31.5ns). The delay is generated simply using coaxial cables of different length. A picture of this module is shown in fig. 6. The circuit is installed in a VME 6U module and its VME control mode is A24D16.

IV. Summary

We have made timing adjustment of individual channels using embedded test pulse function and delay adjustment system which we can tune the signal delay in 0.83ns precision. With these facilities we tried to adjust timing of hit signals which are usually widely distributed due to difference of signal cables and geometrical positions even the origin (muon track) of signals is produced at once. Otherwise we could not make trigger signals using the trigger coincidence logic. We have used about 10000 LVDS cables with 834 different types (1.8m to 12.5m length difference) to connect front-end ASD chips with corresponding PP ASICs on the on-detector electronics in the TGC system. After precise estimation of the propagation speed of signals in a cable, which includes also the attenuation effect of signals, and with the optimization of length of individual cables, we could manage to adjust hit signals within $\pm$2.5ns for all the individual channels as shown in fig. 3.

Although we need definitely beam collision in LHC to adjust the phase shift of bunch crossing clocks between LHC and the TGC electronics, we have been ready to estimate this phase shift with enough precision and the least consumption of the luminosity. From the simulation study, we may be able to find the phase shift if we take 1000 events per data point by artificially changing amount of the shift from -15ns to 9ns with 1ns step for 25 points. If the expected L1A rate will be 500Hz which will be achieved if the LHC luminosity is $10^{31} cm^{-1} s^{-1}$, we can take 2s to calculate the ratio which has been discussed in section III. for one data point. The phase shift parameter is a unique one between the TGC system and LHC to adjust if the phase shift in the individual channels has been adjusted. We had, however, had no delay adjustment facility to modify the phase shift for all the channels at once. We have made a delay module to do that with 0.5ns step for total 64 steps range.

As the timing adjustment for individual channels has been finished. If LHC will supply beam stably, we expect that we optimize the best phase shift in about half an hour. In such a way, our timing adjustment will be completed, and the TGC trigger system will supply reliable L1A candidate signals for muons in the endcap region to the ATLAS CTP.

References

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