Microelectronics User Group Meeting

TWEPP 2009, Paris

22/9/2009

Agenda

- *17:30 – 17:45*

  “Access to ASIC design tools and foundry services at CERN for SLHC”
  by Kostas Kloukinas (CERN)

- *17:45 - 17:15*

  “Mixed-Signal Challenges and Solutions for advanced process nodes”
  by Bruno Dutrey (Cadence Design Systems SAS, Velizy, France)

- *17:15 – 18:45*

  “Digital Block Implementation Methodology for a 130nm process”
  by Sandro Bonacini (CERN)

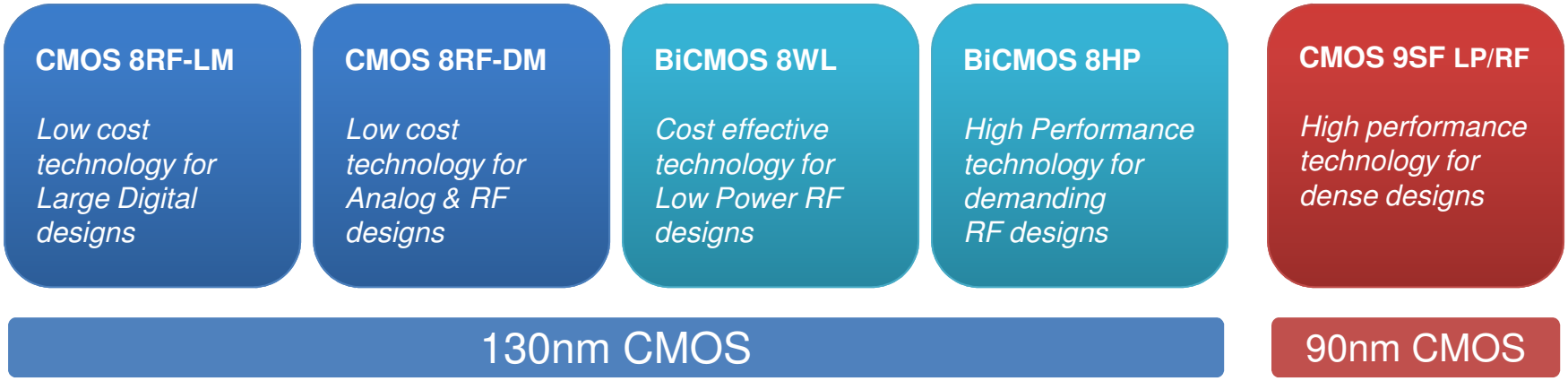
- *18:45 – 19:00*

  “Discussion”

Access to ASIC design tools and foundry services at CERN for SLHC

Kostas Kloukinas
CERN, PH-ESE dept.
CH1211, Geneve 23
Switzerland

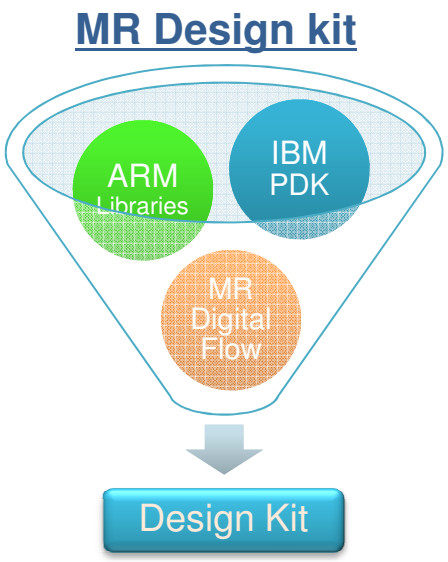
Overview of Technologies



- Access to Foundry services & Technology technical support.
- 130nm (CMOS & BiCMOS) and 90nm contract available since 6/2007.
- Future technologies can be negotiated with the same manufacturer, once the necessity arise.

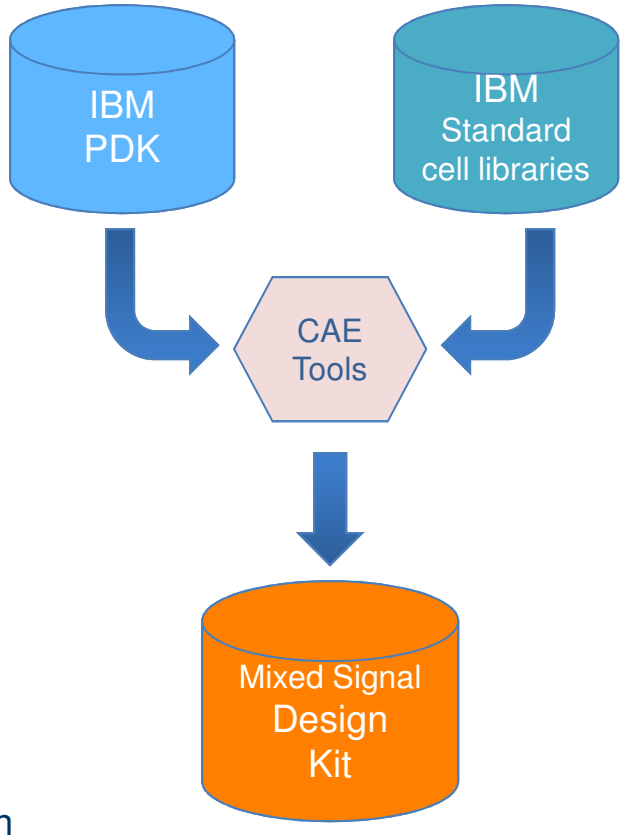
PDK and Mixed Signal Design kit

- Objectives
  - Development of a “Design Kit” for Mixed Signal environments.
    - With integrated standard cell libraries.
    - Establish well defined Analog & Mixed Signal design workflows.
    - Targeted to **big “A”** (analog), **small “D”** (digital) **ASICs**.
    - Implemented on modern versions of CAE Tools.
  - Replace our previous Design Kit distribution.
    - Based on the ARM/ARTISAN cells and an automated *digital only* design flow.
    - Making use of old versions of CAE tools.
    - Two years in service.
    - Already distributed to 25 institutes
    - Users can continue using the old design kit and the ARM libraries since they have signed NDAs directly with ARM. Maintenance and technical support will be provided by ARM.



CMOS8RF Mixed Signal design kit

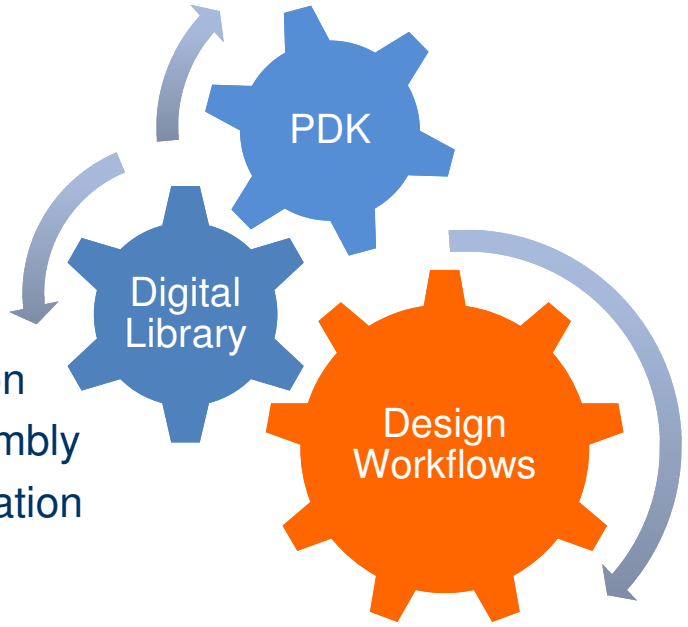
- Key Features:
  - IBM PDK V1.6
  - IBM Standard cell and IO pad libraries
    - Physical Layout views available.
    - Separate substrate contacts for mixed signal low noise applications.
    - Access to standard cells libraries is legally covered by already established IBM CDAs
  - New versions of CAE Tools
    - Open Access database support for increased interoperability of Virtuoso and SOC-Encounter environments.
    - Compatible with the “Europractice” distributions.
      - Virtuoso IC 6.1.3, Analog front-end design
      - SOC Encounter 7.1 Mixed signal back-end design
      - IUS 8.1 support for simulations.
      - Calibre support for Sign-Off Physical Verification
  - Support for LINUX Platform (*qualified on RHEL4*)



- Two independent design kits:
  - CMOS8RF-LM (6-2 BEOL)
  - CMOS8RF-DM (3-2-3 BEOL)

CMOS8RF Mixed Signal Workflows

- Analog & Mixed Signal (AMS) Workflows.
  - Standardized, validated Design Workflows
  - Top-down design Partitioning.
  - Digital Block implementation flow
    - *Presentation by Sandro Bonacini (CERN)*
  - Mixed-Signal Simulation & design Concept Validation
  - Hierarchical design Floorplaning and Physical Assembly
  - Design Performance Validation and Physical Verification



- CERN – VCAD Cadence - IBM collaboration
  - VCAD brought in their invaluable expertise on the CAE tools
    - *Presentation by Bruno Dutrey (VCAD)*
  - IBM provided the physical IP blocks and important technical assistance
  - CERN assists the development and validates the design kit functionality

Design Kit Distribution

- The Design kit will be made available to collaborating institutes.
  - No access fees required.
  - Pay-per-use scheme.
    - Some small fees will be applied when prototyping the designs through CERN,
    - This should cover part of the design kit maintenance costs in the long term.
  - Planned for release in October 2009.
  - Announcement by e-mail to the “130nm user list”.

- Acquiring the CMOS8RF Mixed Signal Design Kit
  - Contact Bert.Van.Koningsveld@cern.ch
    or Kostas.Kloukinas@cern.ch
  - Establish a CDA with IBM (if not already in place).
  - Granted access to the CERN ASIC support web site.

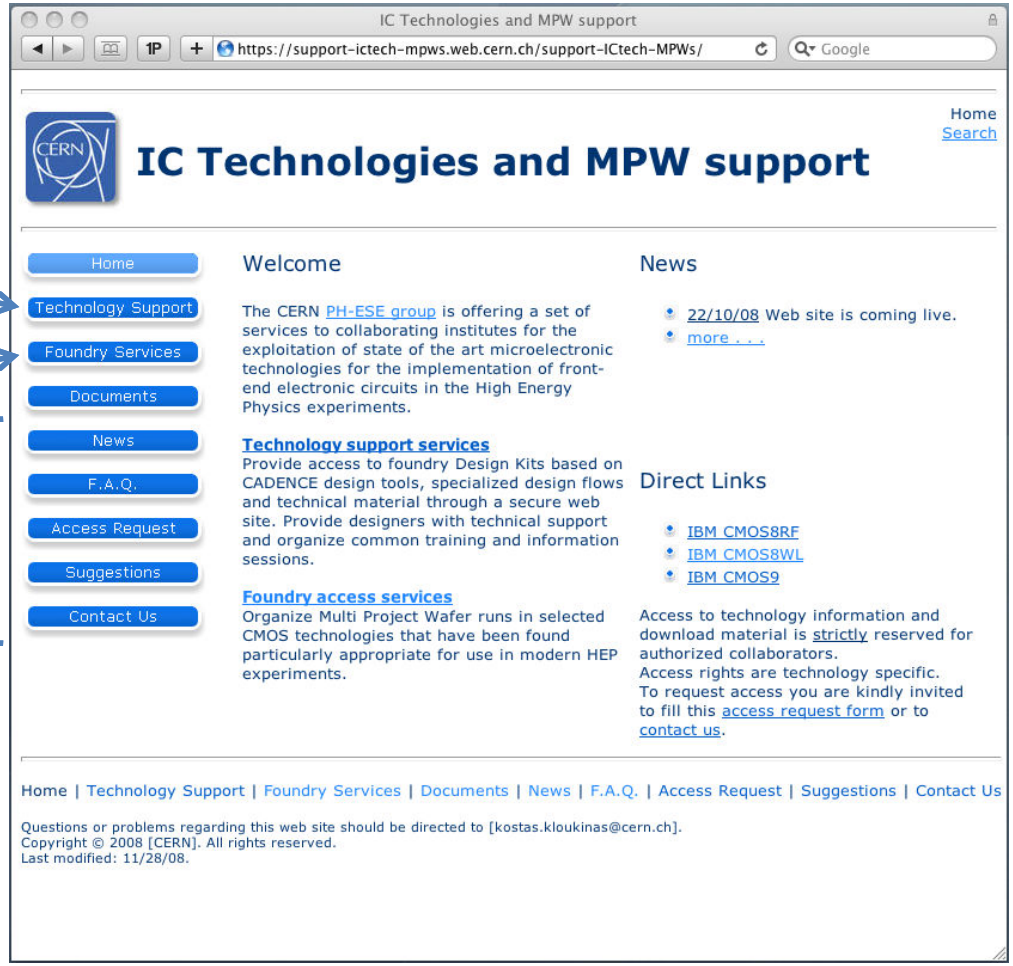
The CERN ASIC support website

http://cern.ch/asic-support

Download Design Kits and access technical documents (**restricted access**)

Information about MPW runs and foundry access services.

Communicate news and User support feedback forms and access request forms.



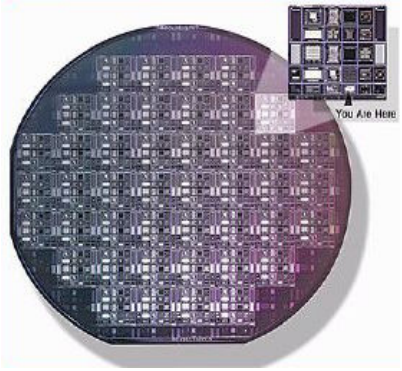
This website replaces our ‘afs’ based download facility.

User Support and Training

- Maintenance
  - Distribution of:
    - IBM PDK updates.
    - Design Flow updates and enhancements.
    - Updates to accommodate new releases of CAE tools.
- User Support
  - Limited to the distributed Design Kit version, running under the supported versions of the CAE design tools.
- Training sessions organized at CERN
  - Scheduled sessions:
    - 1st session: 26 to 30 October (CERN internal)
    - 2nd session: 16 to 20 November (open to external engineers)
    - 3rd session: 30 Nov to 4 December (open to external engineers)

Access to Foundry Services

- Supported Technologies:
  - IBM CMOS6SF (0.25μm), legacy designs
  - IBM CMOS8RF (130nm), mainstream process
  - IBM CMOS8WL & 8HP (SiGe 130nm)
  - IBM CMOS9SF (90nm)



- MPW services:
  - CERN offers to organize MPW runs to help in keeping low the cost of fabricating prototypes and of small-volume production by enabling multiple participants to share production overhead costs.
  - CERN has developed very good working relationships with the MPW service provider MOSIS as an alternate means to access silicon for prototyping.
- Engineering runs
  - CERN organizes submissions for design prototyping and small volume production directly with the foundry.

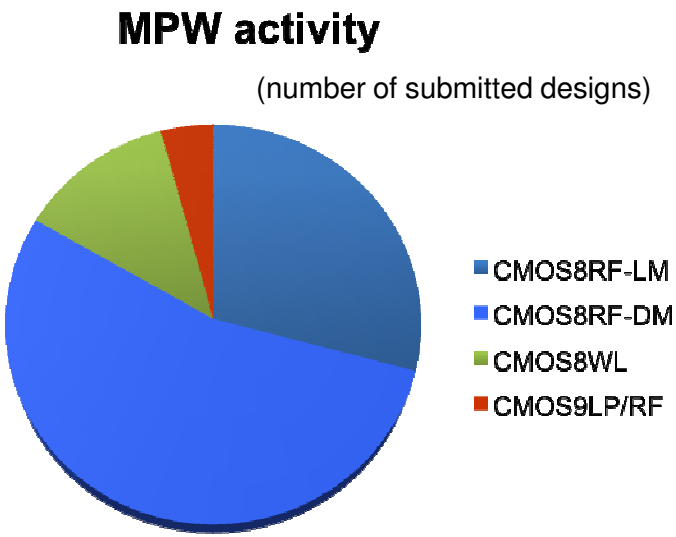
MPW runs with MOSIS

- CERN made extensive use of the MOSIS CMOS8RF MPWs last year.
  - The break-even point for the cost of a CERN MPW and a MOSIS MPW is ~150mm^2.
- Negotiations with MOSIS allowed for better pricing conditions for the CMOS8RF MPW services
  - MOSIS recognized the central role of CERN in research and educational activities.
  - 35% cost reduction compared to 2008 prices
  - Waived the 10mm2 minimum order limit per submission
  - CERN appreciates the excellent collaborating spirit with MOSIS
- Convenience of regularly scheduled MPW runs with MOSIS.
  - In 2008 there were 6 runs scheduled every 2 months.
  - In 2009 there will be 4 runs scheduled every 3 months.
- Convenience for accommodating different BEOL metallization options:
  - DM (3 thin - 2 thick – 3 RF) metal stack.
  - LM (6thin – 2 thick) metal stack.
  - C4 pad option for bump bonding.

Prototyping activity with MOSIS

2008 - 2009

- CMOS8RF (130nm)
  - 20 designs on 5 MPW runs
    - 7 runs organized, 2 canceled by MOSIS due to insufficient number of designs
    - 2 to 8 designs per MPW run
    - Smallest design 1 mm^2, largest design 20 mm^2
    - 13 designs on 8RF-DM and 7 designs on 8RF-LM
  - 100 mm^2 total silicon area
- CMOS8WL (130nm SiGe)
  - 3 designs on 1 MPW run
  - 10 mm2 total silicon area
- CMOS9LP/RF (90nm)
  - 1 design of 4mm^2 on 1 MPW

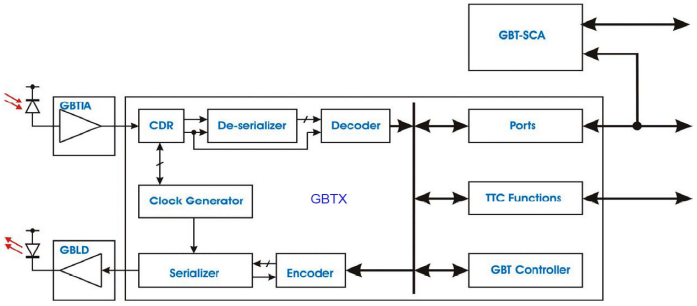


- Re-fabrication requests: 2 designs on 8RF and 2 designs on 8WL

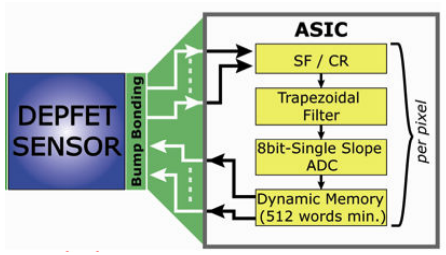
Major Projects

not a comprehensive list

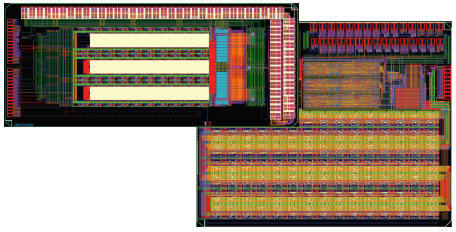
- Gigabit Transceiver Project (GBT)
  - "GBLD" Gigabit Laser Driver chip
  - "GBT-TIA"Tranimpedance Amplifier chip
  - "e-link" test chip
  - "GBTX", first prototype transceiver chip (2009Q4 MPW)



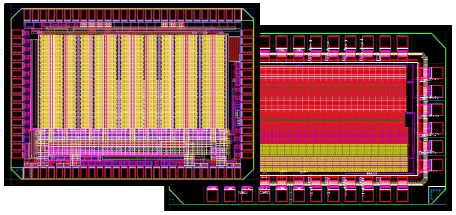
- DSSC Project for the XFEL Synchrotron Radiation Source
  - DRAM test chip, SRAM, test chip, some digital blocks
  - Front-End with source follower readout for DEPFET
  - Front-End with drain follower readout for DEPFET
  - Current-mode trapezoidal filter
  - First proto with all elements in the pixel, bump test chip (2010 MPW)



- NA62 Pixel Gigatracker detector
  - Readout test chip with ON pixel TDC cell
  - Readout test chip with End-Of-Column TDC cell



- ATLAS PIXEL 'b-layer upgrade'
  - Discriminator test chip
  - SEU evaluation test chip
  - FEI4 first full scale prototype chip (2009Q4 engineering run)



Prototyping activity with IBM

2008 - 2009

- CMOS8RF Engineering run **submitted** in 2008Q3.
  - "MEDIPIX-3" PIXEL matrix readout chip.
  - Size: 14 X 17 mm^2
  - 12 wafers ordered.

- CMOS8RF **scheduled** Engineering run
  - "FEI4", ATLAS PIXEL readout chip
  - 19 X 20 mm^2
  - Tape out : 2009Q4

Wrap-Up

- Technology support & foundry services.
  - Provide standardized common design kits and design flows.
  - Provide access to advanced technologies by sharing expenses.
  - Organize common Training and Information sessions.
  - Collective activities help to minimize costs and effort.

- Availability of foundry and technology services is modulated by user's demand.

- Your feedback is welcomed. Please contact:
  - Organizational issues, contracts etc.:
    - Alessandro.Marchioro@cern.ch
  - Technology support & Foundry services:
    - Kostas.Kloukinas@cern.ch
  - Access to design kits and installation:
    - Bert.van.Koningsved@cern.ch

THANK YOU

Agenda

- 17:30 – 17:45
  - “Access to ASIC design tools and foundry services at CERN for SLHC” by Kostas Kloukinas (CERN)
- 17:45 - 17:15
  - “Mixed-Signal Challenges and Solutions for advanced process nodes” by Bruno Dutrey (Cadence Design Systems SAS, Velizy, France)
- 17:15 – 18:45
  - “Digital Block Implementation Methodology for a 130nm process” by Sandro Bonacini (CERN)
- 18:45 – 19:00
  - “Discussion”

Agenda

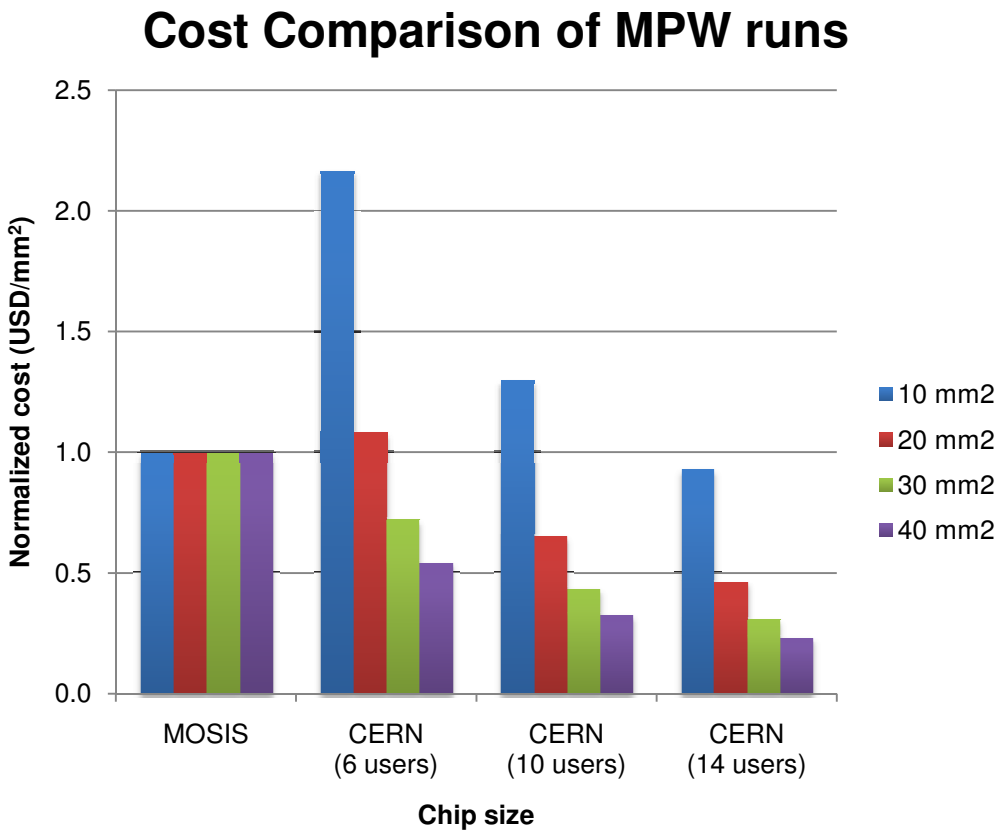
- 17:30 – 17:45
  - "Access to ASIC design tools and foundry services at CERN for SLHC" by Kostas Kloukinas (CERN)
- 17:45 - 17:15
  - "Mixed-Signal Challenges and Solutions for advanced process nodes" by Bruno Dutrey (Cadence Design Systems SAS, Velizy, France)
- 17:15 – 18:45
  - "Digital Block Implementation Methodology for a 130nm process" by Sandro Bonacini (CERN)
- 18:45 – 19:00
  - "Discussion"

Agenda

- 17:30 – 17:45
  - “Access to ASIC design tools and foundry services at CERN for SLHC” by Kostas Kloukinas (CERN)
- 17:45 - 17:15
  - “Mixed-Signal Challenges and Solutions for advanced process nodes” by Bruno Dutrey (Cadence Design Systems SAS, Velizy, France)
- 17:15 – 18:45
  - “Digital Block Implementation Methodology for a 130nm process” by Sandro Bonacini (CERN)
- 18:45 – 19:00
  - “Discussion”

SPARES

130nm MPW Pricing (2009)



- The break-even point for the cost of a CERN MPW and a MOSIS MPW is ~150mm^2.
- At present the level of demand is below threshold for CERN-organized MPWs.

Technology Key Features

	8RF-LM	8RF-DM	8WL	8HP	9SF	9LP/RF
Process	130nm	130nm	130nm SiGe	130nm SiGe	90nm	90nm
Vdd (V)	1.2/1.5	1.2/1.5	1.2	1.2	1.0/1.2	1.0/1.2
Pad cell (V)	2.5/3.3	2.5/3.3	2.5/3.3	2.5/3.3	2.5	2.5
Level of Metals	6-8	6-8	6-8	6-8	4-10	4-10
Metalization	Cu	Cu + Al	Cu + Al	Cu + Al	Cu	Cu
Analog Thick Metal	No	Yes	Yes	Yes	No	Yes
Density (Kgates/mm2)	200	200	200	200	400	400
Power (μw/MHz/gate)	0.009	0.009	0.009	0.009	0.006	0.006
Ring Osc. Delays (ps)	27	27	27	27	21	21
Bipolar beta	-	-	230	600	-	-
Bipolar ft (GHz)	-	-	100	200	-	-
MIMcap (fF/μm^2)	n/a	2.05	4.1	1.0	n/a	
VNCAP (fF/μm^2)	n/a	1.3	1.3	n/a	n/a	
Resistors	n$^+$diff. p$^+$, p$^-$ poly. tantalum	n$^+$diff. p$^+$, p$^-$ poly. tantalum	n$^+$diff. p$^+$, p$^-$ poly. p poly tantalum	n$^+$diff. p$^+$, p$^-$ poly. tantalum	n$^+$diff. p$^+$, p$^-$ poly. tantalum	n$^+$diff. p$^+$, p$^-$ poly. tantalum
efuse	yes	yes	yes	yes	yes	yes

CMOS8RF Technology Features

Standard Features

- **130 nm lithography, twin-well on 1-2 Ω-cm non-epi P- substrate, low K dielectric**
- **Thin Oxide (22Å gate) FETs (1.2 /1.5V)**
- **Thin Oxide MOS Varactors**
- **Forward bias diodes**
- **N-well resistor**
- **5 to 8 levels of metal**
  - Thin and thick Cu metal (~0.3/0.55 μm)
  - Last metal options:

    LM: Cu 0.55μm DM: 3 μm Cu + 4 μm Al
- **Vertical Natural Capacitor**
- **Spiral inductors, RF Transmission lines**
  - Series & Symmetrical inductors in DM wiring option only
- **Electrically programmable fuses**
- **Wire bond or solder bump (C4) terminals**

Optional Features

- **Triple-well NFETs**
- **Thin Oxide Low power FETS**
- **Thin Oxide Low-Vt FETs**
- **Thick Oxide (52Å) 2.5V FETS**
- **Thick Oxide (52Å) 3.3V FETS**
- **Thin and thick Oxide Zero-Vt NFETs**
- **Thick Oxide MOS Varactors**
- **Hyperabrupt Varactor**
- **Polysilicon and diffused resistors**
- **TaN metal resistor**
- **Single and dual-layer MIM capacitor (DM option only)**

CMOS8RF Wiring options

	LM Last Metal						DM Last Metal				
	8	7	8	7	6	5	6	7	7	8	8
DM Option							MA	MA	MA	MA	MA
							E1	E1	E1	E1	E1
							LY	LY	LY	LY	LY
LM Option	LM	LM	LM	LM	LM	LM					
2X Levels	MG	MG							MG	MG	
	MQ	MQ	MQ	MQ	MQ	MQ	MQ	MQ	MQ	MQ	MQ
1X Levels			M6								
	M5		M5	M5							
	M4	M4	M4	M4	M4						M4
	M3	M3	M3	M3	M3	M3		M3		M3	M3
	M2	M2	M2	M2	M2	M2	M2	M2	M2	M2	M2
	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1
Code	5-2	4-2	6-1	5-1	4-1	3-1	2-1	3-1	2-2	3-2	4-1

Fabrication Through MOSIS

MOSIS MPW Fabrication Schedule (indicative*)

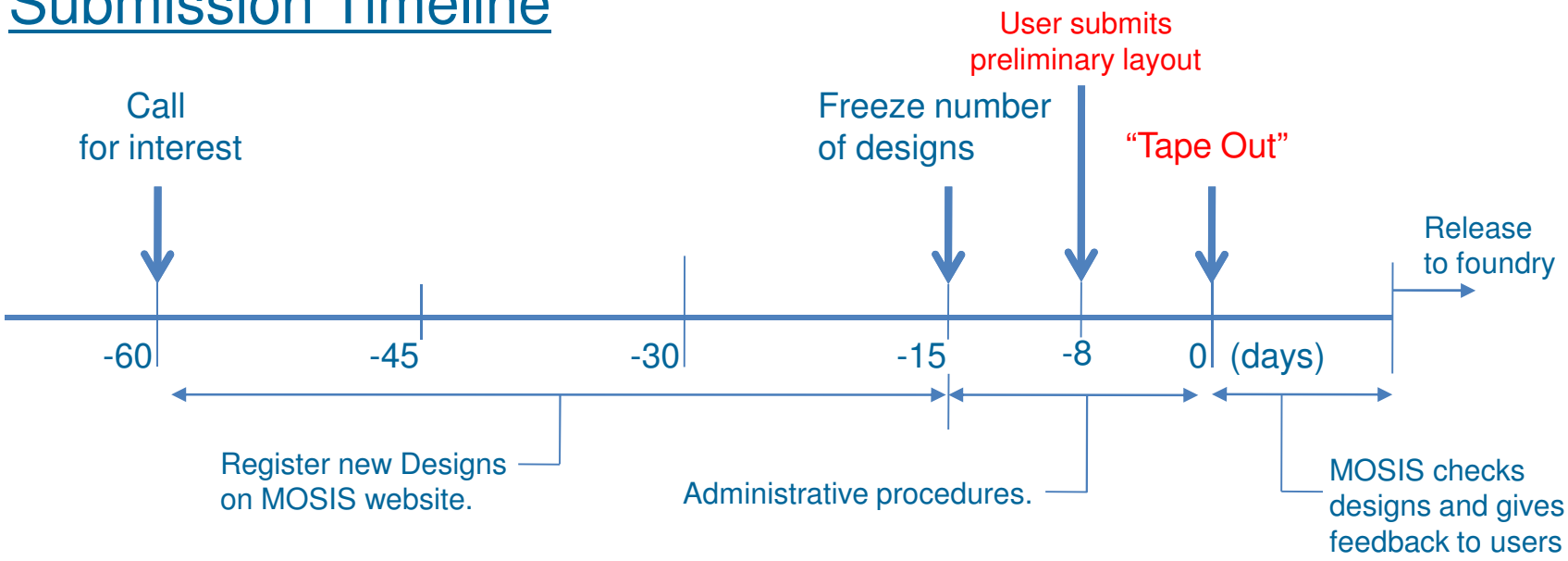
	2009		2010										
	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
CMOS8RF-DM[1]	9			1			10			9			8	
BiCMOS8WL	16			22			24			23			15	
BiCMOS8HP		14		16			17			16			8	
CMOS9LP/RF				22				21				25		

(*) as published on the MOSIS web site: http://www.mosis.com/ibm/ibm_schedule.html
([1]) 8RF-LM 0.13 µm designs can be added to 8RF-DM runs with sufficient advance notice

- Early planning is essential for cost effective prototyping.
- Communicate your submission plans with: Kostas.Kloukinas@cern.ch
- *There are advantages to submit to MOSIS via CERN.*

Fabricating through MOSIS

Submission Timeline



- Turn Around Time: ~70 calendar days from release to foundry
- Number of prototypes: 40 pieces

Access to Technology Data

- Distributed by CERN

Technology	Process	Distributable
CMOS8RF-LM	130nm	IBM PDK, Design Kit
CMOS8RF-DM	130nm	IBM PDK, Design Kit
BiCMOS8WL	130nm (SiGe)	IBM PDK
BiCMOS8HP	130nm (SiGe)	IBM PDK
CMOS9SF	90nm	IBM PDK

- IBM PDK : Physical Design Kit for Analog full custom design.
- Design Kit : Design Kit that supports Analog & Mixed Signal design.