Roadmap for serial powering

Marc Weber, RAL

Power Working Group, TWEPP, Paris 2009

Serial powering elements

What have we done in the last few years?

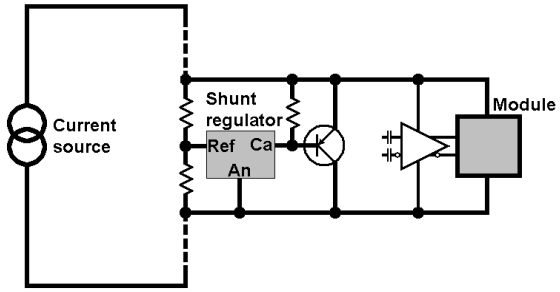
What have we learnt so far ?

Roadmap

Serial powering system elements

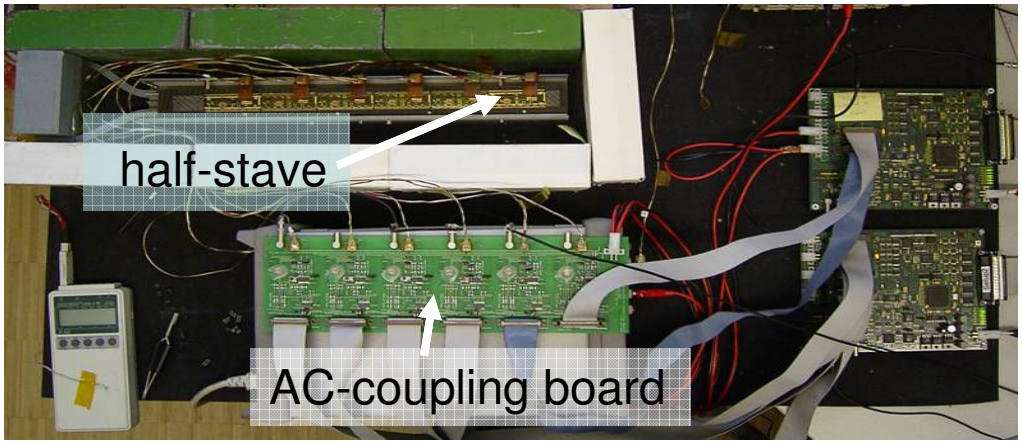
- Shunt regulator/ shunt transistors
- AC coupling
- Protection
- Constant Current Source

- Monitoring and control



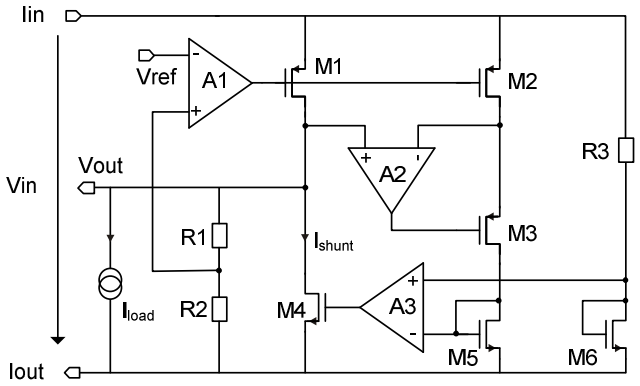
We have chosen to gain practical experience with most elements early on and this was helpful

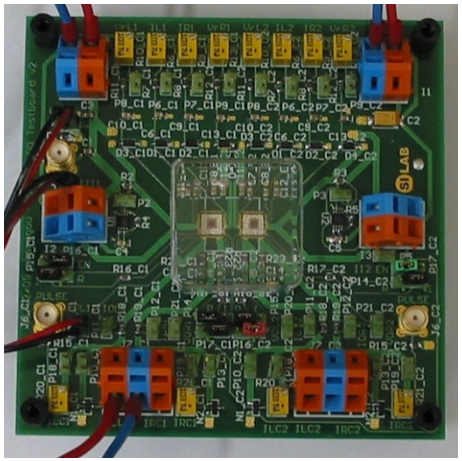
What have we done in the last few years?



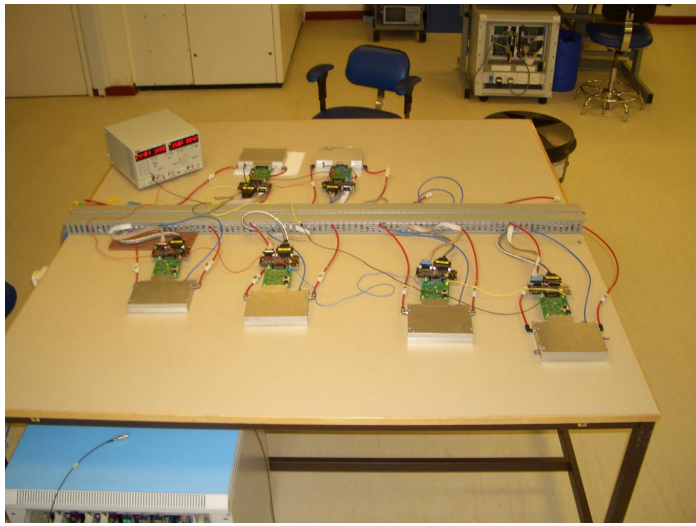
Proof of principle for pixels by Bonn group with custom electronics in FE-I3

D. B. Ta, T. Stockmanns, F. Hügging, P. Fischer, J. Grosse-Knetter, Ö. Runolfsson, N. Wermes, Nucl.Instr. Meth. A557 (2006) 445-459.



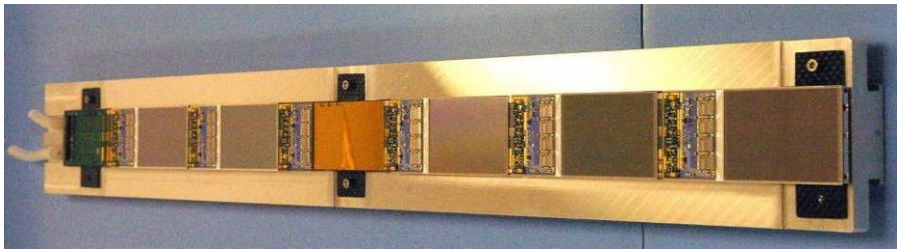


Schematic and test chip of Shunt-LDO in 130 nm for FE-I4 by Bonn (M. Karagounis)

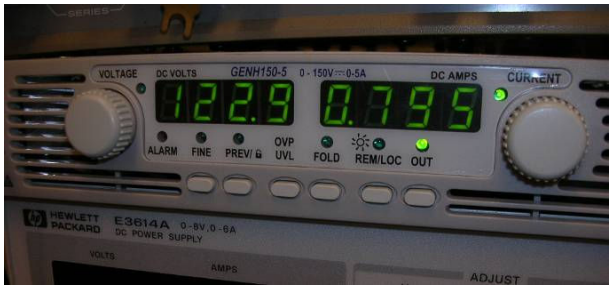


First silicon strip tests at RAL with commercial SP electronics

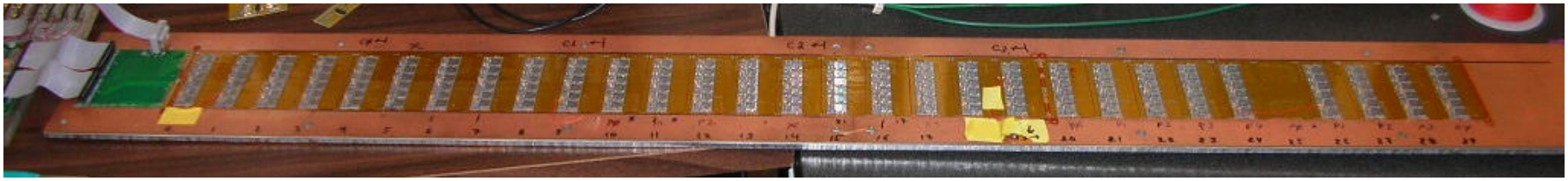
What have we done in the last few years?



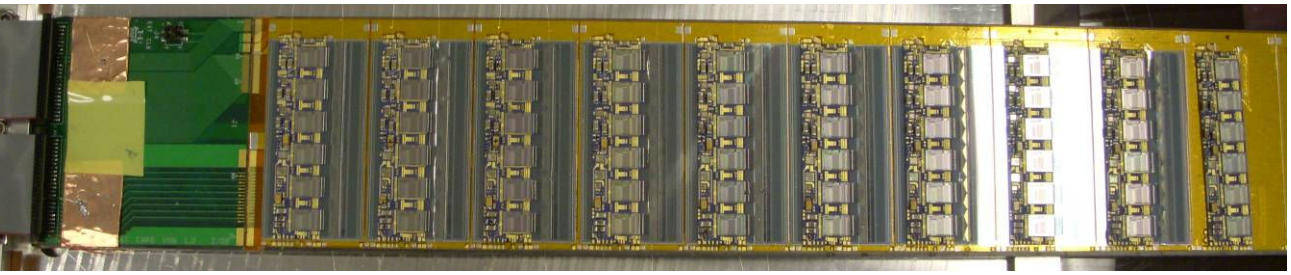
Silicon strip stave 6 module tests at RAL and LBNL

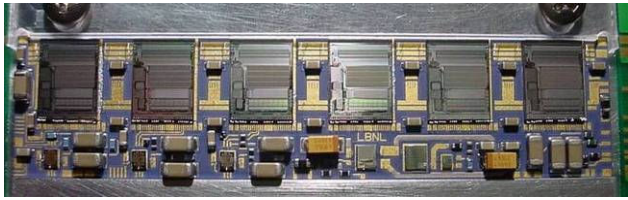


4V x 30 hybrids ~ 120V (0.8A)

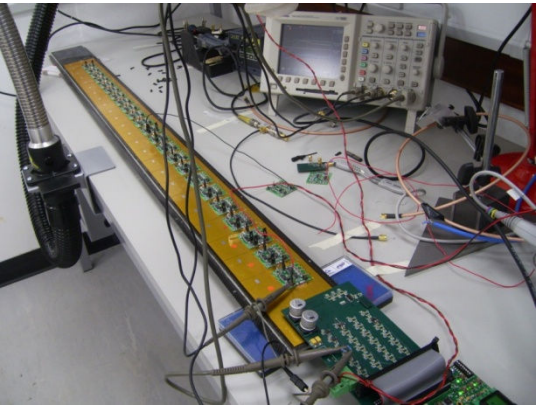


30 hybrid test vehicle and custom hybrid stave at LBNL



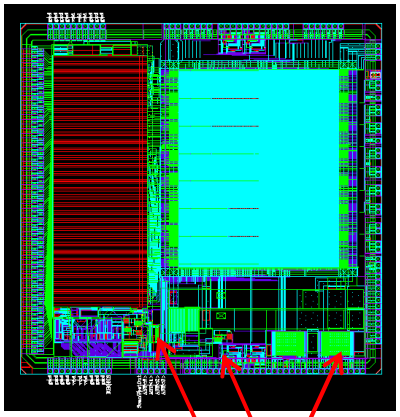


ABCD hybrid with comm. SP

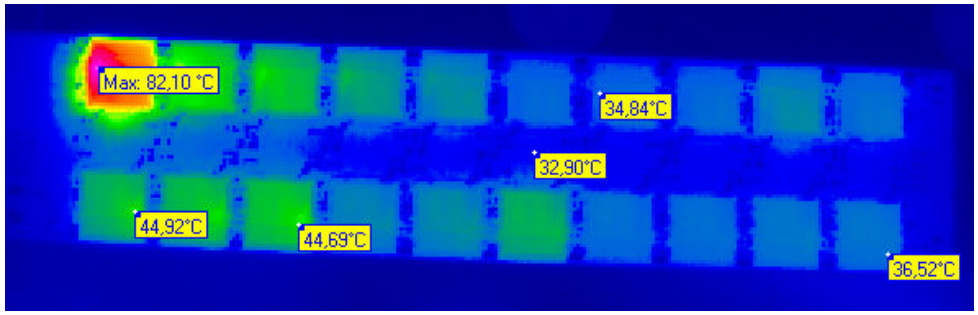


Dedicated AC coupling tests
(Oxford)

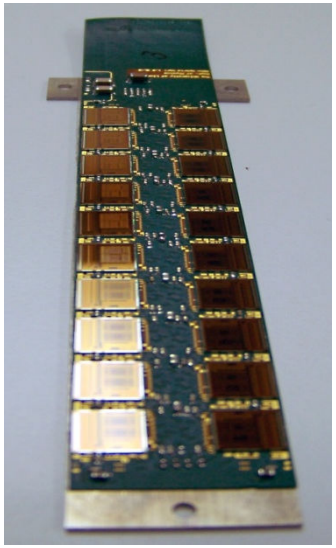
What have we done in the last few years?

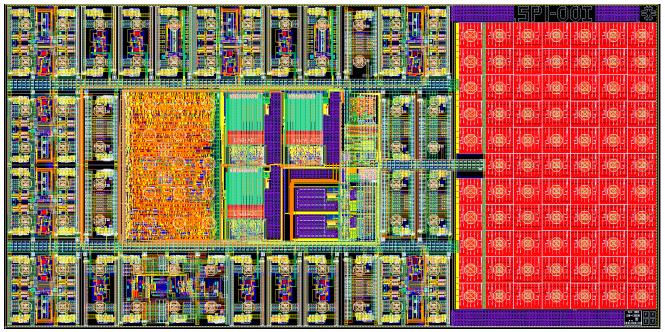


Custom power blocks in ABCN-25



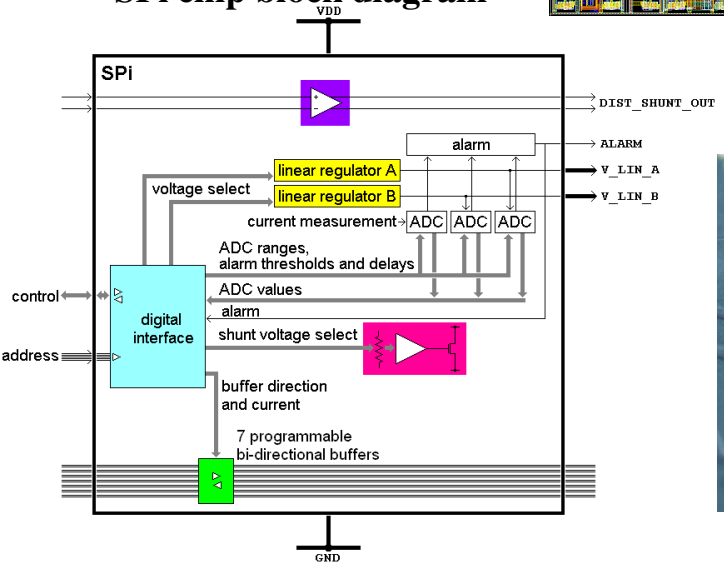
Stress tests of shunt transistors in 20 chip hybrid



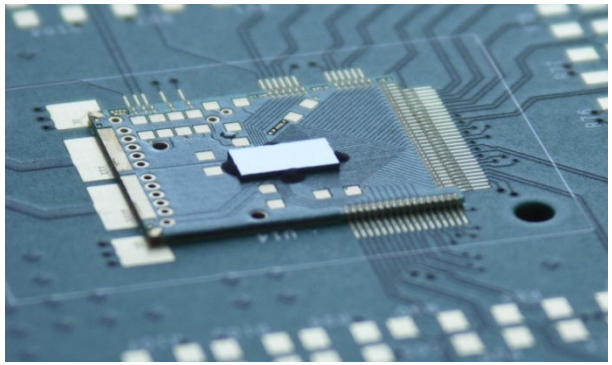


SPi layout (Design M. Trimpl, FNAL and M. Newcomer, Penn)

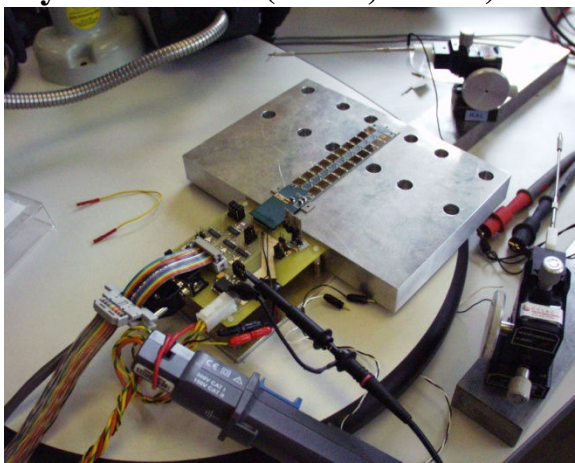
SPi chip block diagram



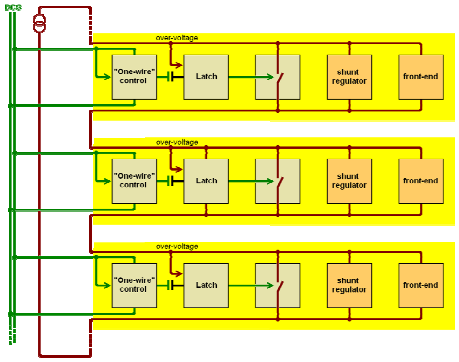
SPi bumped to daughter board on test PCB



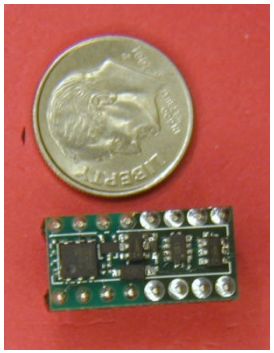
Characterization of 20 ABCN-25 hybrid at RAL (T. Tic, ACSR)



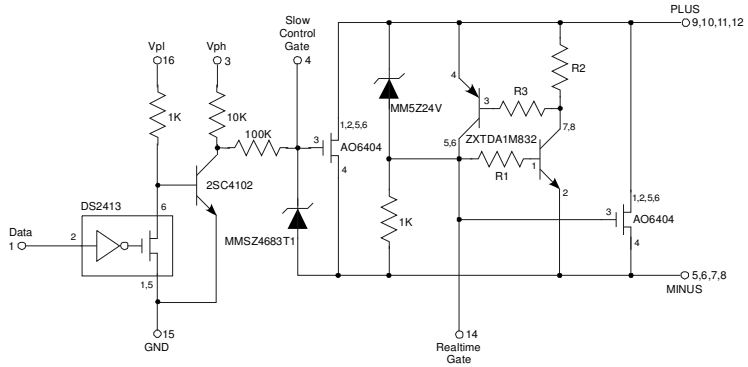
What have we done in the last few years?



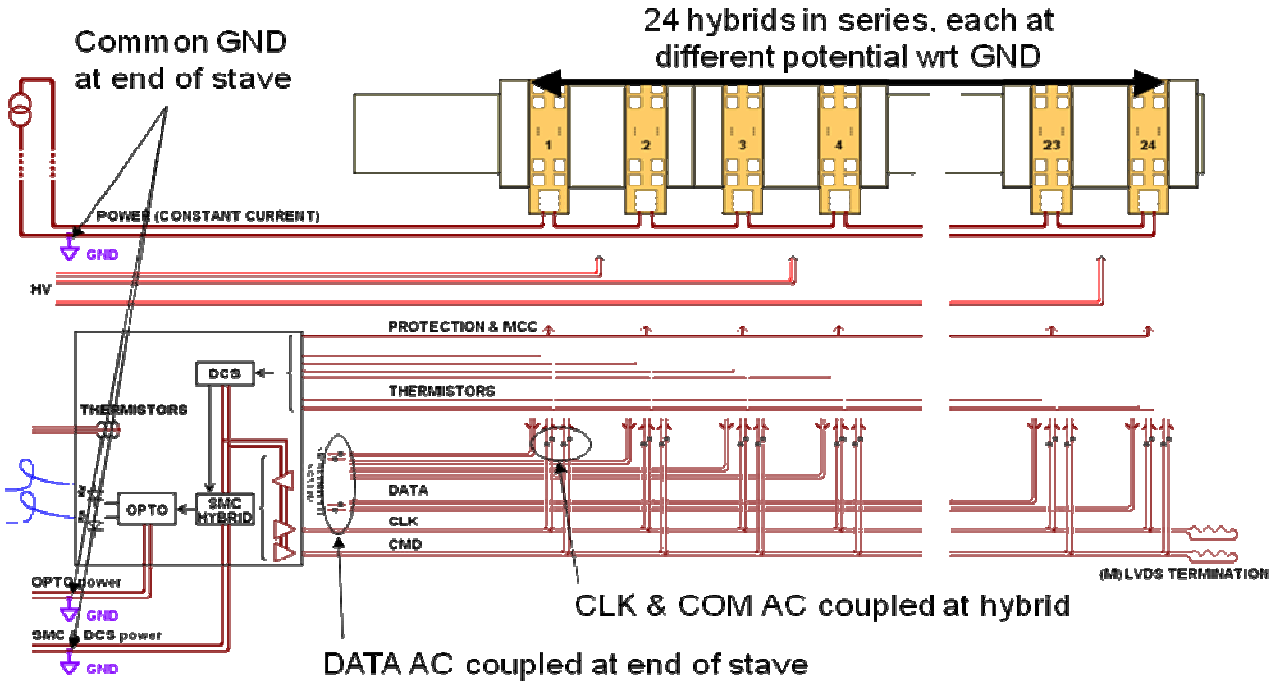
Protection illustration



Discrete protection PCB (BNL)

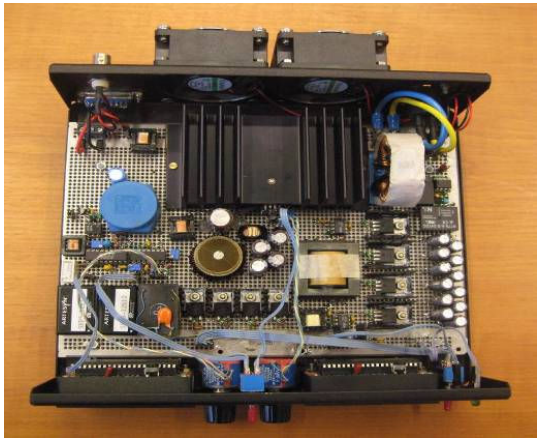


Protection schematic (BNL, Bonn, RAL)



Strip supermodule stave system illustration

Current source prototype (J. Stastny, ACSR)



What have we learnt so far?

Serial powering on pixels is working fine

Noise not an issue (which is welcome news for DC-DC too); pixel staves shorter than strip staves; length of SP chain is ~8 ⇔ high efficiency gain, though less than for strips; however, watch power efficiency of Shuldo scheme

AC-coupling looks fine

I would not exclude having initial difficulties on stavelets; but AC coupling will be trivial with future DC-balanced code; will also be easy with custom SPi or MCC receivers (M. Newcomer)

Know we can build functional custom SP circuitry for strips

Three different architectures in 0.25 um CMOS are all functional (for architectures see slide in appendix); we have gone far beyond the first FE-I3 concepts; we are ready to select favorite architecture and move on to 130 nm

Know how to provide redundant protection

Reached consensus that protection and current by-passing is desirable and practical; convergence on specifications; discrete boards functional; ready to proceed with custom design to miniaturize and realize minimum voltage drops

Grounding and shielding

Have the basic scheme; largely tested with various ABCD stave prototypes

Can bias different sensors from single HV line

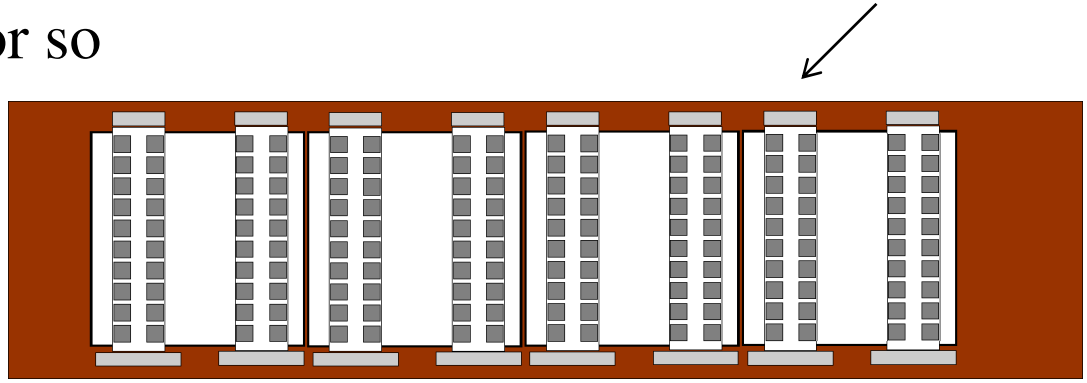
Need this for any module with two hybrids; need to take some care when the first ABCN-25 modules come in, but it will work; if we chose to gang pairs of modules together, we gain the required reduction of HV cables by a factor 2.

Current source

A promising basic prototype is available. Functionality and block diagram for the next iteration have been agreed.

Roadmap. How to best get to final SP system ?

- Consolidate the above with ATLAS stavelets within next ½ year or so



***Stavelets**: short staves with up to 4 integrated sensors on top side (8 hybrids). Precursor of 12+12 module stave09*

The power plug-in concept →

- Reduce options now (or after stavelet test) where possible
- Specify SP system fully, design and prototype all system elements in parallel and build prototypes in 130 nm

This is easier and less involved than it might look;
work has already started

Which SP regulator architecture ?

- W scheme, M scheme or SPi external?
  (i.e. fully distributed, distributed shunts and external regulator, fully external)

- I recommend selecting one of the schemes soon.
  Best in a review, which considers the results of the ATLAS stavelets tests. I just think making a decision soon will get us a better SP system faster.

- The large ABCN-25 hybrid current fluctuations of $\Delta I \sim 1.5$ A probed the 3 schemes much more than expected. The M scheme coped well.

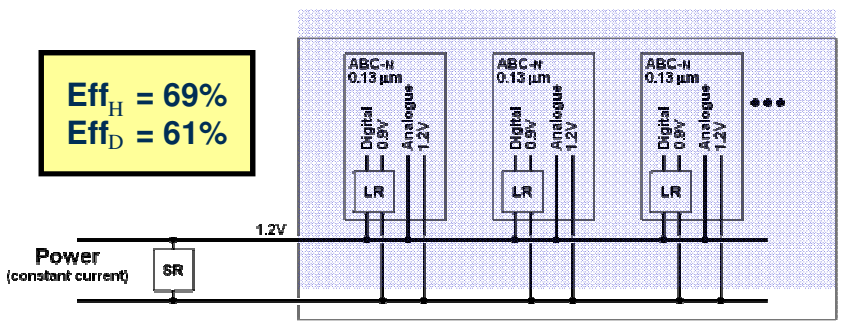
- M scheme is strong candidate for final system (even if current bumps disappear):

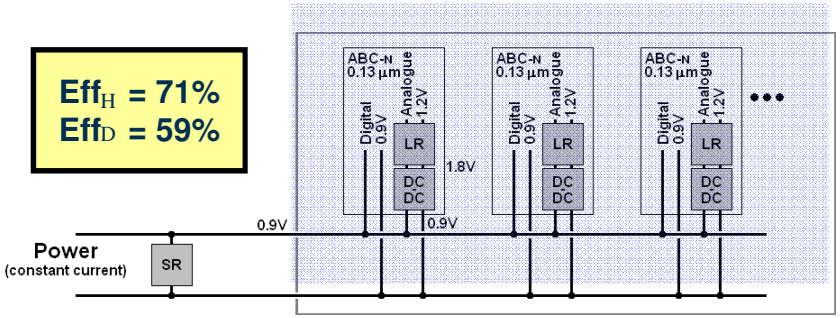
+ it is relatively simple
+ thermally robust, since distributed shunts
+ performs very well today
+ flexible, since feed-back loop is accessible on hybrid
+ no need for external control lines (same for W)
– less redundant than W
– one extra die for shunt op-amp
– couples readout chip and regulator chip unlike SPi

Advantages outweigh the disadvantages in my view

How to derive two voltages efficiently ?

- This is very much an open question for 130 nm (not for 250 nm) and the answer will most probably require prototyping. To be found out: on-chip-efficiency and “noise”.

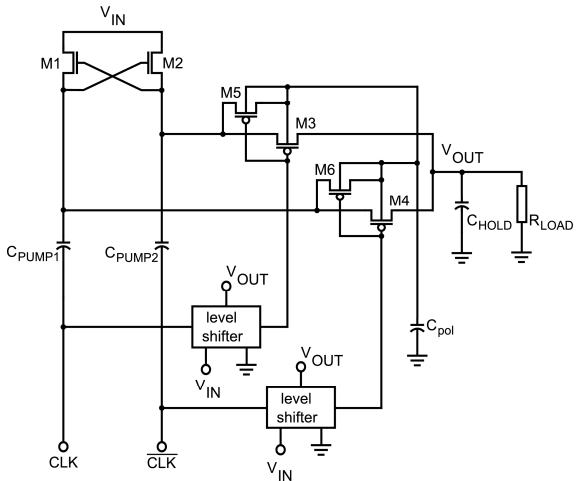


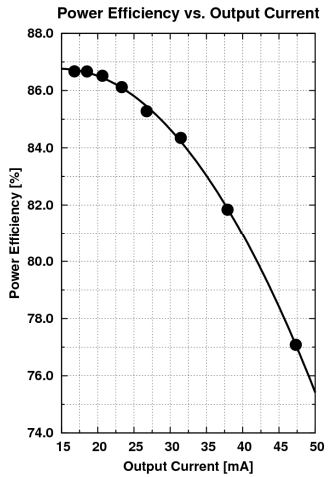


- Two main alternatives are:

  shunt regulator provides **analog, LDO** gives lower **digital voltage**
  shunt regulator provides d**igital, step-up converter** gives higher **analog voltage**

For step-up and down DC-DC converters in 130 nm, see poster of M. Bochenek





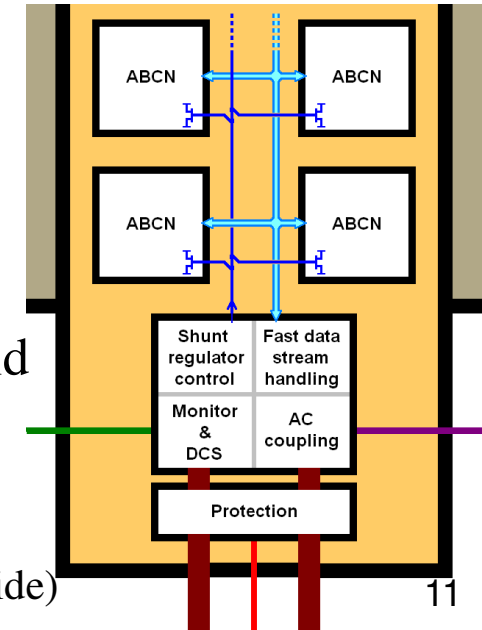
MCC chip specs

Power blocks of ABCN-13: "shunt transistors", LDO(s), possibly DC-DC

- Main function of MCC is data multiplexing and other digital service tasks.
- However, MCC is excellent location for residual powering blocks:

  - shunt op-amp for M scheme
  - AC coupling receivers
  - limited resolution ADCs and IO for monitoring of
    a) global hybrid voltage;*
    b) shunt op-amp output;
    c) hybrid temperature.

- MCC is single point-of-failure even without powering functions. So it make sense to overload it with other crucial functions.
- Should explore schemes with two redundant MCCs/hybrid

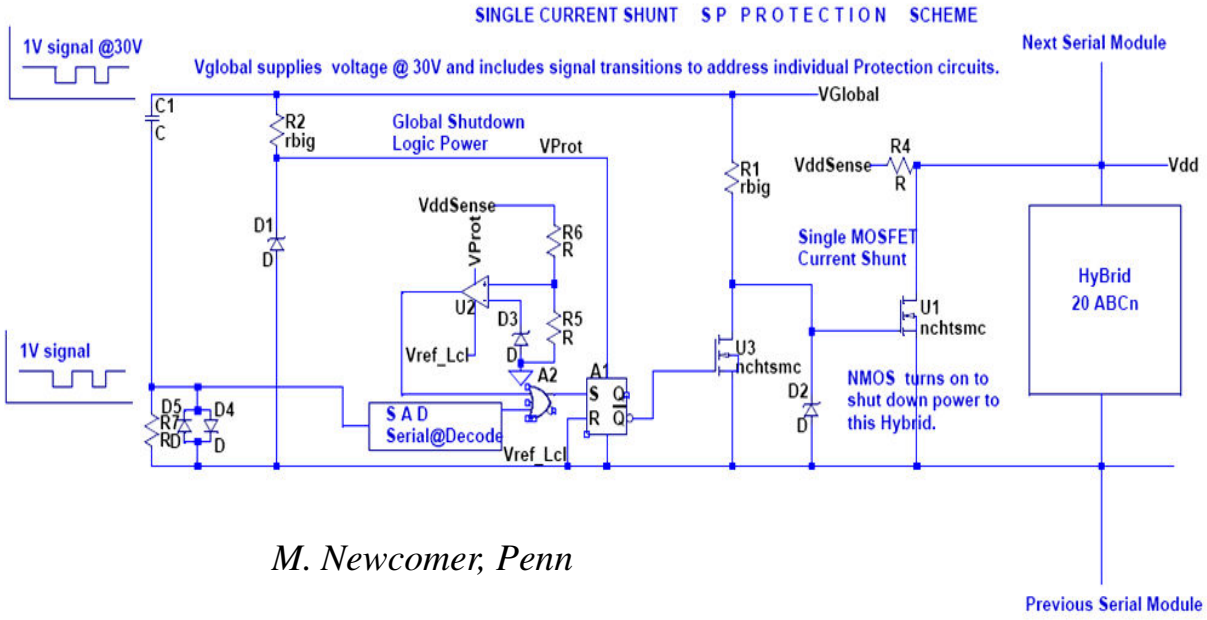


We are ready to define detailed specs of MCC now

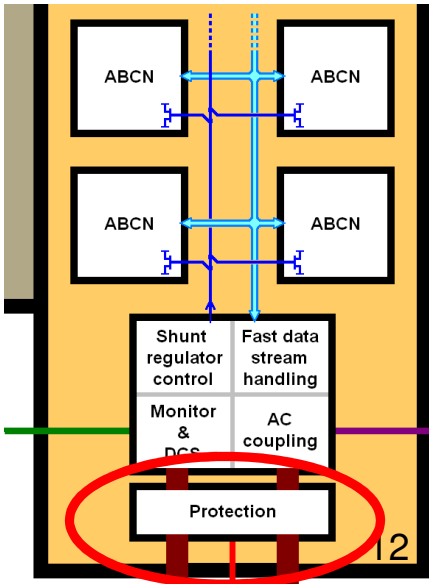
* (digital or analog depending on chosen implementation, see previous slide)

SP protection chip

- Prudent to implement an entirely separate protection and module by-passing function.
- Protection specs have been discussed between BNL, Bonn and RAL.
  A discrete version by BNL is available.
- The custom solution could be placed on or off hybrid. Both solution are plausible.
- The protection itself should not have further redundancy! E.g. it will be enabled by a common protection bus.
- Design in progress. Expect submission in January.

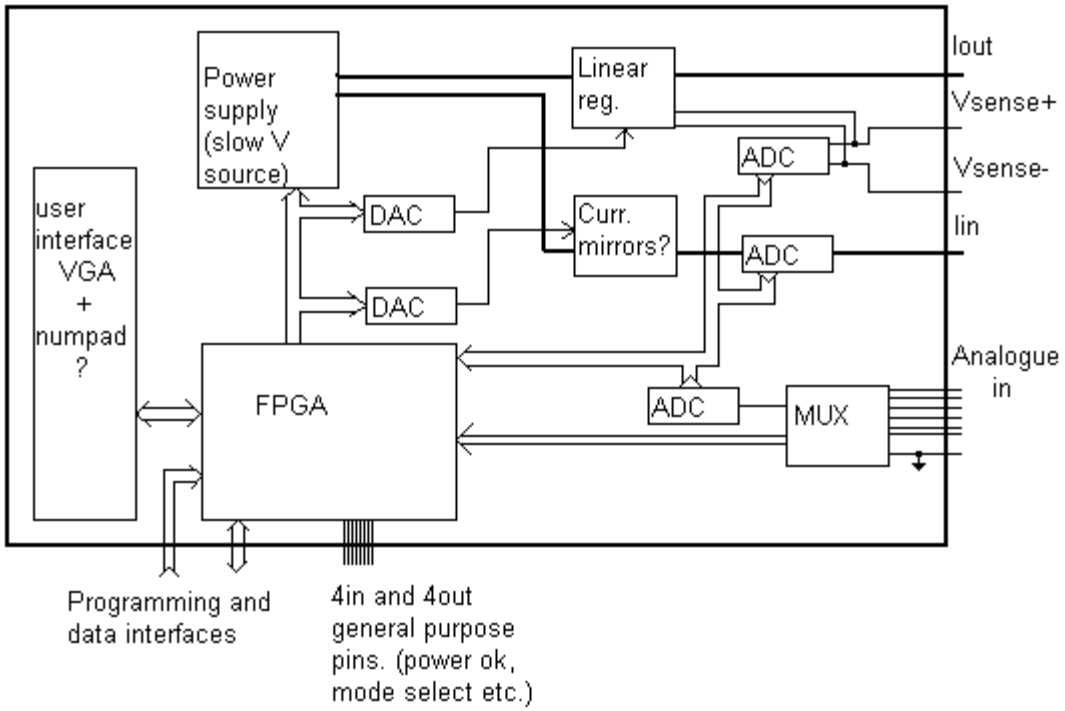


M. Newcomer, Penn



Current source

- "Current-source" design could have been started later, but why wait ?
- Jan has built a great prototype already.
- We decided to make the next iteration more intelligent to be flexible with current bumps, possible protection scenarios, safe ramping up, and to maximize power efficiency.
- We aim to have the first programmable prototype in time for stave09.



Summary

- We have come a long way with serial powering.
- Will consolidate our current knowledge with ATLAS stavelets.
- We are ready to specify and design all components in 130 nm today (I hope and expect 130 nm is the chosen SLHC strip technology)
- Designing all components in parallel is practical. This is the best and most prudent strategy, in my view.
- It will be crucial to find ways to test 130 nm SP electronics in a chain before the full ABCN-13 is available. I think this can be done. (Even if we only have the ABCN-13 front-end with a few digital blocks.)

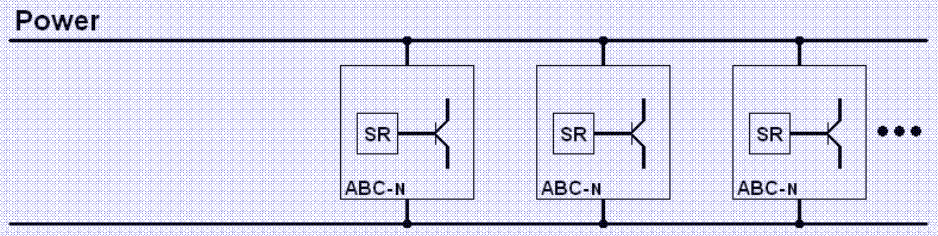
Thank you very much for the good collaboration! It was great fun.

Appendix

ABC-Next Serial powering options

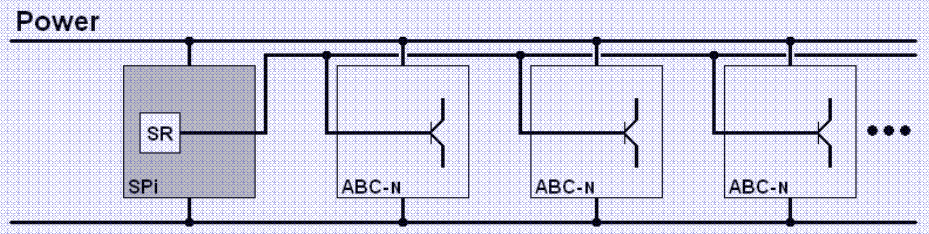
Wladek Dabrowski scheme

Each ABC-N has its own shunt regulator & transistor(s)



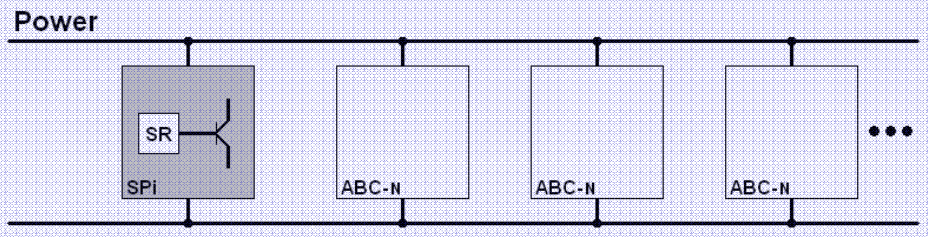
Mitch Newcomer scheme

Just one shunt regulator – Use each ABC-N transistor(s)



SPi-type scheme

Just one shunt regulator and transistor



SR = Shunt regulator
Linear regulators and other connections omitted

Power Requirements with Modern Process Technologies

					Power per 128 channel chip	per channel
In ATLAS SCT	**ABCD** (0.8μm, biCMOS)	Digital:	4.0 volts	35 mA per chip (actual)	=> 4.0 x 35 + 3.5 x 74	
		Analogue:	3.5 volts	74 mA per chip (actual)	= 399 mW	**3.1 mW**
Present Prototype	**ABCN25** (0.25μm CMOS)	Digital:	2.5 volts	95 mA per chip (preliminary)	=> 2.5 x 95 + 2.2 x 27	
		Analogue:	2.2 volts	27 mA per chip (preliminary)	= 300 mW	**2.3 mW**
Proposed	**ABCN13** (0.13μm CMOS)	Digital:	0.9 volts	**51 mA per chip (estimate)	=> 0.9 x 51 + 1.2 x 16	
		Analogue:	1.2 volts	**16 mA per chip (estimate)	= 65 mW	**0.5 mW**

ABCN25: Vdig > Vana Idig >> Iana

If we generate Vana from Vdig using LR:

- 27mA * 0.3V = 8.1mW per chip
- 3% of chip power

ABCN13: Vana > Vdig Idig >> Iana

If we generate Vdig from Vana using LR:

- 95mA * 0.3V = 28.5mW per chip
- **44% of chip power**
- Can we do better than this? *Of course…*

** Power Estimates for an ABCN in 130nm Technology, Mitch Newcomer, Atlas Tracking Upgrade workshop, NIKHEF, November 2008
http://indico.cern.ch/getFile.py/access?contribId=16&sessionId=8&resId=0&materialId=slides&confId=32084

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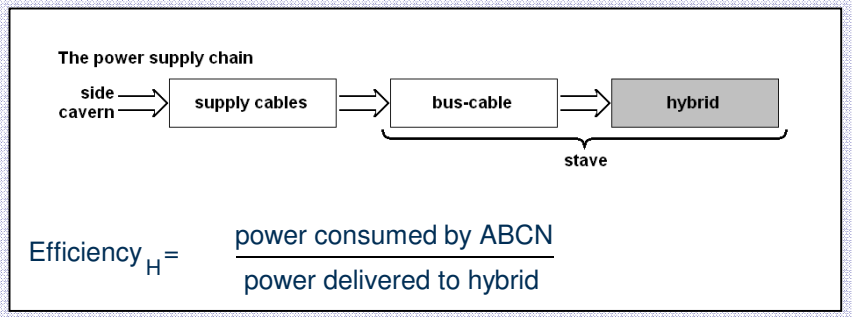
Efficiency - definitions

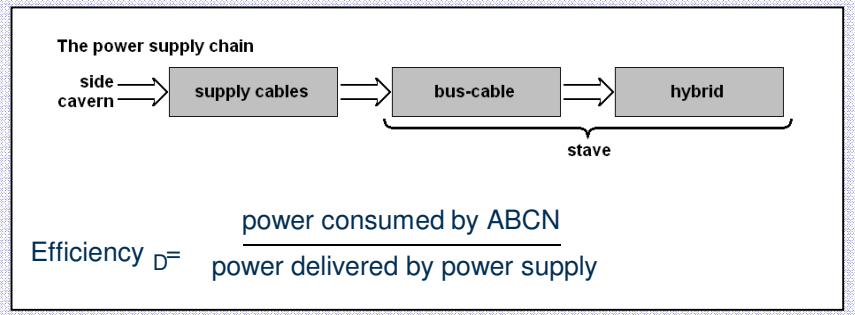
Definition – *Hybrid* (excludes stave interconnects & supply cables)



$$\text{Efficiency}_H = \frac{\text{power consumed by ABCN}}{\text{power delivered to hybrid}}$$

Efficiency$_H$

Definition – *Detector* (includes all supply cables)



$$\text{Efficiency}_D = \frac{\text{power consumed by ABCN}}{\text{power delivered by power supply}}$$

Efficiency$_D$

Some assumptions: Cable resistance 2 ohms for each line pair, SR = 85%, low current DC-DC = 90%, high current DC-DC = 85%

ABCN demand power is dependant on task. This will normally mean a shunt regulator will dissipate some power to maintain voltage under all conditions.

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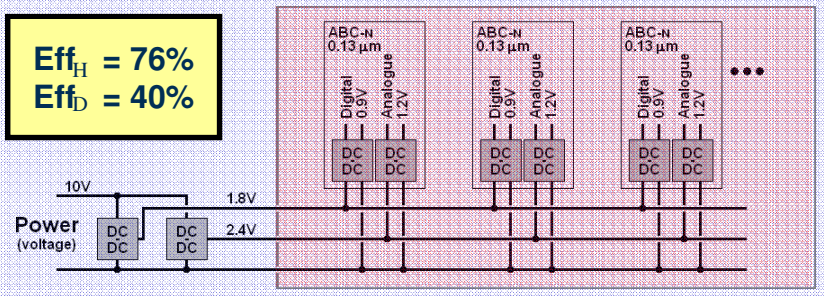
For the sake of Comparison…

Off-chip DC-DC conversion from 10V to 2.4V and 1.8V (assume 85% efficiency)

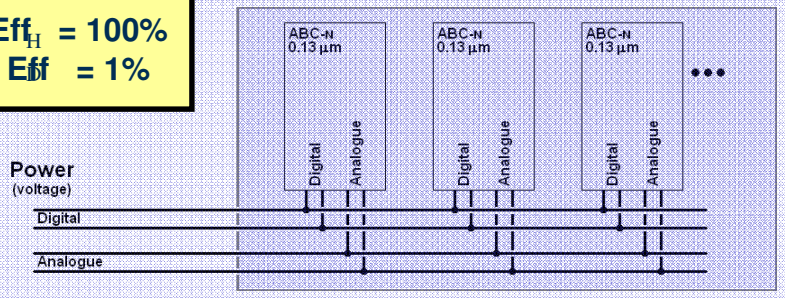
"On-chip" DC-DC conversion using switched capacitors (assume 90% efficiency)

Eff_H = 76%
Eff_D = 40%



Independent Power

Eff_H = 100%
Eff_D = 1%



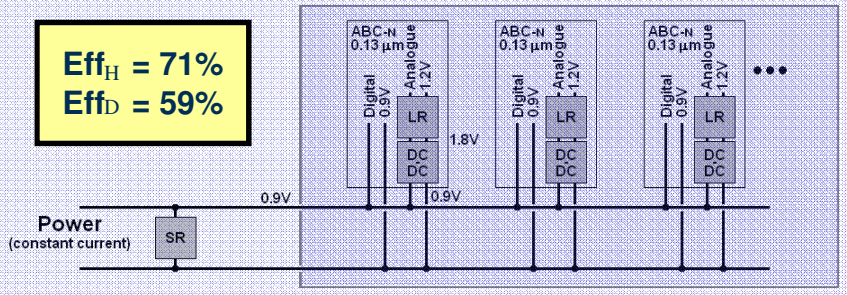
With ABCN in 130 nm technology, we shall study several options to obtain the best balance between efficiency and performance…

Favoured SP Options

Also Low Noise:

Analogue from on-chip DC-DC step using switched capacitors *and* linear regulator

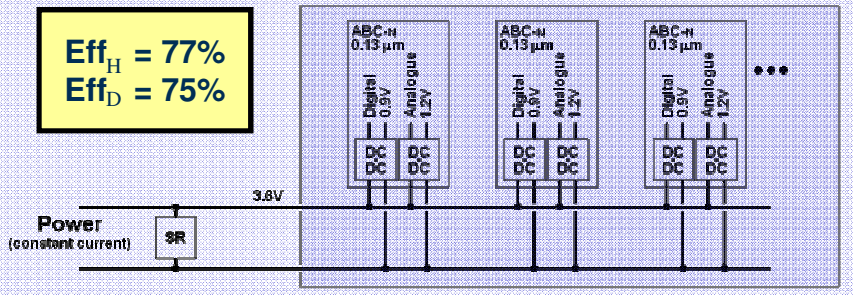
Eff_H = 71%
Eff_D = 59%



Highest Efficiency:

"On-chip" DC-DC conversion using switched capacitors. Only for illustration, not a practical option as such.

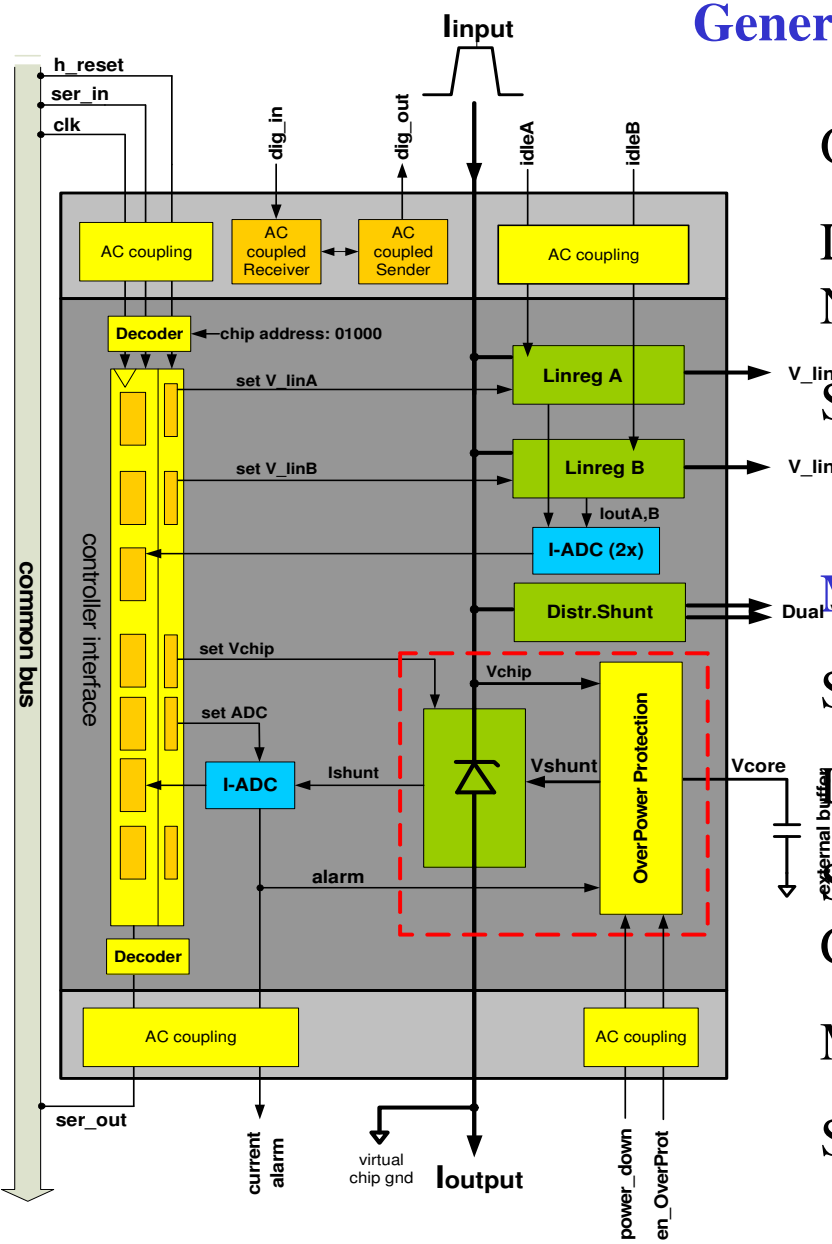
Eff_H = 77%
Eff_D = 75%



For further details, see this afternoon's presentation by W. Dabrowski: "Serial power circuitry in the ABC-Next and FE-I4 chips"

SPi chip

General purpose SP interface



Overall layout and design: Marcel Trimpl, FNAL

LVDS comports and stand-alone SR: Mitch Newcomer and Nandor Dressnandt, Penn

Specification and KE: Giulio Villani, RAL

Main blocks and features:

Shunt regulator(s) and shunt transistors;

LVDS buffers; over current protection;

Shunt current sensing ADC; TSMC 0.25µm CMOS with almost rad-hard layout;

Max. shunt current: 1 A design, “expected” >3 A;

Size: ~ 14 mm^2; flip-chip