DIRAC v2: a DIgital Readout Asic for hadronic Calorimeter

R. Gaglione[ab], C. Adloff[b], M Chefdeville[b], C. Drancourt[b], G Vouters[b]

[a] IPNL, Université de Lyon, Université Lyon 1, CNRS/IN2P3, France / MICRHAU

[b] LAPP, Université de Savoie, CNRS/IN2P3, France

gaglione@lapp.in2p3.fr

Abstract

DIRAC is a 64 channel mixed-signal readout integrated circuit designed for Micro-Pattern Gaseous Detectors (MICROMEGAS, Gas Electron Multiplier) or Resistive Plate Chambers. These detectors are foreseen as the active part of a digital hadronic calorimeter for a high energy physics experiment at the International Linear Collider. Physic requirements lead to a highly granular hadronic calorimeter with up to thirty million channels with probably only hit information (digital calorimeter). The DIRAC ASIC has been especially designed for these constraints. Each channel of the DIRAC chip is made of a 4 gains charge preamplifier, a DC-servo loop, 3 switched comparators and a digital memory, thus providing additional energy information for a hit. A bulk MICROMEGAS detector with embedded DIRAC v1 ASIC has been built. The tests of this assembly, both in laboratory with X-Rays and in a beam at CERN are presented, demonstrating the feasibility of a bulk MICROMEGAS detector with embedded electronics. The second version of the ASIC, with improved noise and additional functionalities, has been tested on bench and characterisation is detailed, and foreseen associated detectors are presented.

I. Digital Hadronic Calorimeter at the International Linear Collider

MICRO MEsh GAseous Structure (MICROMEGAS [1]), Gas Electron Multipliers and Resistive Plate Chambers detector are three candidates for the active part of a Digital Hadronic CALorimeter (DHCAL) for a high energy physics experiment at the International Linear Collider. Physics requirements lead to a highly granular hadronic calorimeter with up to thirty million channels with probably only hit information (digital calorimeter).

To validate the concept of digital hadronic calorimetry, a 1 m^3 technological prototype, made of 40 planes of 1 m^2 each will be built.

Such a technological prototype involves not less than 400 000 electronic channels, thus leading to the development of DIRAC ASIC.

A. Detectors signals

Table 1 shows the signal characteristics of the three foreseen gaseous detectors. MICROMEGAS and GEM have slightly the same amplitude, whereas RPC, which have much higher gain, provide ten times more charges than Micro Pattern Gaseous Detectors. This implies different dynamic ranges in the ASIC.

Although they have different shapes, the signal bandwidth are very close, the detector capacitances are similar, so they can be handled by the same preamplifier.

Table 1: Signal characteristics of foressen detectors

	MICROMEGAS	GEM	GRPC
Charge	1–100 fC	1–100 fC	0.1–10 pC
C_{det} (1 cm^2)	60 pF	60 pF	60 pF
t_r	<2 ns	<2 ns	<2 ns
Pulse width	complex shape	20 ns	20 ns

B. Collider timing

In addition to detector's signals, ASIC must fit with beam timings. The beam is composed of bunch-crossing trains every 200 ms (Figure 1). Inside trains, bunch-crossing are periodical, according to Table 2 [2]. As the data rate for the HCAL is foreseen to be low (1 hit per channel per train), raw data will be held in front-end memory during trains, and read by data acquisition system between train. Thus, no trigger decision is needed for front end. Additionally, to save electrical power, the analog front-end will be shut down outside trains, with a ratio lower than 1%.

Table 2: ILC beam train timing characteristics

	Minimum	Nominal	Maximum
Bunchs # per train	1320	2625	5120
Bunchs period (ns)	189	369	480
Train length (µs)	250	1000	2500
ON/OFF ratio (%)	0.1	0.5	1.25
Rate (Hz)		5	

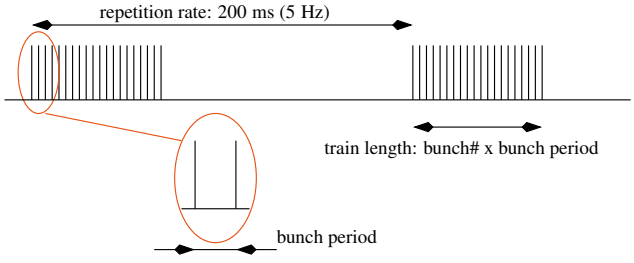

Figure 1: ILC beam structure

II. DIRAC v2 ASIC

DIRAC ASIC have been specifically designed to comply with ILC DHCAL requirements, for both Micro Pattern Gaseous Detectors in one hand and for Resistive Plate Chamber one the other hand.

A chip is made of 64 channels, divided into 2 banks of 32 channels. Each channel is made of a gated integrator with four dynamic ranges (50, 100, 200 fC or 10 pC), a baseline restorer and three comparators. Thresholds are common for a bank of 32 channels, and each threshold is set by a 8-bit DAC, so they are six DAC inside the chip. The 2-bit result of the comparison is stored into a 8-event depth memory and stamped with a 12-bit bunch identifier. Additionaly, each channel has a trigger masking bit. A multiplexed analog readout has been implemented for fine detector measurements. A detailed schematic of the architecture of the second version of this chip is given in Figure 2.

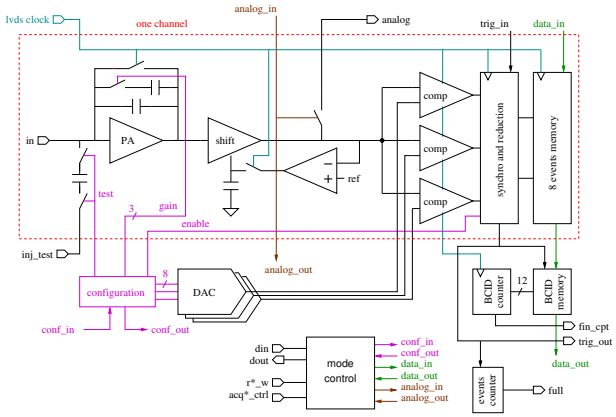

Figure 2: DIRAC v2 architecture

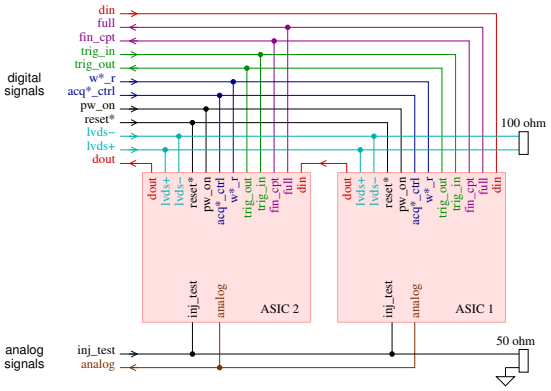

Figure 3: Daisy chain of several ASIC

During the bunch crossing, the gated integrator, synchronized on LVDS clock acquires signal from detector, and, at the end of this period, the measured charge is compared to the threshold and the result stored. Outside trains, the analog front-end is shuted down, the memory emptied and, if needed, configuration performed.

Configuration and readout are LVCMOS serial digital signals, and output flag are open-drain signals. Thus, several ASICs may be chained (Figure 3) to equip a large area detector.

All the pins for digital I/O and daisy chaining are on the left side of the die (Figure 4), the analog power supplies, external voltage references and bias are on the right side, detector inputs are on the lower and upper part of the die. This allows to simplify the PCB routing, as it is a part of the gaseous detector. The dimensions of the die are only 1.6 mm×4.8 mm, and the chosen technology is Austriamicrosystem 0.35 µm CMOS process.

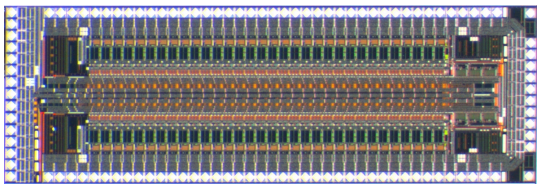

Figure 4: Die photography of DIRAC v2

III. ASIC TESTS

A. Bench

The layout of this testboard is as close as possible to the future detector boards. The acquisition chain used to test DIRAC v2 ASIC consists of a PC with a Labview software, linked with USB connection to a CALICE HCAL DIF [3] board, providing state machine and clock generation for ASIC thanks to FPGA, an intermediate board, which provides reference voltages (will be used in future for detector biasing) and finally the test board, with a socket to insert the ASIC on one side, and 64 anodes, 1 cm^2 each, to simulate detector capacitance.

B. Procedure

It is important to characterize each of the five received prototypes and measure dispersions, to check if individual channel and/or chip calibration will be compulsory for the foreseen digital calorimeter. Thus, for each channel, each comparator has to be checked, and some figure of merit to be extracted to verify comformity. The choosen figure of merit are the gain and the pedestal of each comparator, and the linearity error. The same methodology will be used in production to verify if each ASIC meets the specifications:

- Measure trigger efficiency *vs* thresholds (t) for different input charge (q);
- For each input charge, extract s-curves and fit it with a Fermi-Dirac distribution:

$$S(t,q) = \frac{max}{1 + e^{\frac{t-\mu(q)}{w}}} \qquad \begin{array}{rcl} max & : & \text{maximum efficiency} \\ \mu & : & \text{inflexion point abcisse} \\ w & : & \text{inflexion slope} \end{array}$$

One example of s-curve and fit, for an injected charge of 60 fC can be seen in Figure 5. Then, the linearities can be plotted:

- $M(\mu(q))$: μ *vs* input charge for each channel;

- Linear fit:

$$F(q) = 1/g \cdot q + b \qquad \begin{array}{rcl} g & : & \text{gain} \\ b & : & \text{pedestal} \end{array}$$

- Linearity error: $\frac{F-M}{M}$ normalized in %.

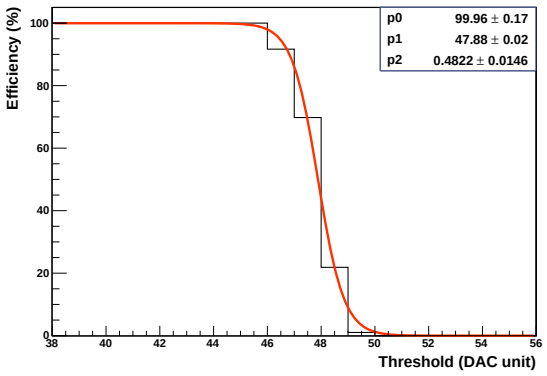

Figure 5: Example of s-curve

Input charge is injected with a GPIB controlled pulse generator delivering a voltage pulse to on-chip 1 pC test capacitor through -20 dB attenuator. All data are collected to PC thanks to Labview software, and analyzed offline with a ROOT/C++ framework.

C. Results

The characterisation of DIRAC v1 has been described in details in [4].

DIRAC v2 brings some improvements to these results: Table 3 gives results of a gaussian fit for gain and pedestal distribution for the five prototypes. These values are good enough to avoid any channel to channel ASIC calibration in the calorimeter.

The linearity is within +1/-3% on the 20–200 fC range.

The noise, extract from s-curve, is the width from 100% efficiency to 0% efficiency. At 5σ, the noise is less than 5 fC.

The minimum threshold is less than 10 fC which corresponds to half of the most probable signal from minimum ionising particles in MICROMEGAS detectors developped at LAPP.

Moreover, a power-on time less than 3 µs has been measured. To obtain this result, efficiency and inflexion point of the s-curve have been observed in function of the power-on time.

Table 3: Prototype dispersion summary

Chip ID		1	2	3	4	5
Gain (fC/DACU)	mean	1.1	1.0	1.1	1.0	1.1
	sigma	0.03	0.03	0.02	0.02	0.02
Pedestal (fC)	mean	6.2	4.0	6.7	6.9	5.6
	sigma	2.0	1.6	1.8	1.6	1.7

[1] In a DHCAL, this cover will be a part of the calorimeter absorber.

IV. ASIC EMBEDDED IN MICROMEGAS CHAMBER

To minimize shower leakage and minimize HCAL diameter, the thickness of the active medium must be thinner than 8 mm. In that respect, the Bulk MICROMEGAS is an attractive option as the fabrication process allows a PCB with front end ASICs soldered on one side, and anode pads patterned on the other side to be equipped with a MICROMEGAS mesh. This is crucial for the construction of a real scale DHCAL for which large areas should be instrumented and dead zones minimized to insure a good hermeticity of the HCAL.

A MICROMEGAS detector consists of a gas volume separated in a drift and an amplification region by a thin mesh. An industrial technology, called bulk [5] has been chosen. The drift region is defined by a 3 mm thick resin frame manufactured by stereolithography. This frame also provides gas inlet and outlet. The drift electrode (cathode) is made of a 5 µm thick copper foil and a 75 µm Kapton insulator, glued together on a 2 mm thick steel plate, which is the MICROMEGAS chamber lid[1]. The amplification electrode consists of a woven mesh of stainless steel wires (18 µm diameter, 56 µm pitch) maintained by insulating pillars patterned by photolithography (400 µm diameter) at precisely 128 µm of the anodes. This technology has been chosen for its performances (especially near 100% efficiency for MIP), its robustness [6][7] and its ease of industrialisation in a PCB workshop (big amount of detectors and large areas are expected in the future). A cut view of the detector is presented Figure 6.

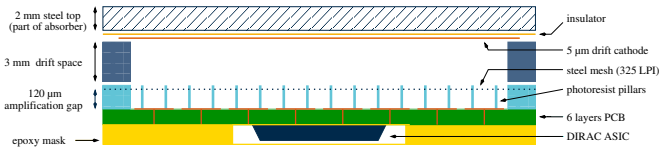

Figure 6: Micromegas with embedded ASIC

The first tests are made with an X-ray source (^{55}Fe) thanks to a small hole in the lid of the chamber. The energy resolution is measured and the gain of the detector *vs* high voltage is checked (Figure 7). The pedestal is at 5 ADC counts, the photopeak at about 770 (σ=63). This gives an energy resolution σ_E/E of 8.5% at 5.9 keV. A typical gain is 10^4 for a -420 V mesh voltage.

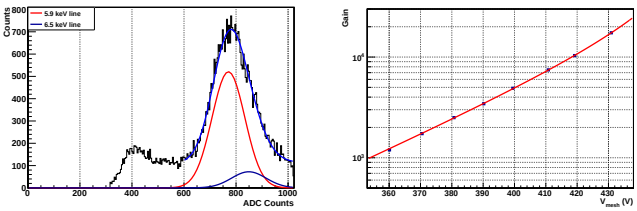

Figure 7: Detector characterisation

This chamber has been tested in a 200 GeV pion beam at the CERN/SPS [8]. A drift cathode voltage of 460 V and a mesh

voltage of 410 V have been used. Thresholds have been set to 24, 40 and 80 DAC code (respectively to 19, 32 and 64 fC). Figure 8 shows the beam profile in hit counts.

The measured hit multiplicity (mean number of pad hit for each trigger) is 1.10. This is in very good agreement with previous measurements performed with analog readout prototypes of same chamber geometry [9] [10].

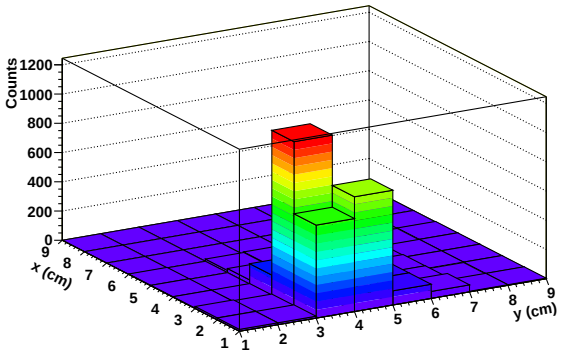

Figure 8: Beam profile

V. Future improvement

Recent physics simulation may indicate that the lowest threshold for a DHCAL should be around 1 MIP-MPV. However, a 97% efficiency for the detector invloves a minimum threshold of 1.3 fC. Thus, to perform further R&D on the micromegas detector, a new preamplifier is needed, with improved gain, improved bandwidth, and improved noise, and without rising the power consumption too much. An improved design, presented Figure 9 has started. The difference with the first version are a gain boost stage, a cascoded current source (I2) and a voltage follower at the output. With I1=200 µA, I2=20 µA, I3=I4=10 µA, the preliminary simulation results give a gain of 108 dB, a bandwidth of 8 kHz, and a gain-bandwidth product of 2 GHz. The phase margin is 72° and the minimum phase (in the bandwidth) of 51°. With no increase in the bias current, the rms noise is 2.2 mV with C_{det}=60 pF. This value will be improved with increase of I1.

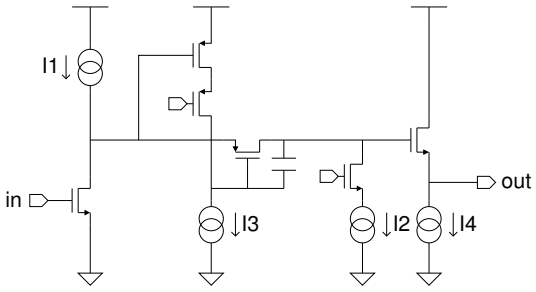

Figure 9: Preamplifier schematic

VI. Conclusion

The construction of a bulk MICROMEGAS chamber with embedded ASIC has been demonstrated by producing and testing a first prototype equipped with a DIRAC v1 chip. The second version of DIRAC ASIC is currently under characterisation. Further measurements of detection efficiency and hit multiplicity are foressen to assess in more details the performance of DIRAC based MICROMEGAS chambers. For that purpose, four chambers of small size (8×8 cm^2) are well suited and are currently under development. These measurements will be performed with beam at CERN.In parralel, the design of medium area PCB (32×48 cm^2) has began to build a 1 m^2 MICROMEGAS chamber.

VII. Acknowledgments

DIRAC v1 preamplifier has been designed by H. Mathez, acquisition board by C. Girerd and acquisition sofware by C. Combaret. The mask and the mesh lamination have been performed at CERN by R. De Oliveira and his TS/DEM group. Chamber design, assembly, handcrafting and tests have been conducted at LAPP by the LC-Detector group. Special thanks are addressed to F. Peltier for his involvement in the detector assembly.

VIII. References

References

[1] I. Giomataris, P. Rebourgeard, J.-P. Robert, G. Charpak, *MICROMEGAS: A high-granularity position-sensitive gaseous detector for high particle-flux environments*, doi:10.1016/j.nima.2005.12.222, *NIM-A* **376-1** 29–35, June, 21, 1996.

[2] C. Adloff *et al.*, *International Linear Collider Reference Design Report*, ILC Global Effort and World Wide Study, October, 2007.

[3] CALICE wiki: https://twiki.cern.ch/twiki/bin/view/CALICE/DetectorInterface

[4] R. Gaglione and H. Mathez, *DIRAC: a Digital Readout Asic for hAdronic Calorimeter*, in *IEEE-NSSS conference record*, October, 19–25, 2008, Dresden, **1** 1815-1819.

[5] I. Giomataris, R. De Oliveira *et al.*, *MICROMEGAS in a bulk*, doi:10.1016/j.nima.2005.12.222, *NIM-A* **560-2** 405–408, May, 10, 2006.

[6] P. Baron *et al.*, *Large bulk-micromegas detectors for TPC applications in HEP*, in *IEEE-NSSS conference record*, October, 27–28, 2007, Honolulu, **6** 4640–4644.

[7] T. Alexopoulos *et al.*, *Development of large size Micromegas detector for the upgrade of the ATLAS Muon system*, doi:10.1016/j.nima.2009.06.113, *NIM-A* in press.

[8] R. Gaglione, C. Adloff, M. Chefdeville, A. Espargilière, N. Geffroy, Y. Karyotakis and R. De Oliveira, *A MICROMEGAS chamber with embedded DIRAC ASIC for hadronic calorimeter*, First Conference on Micro-Pattern Gaseous Detectors proceedings, Kolympari, Crete, Greece, June, 12–15, 2009, *JINST* in press.

[9] C. Adloff, A. Espargilière, Y. Karyotakis, *Large surface MicroMegas with embedded front-end electronics for a digital hadronic calorimeter*, in *IEEE-NSSS conference record*, October, 19–25, 2008, Dresden, **1** 1433-1435.

[10] C. Adloff, J. Blaha, M. Chefdeville, A. Dalmaz, C. Drancourt, A. Espargilière ,R. Gaglione, R. Gallet, N. Geffroy, J. Jaquemier, Y. Karyotakis, F. Peltier, J. Prast, G. Vouters, D. Attié, P. Colas, I. Giomataris, *MICROMEGAS chambers for hadronic calorimetry at a future linear collider*, `arXiv:0909.3197`, *JINST* in press.