

DIRAC v2: a Digital Readout Asic for hadronic Calorimeter

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The first version of this chip has been tested in beam last year on a detector, thus proving the feasibility of Micromegas with embedded digital readout.

Summary

This mixed-signal circuit is a 64 channels readout R&D ASIC for Micro-Pattern Gaseous Detectors (Micromegas, Gas Electron Multiplier) or Resistive Plate Chambers. These detectors are foreseen as the active part of a digital hadronic calorimeter for a high energy physics experiment at the International Linear Collider. Physics requirements lead to a highly granular hadronic calorimeter with up to fifty millions channels with probably only hit information (digital calorimeter).

Each channel of the chip is made of a 4 gains charge preamplifier, a DC-servo loop, 3 switched comparators and a digital memory, thus providing additional energy information for a hit. For detector characterization, a multiplexed analog readout has been implemented.

Configuration and readout are fully digital, indeed six 8-bit DACs are embedded to set comparators thresholds. Power-down circuitry has been included, decreasing the power consumption to 10 μ W per channel. To achieve a low cost electronics, a cheap full CMOS 0.35 μ m foundry process has been chosen and the floorplan has been designed to reduce Printed Circuit Board costs.

The SPS beam tests of the DIRAC first version embedded in a bulk Micromegas will be presented. The second version has just been received and preliminary results will be detailed. Large area detectors equipped with these chips are planned to be put in the PS beam this year.

Author: Dr GAGLIONE, Renaud (LAPP, Université de Savoie, CNRS/IN2P3)

Presenter: Dr GAGLIONE, Renaud (LAPP, Université de Savoie, CNRS/IN2P3)

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