SPi test results

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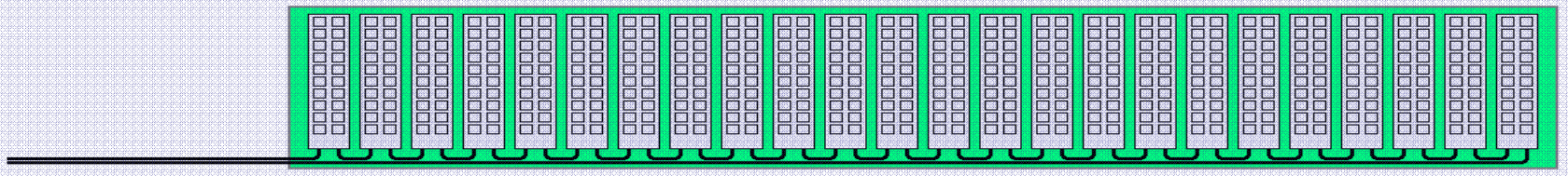
SPi introduction

SPi = "Serial Powering interface"

ASIC with many flexible features to enable serial powering and data interfacing

One SPi on each SCT hybrid



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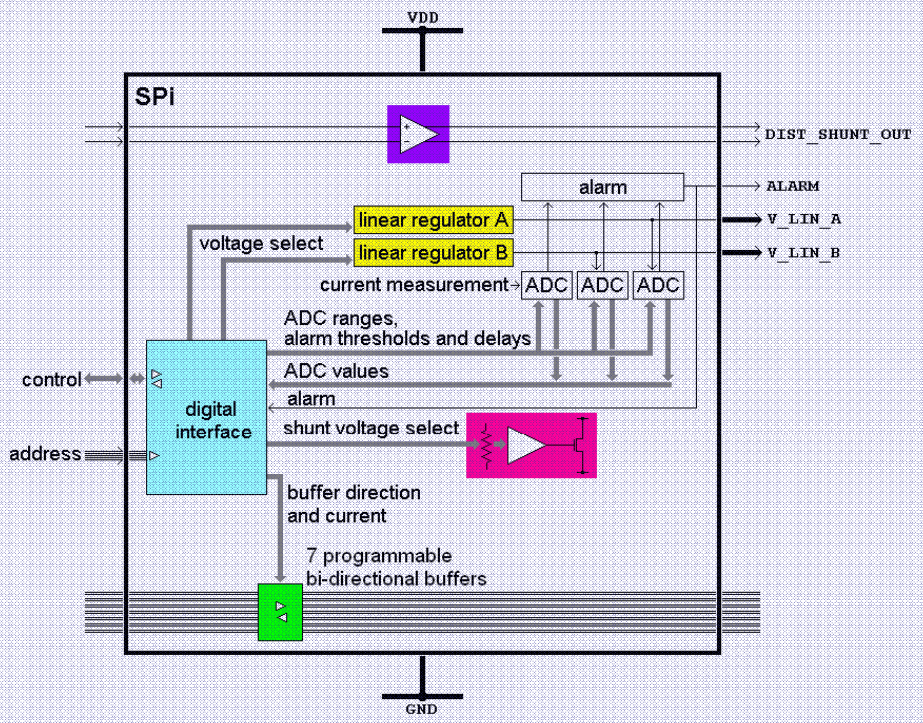
What is in SPi?

SPi offers…

- **Shunt regulator schemes**
- **Data communication**
- **Power management**
- **Monitoring/alarms**

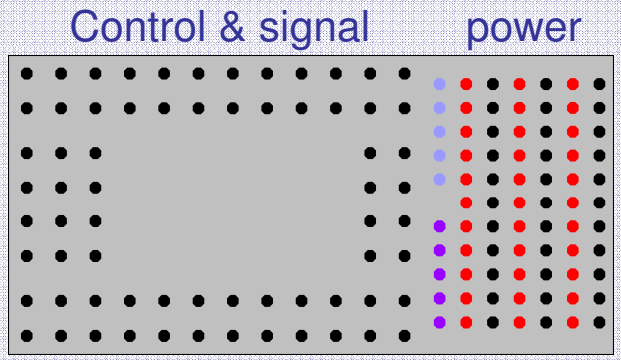
Designed by
Marcel Trimpl (FNAL)
And
Mitch Newcomer (U Penn)

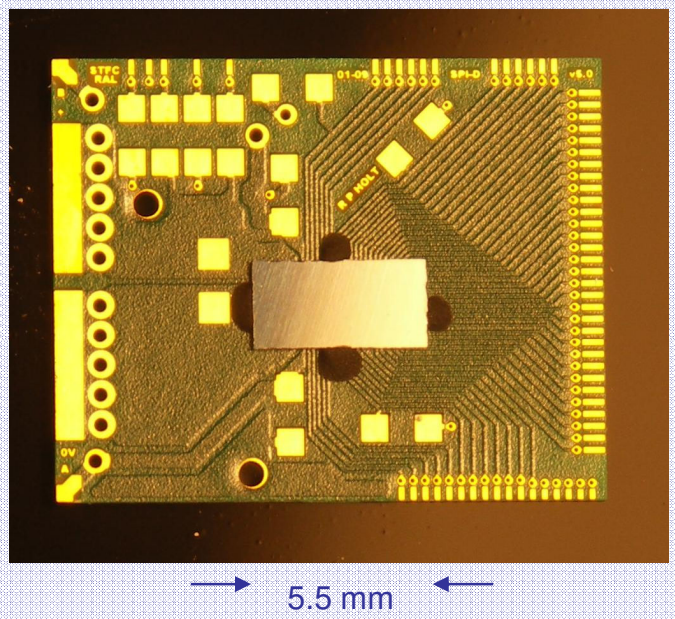


SPi – What does it look like?

SPi bump bonded flip chip

- **144 pads (68 I/O, 76 power)**
- **Sub-set used for each application**





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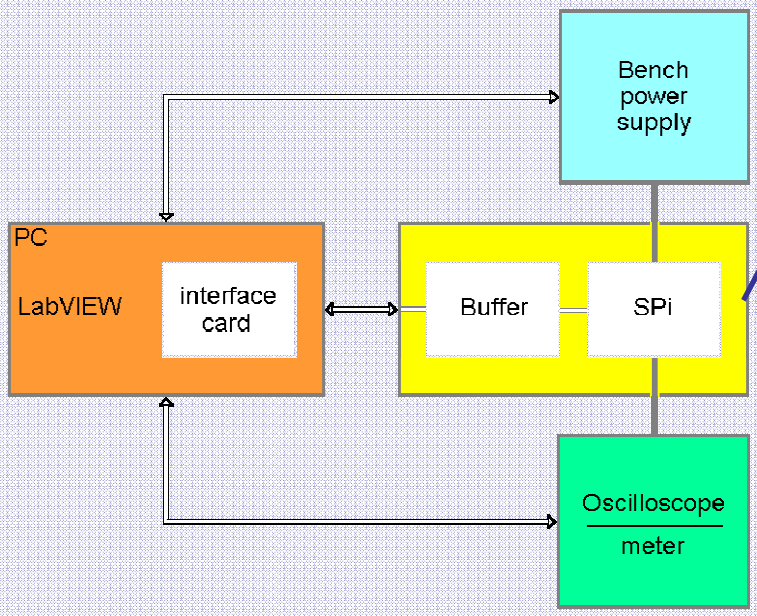
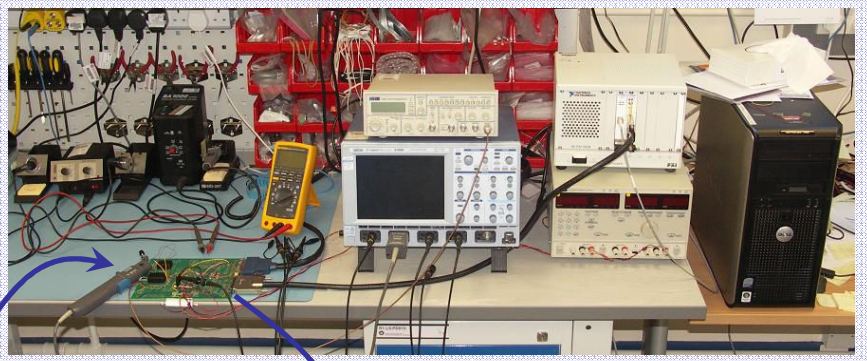
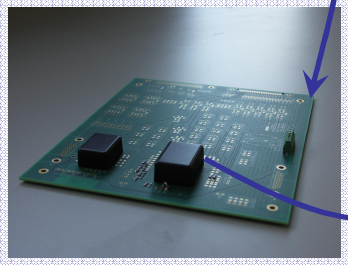
SPi – How is it tested?

- **Test PCB (access to all features)**
- **Test with hybrid**

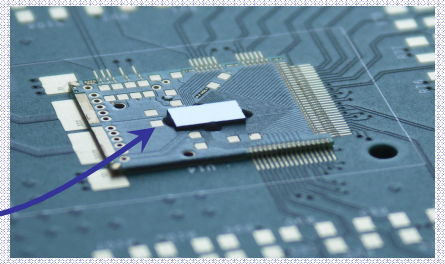




SPi on test PCB
under protective cover



Bump-bonded SPi…
Wire-bonding to test PBC

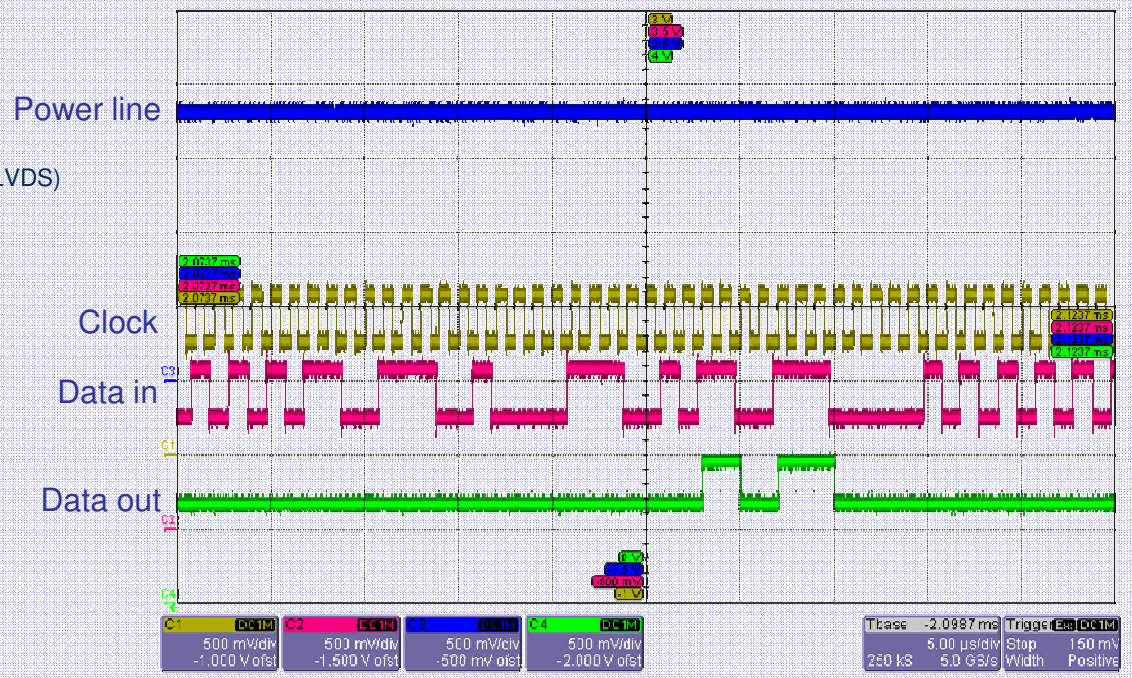


Example tests

Control √

Communication lines (AC-coupled LVDS)
- clock
- data in
- data out
- reset

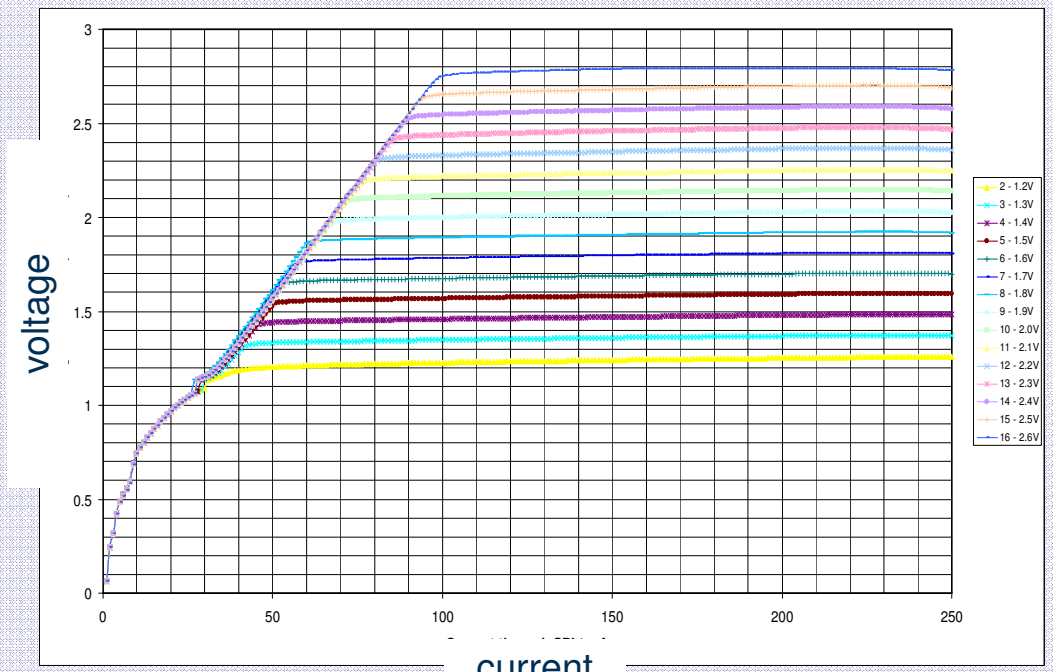
Controlled parameters
- shunt regulator voltage
- linear regulator voltages
- buffers
- ADCs
- alarms



Example tests

Programmable internal shunt regulator √

1.2 to 3 volts
0 to 4 amps
At higher power…
cooling is required



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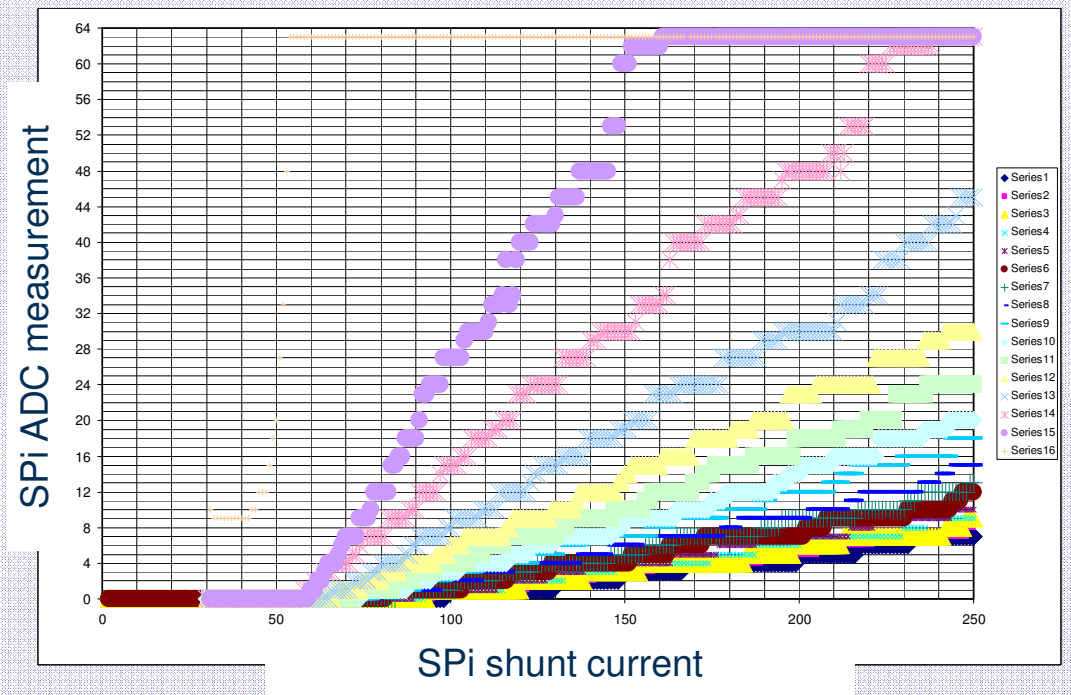
Example tests

Current measurement

√

6-bit ADC
16 measurement ranges
60mA to full capacity of SPi



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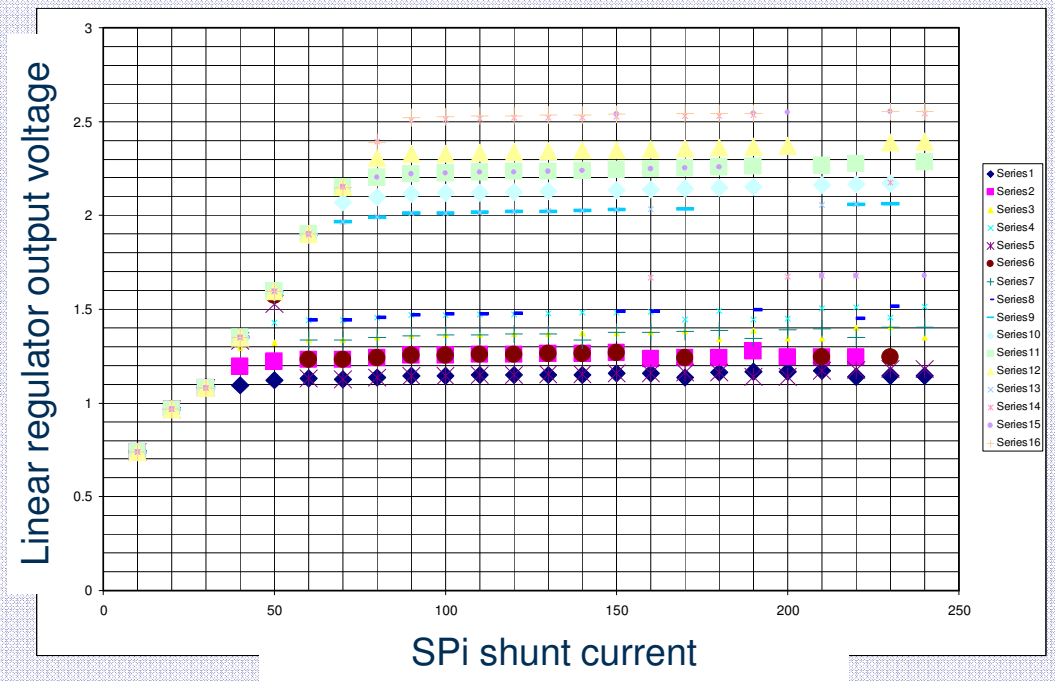
Example tests

Linear regulators

√

2 linear regulators
16 output levels
and 6-bit bias



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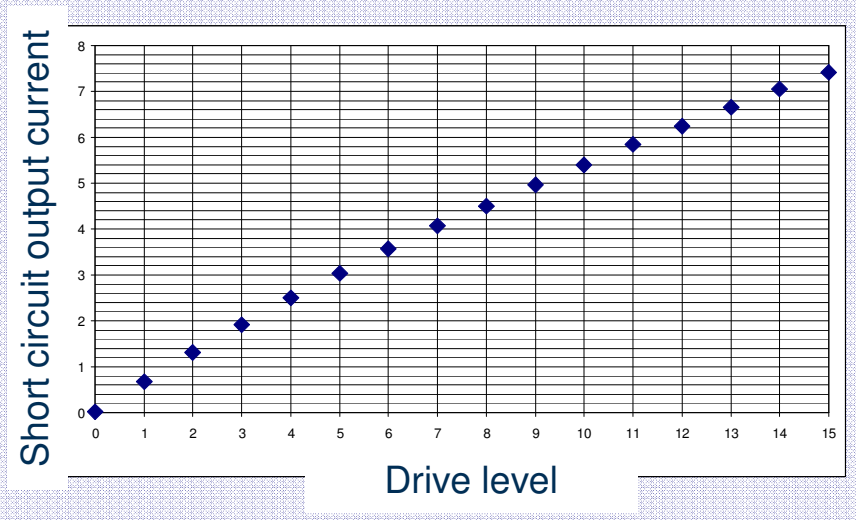
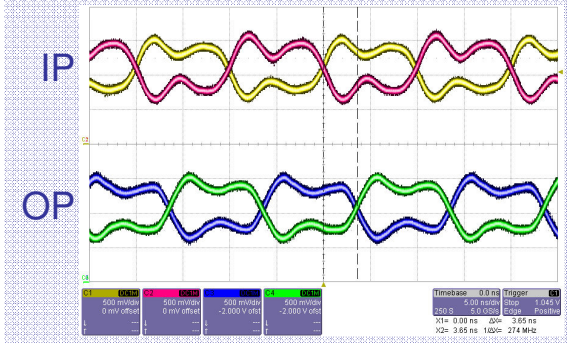
Example tests

Data communication through SPi

+ LVDS
+ 16 drive levels
+ Programmable direction
+ AC coupling compatible

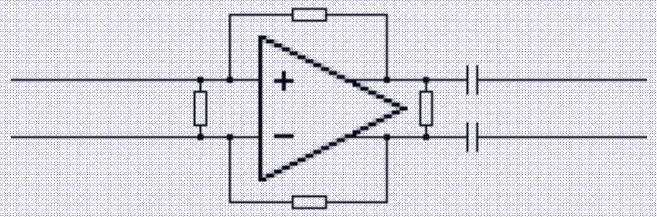
√





50 MHz clock,
Showing LVDS inputs and outputs

3.65 ns delay



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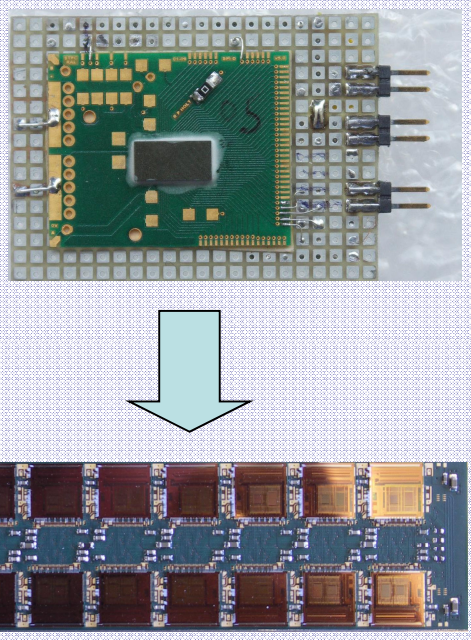
SPi with a hybrid

- **Shunt regulator schemes**
  - √ ABCN with SPi internal shunt regulator
  - √ ABCN with SPi controlling distributed shunt transistors
- **Data communication**
  - √ Data has passed through SPi
- **Power management**
  - √ Shunt current monitoring
  - √ Shunt regulator voltage setting
  - √ Linear regulators voltage setting
  - √ Alarm



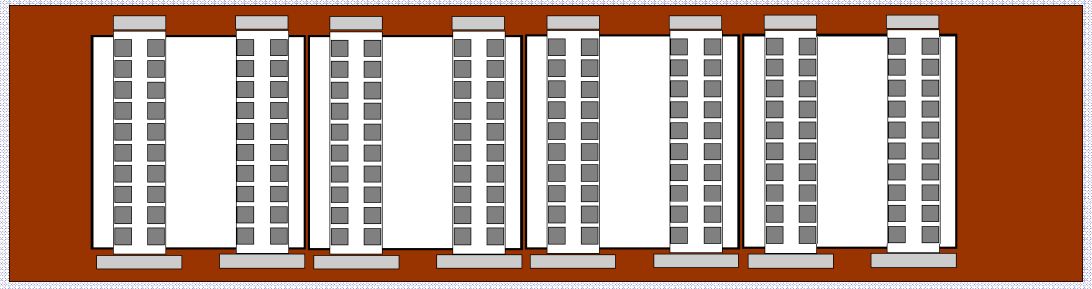
√ = tested and working Documentation is available to users

The future

What next?

The future

SPi will be used by the ATLAS community to power a demonstration stave



The power plug-in concept


Distributed


SPi

DC-DC

SPi will also be used in STAVE09

Diagrams above are not to same scale

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The future

A new design is planned

Slower data rate
Fewer control lines
More address bits
Temperature measurement
Integrated protection features
Improved shunt regulator

Reliability

New features

Hardware voltage setting
Power-on reset
Digital controller supply DC-DC
Radiation tolerance

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Summary

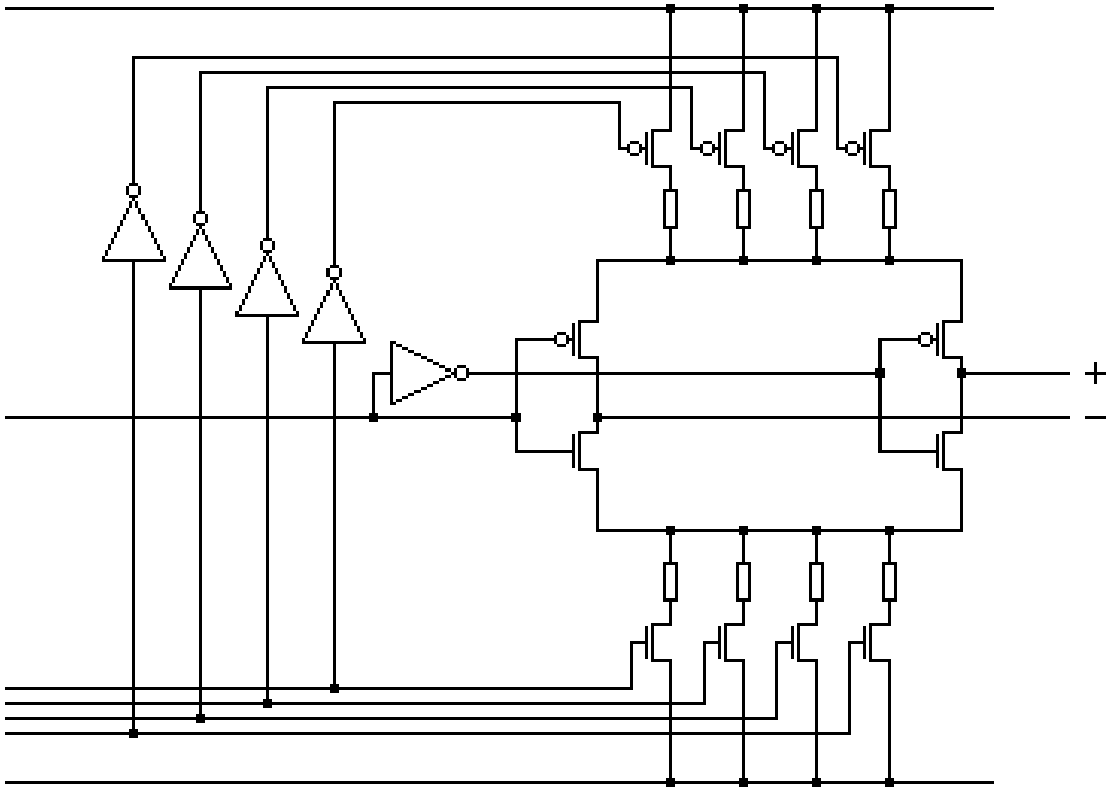
SPi exists SPi works

SPi will be used on a stave

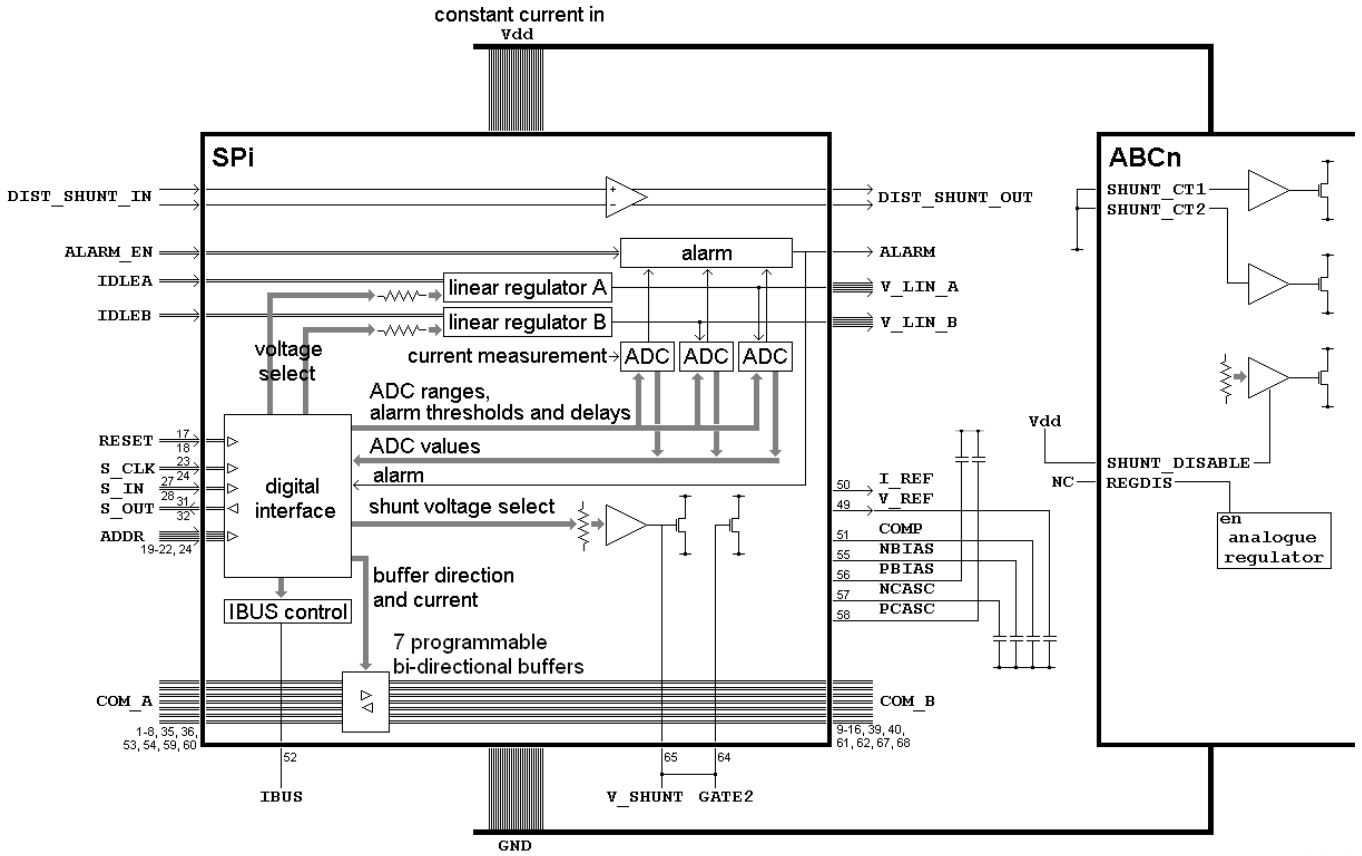
User documentation available

Supplemental slides

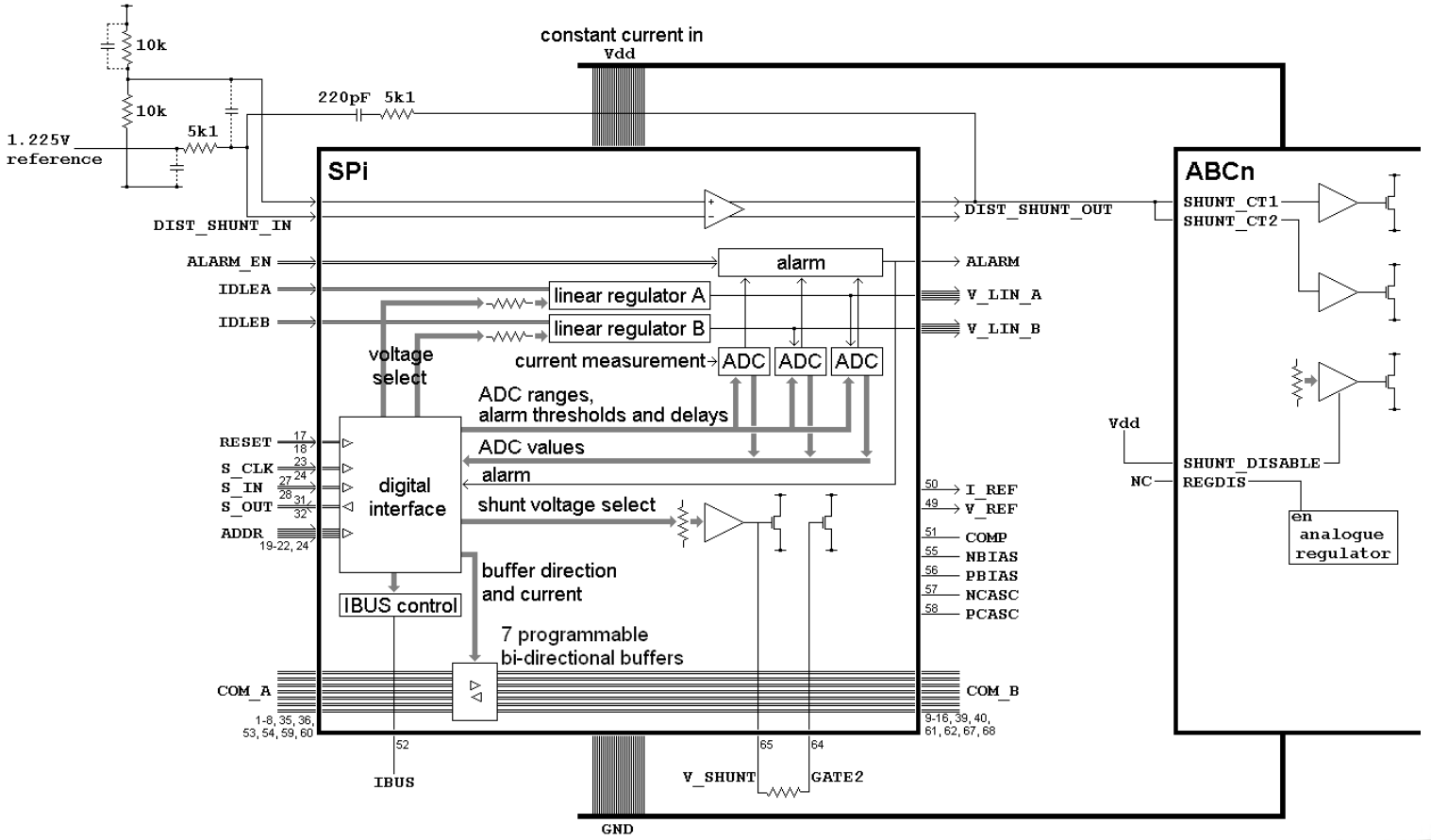
SPi internal serial data drive circuit



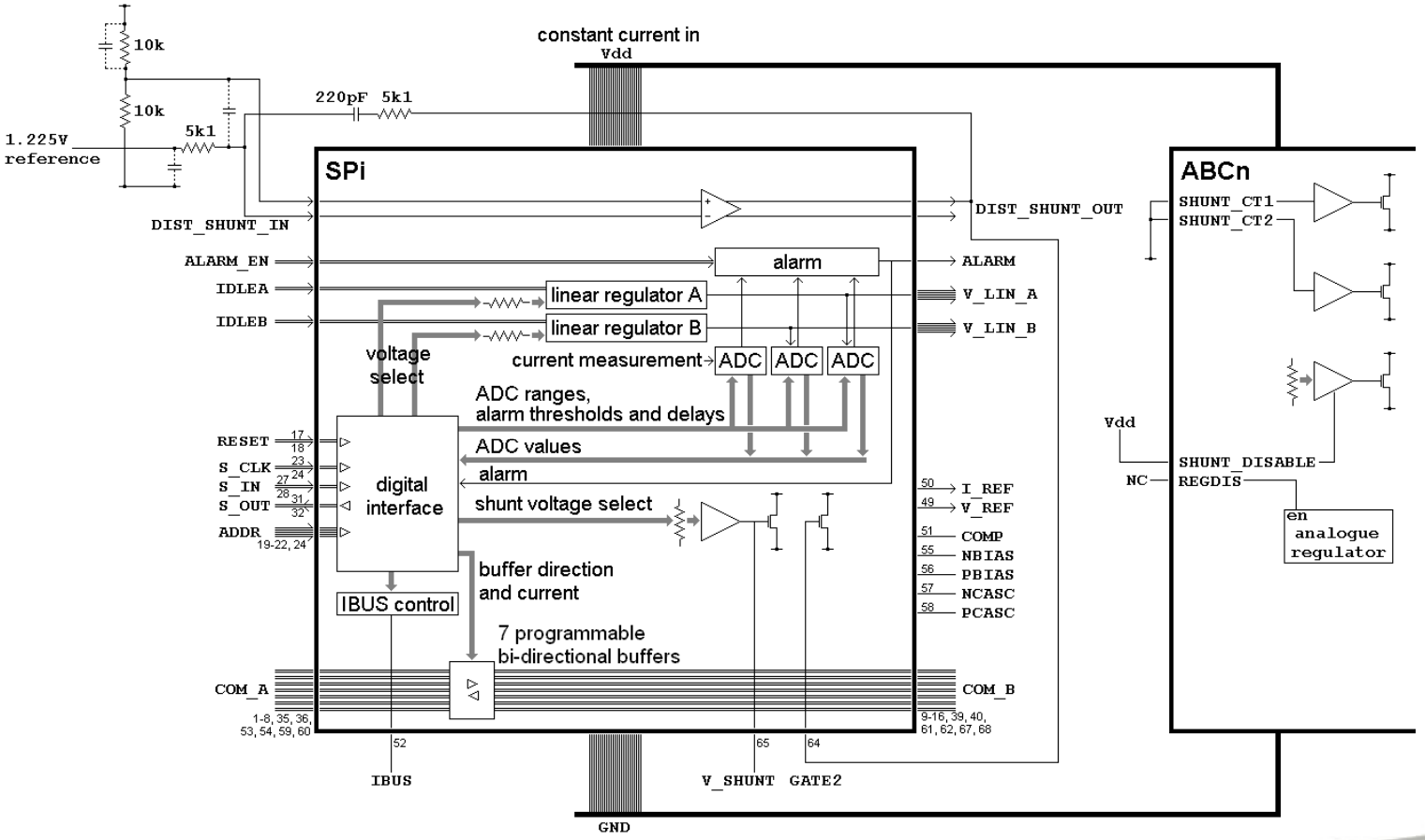
SPi internal digitally controlled shunt regulator



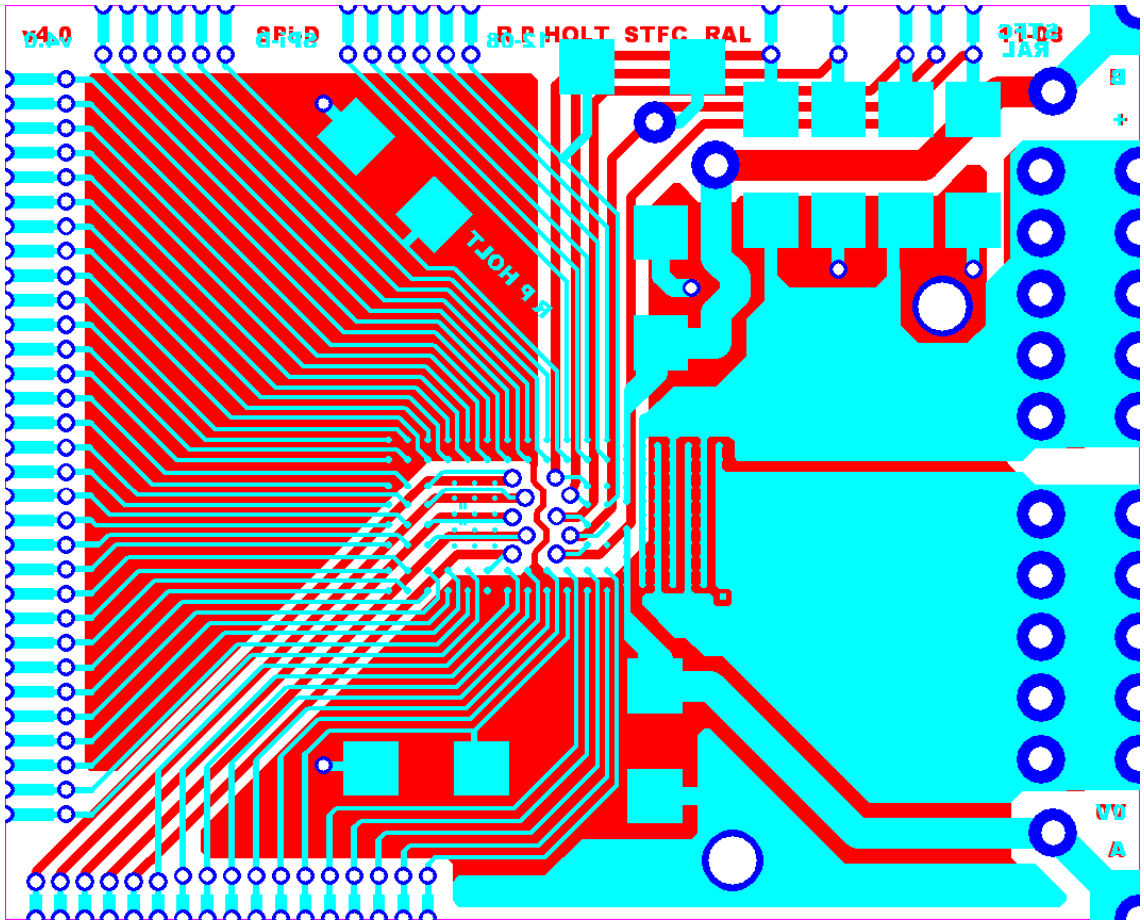
SPi linear shunt regulation, external shunt transistor(s)



SPi linear shunt regulation, internal shunt transistor(s)



Daughter PCB



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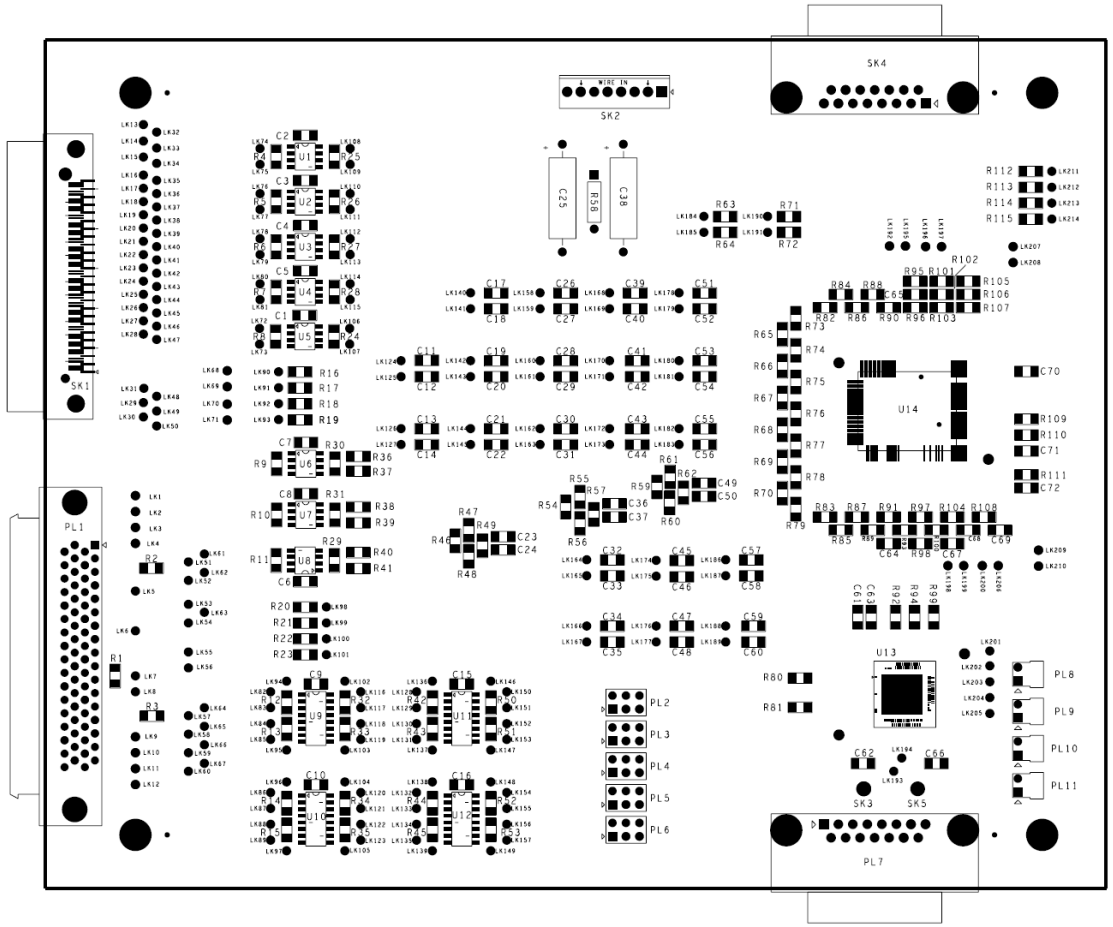
Mother PCB



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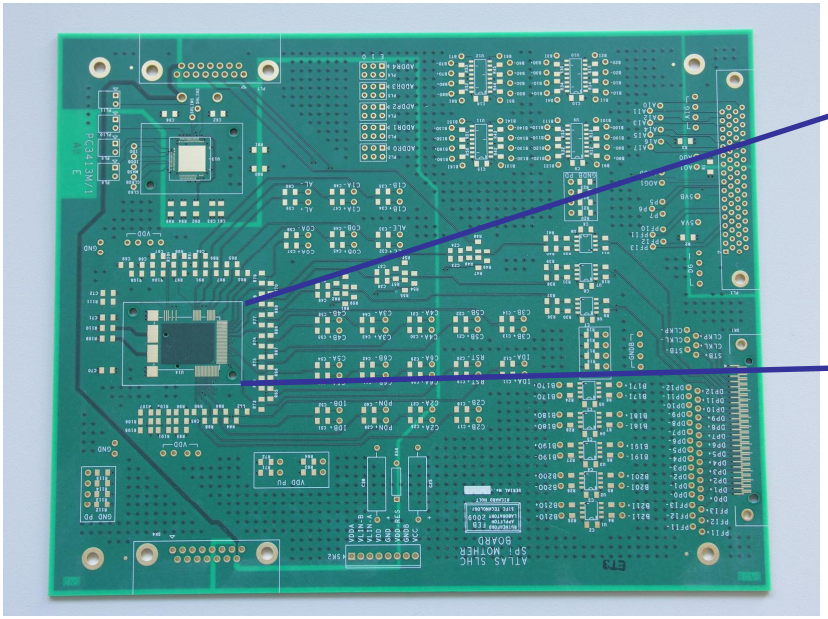
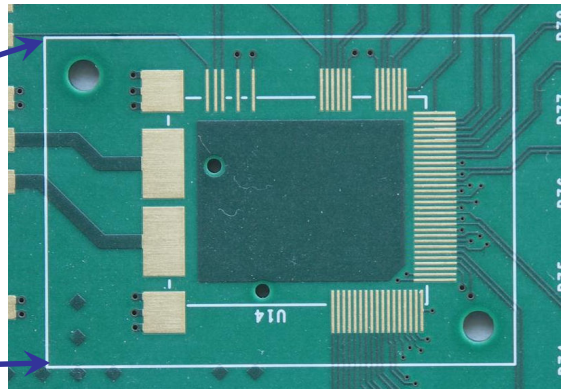
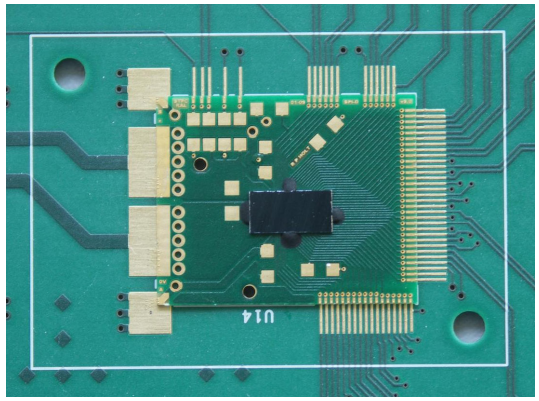
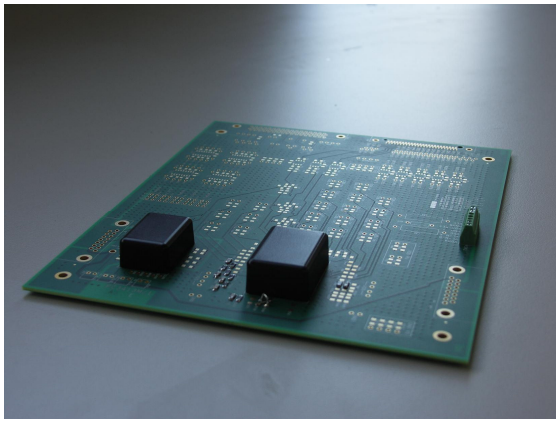
Mother PCB









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ASIC design