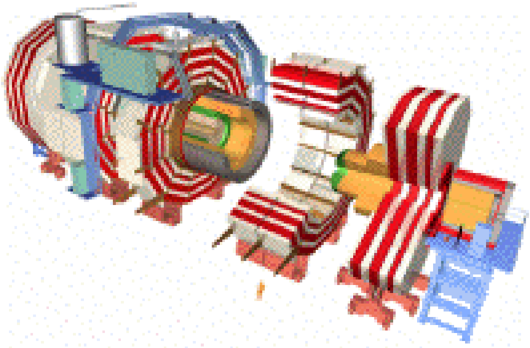


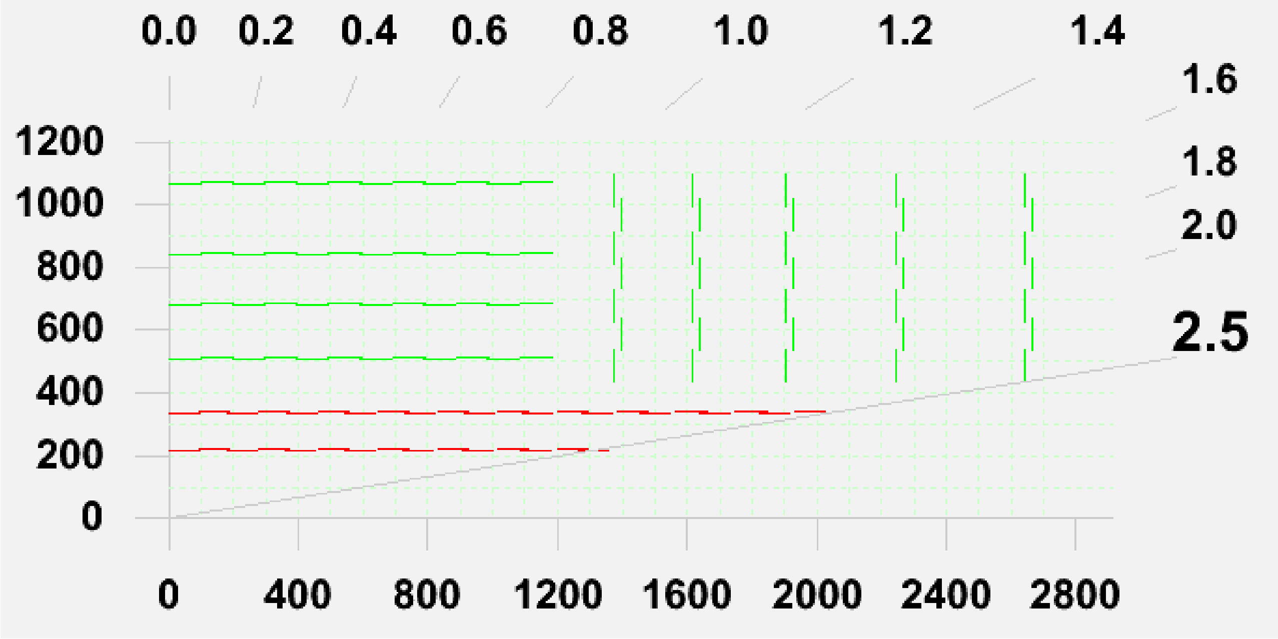
Trigger module for the CMS Tracker at SLHC

Special thanks to
A Marchioro, M. Pesaresi, M. Raymond
CMS Track-trigger task force
CMS Tracker upgrade simulation team

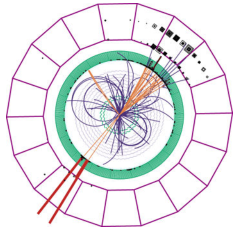
Geoff Hall

New CMS Tracker for $10^{35}cm^{-2}s^{-1}$

- Alternative layouts under consideration. All required to provide tracker information into L1 trigger.
  – eg pixels, short strip outer Tracker, plus "PT layers"



= double layer modules with correlation capability which can identify tracks above certain p_T value



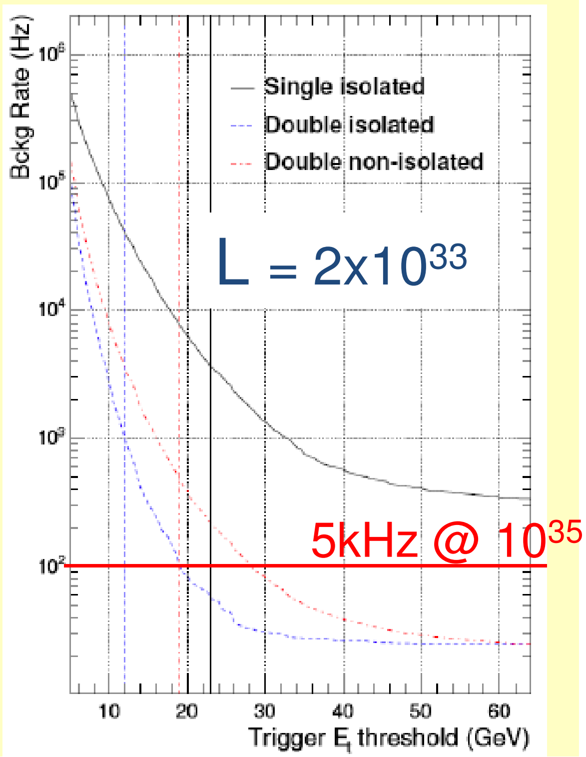
Why tracker input to L1 trigger?

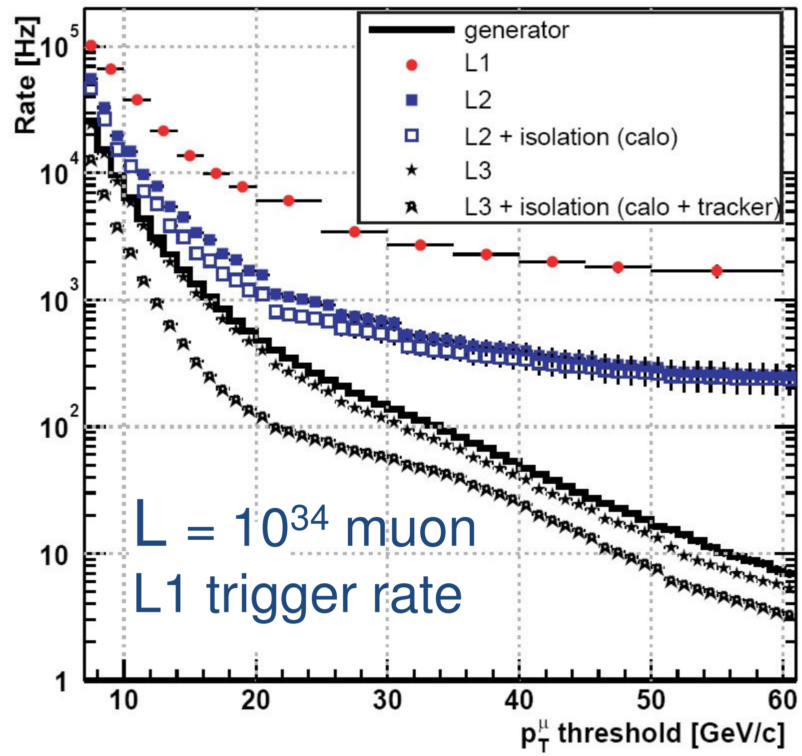
- Single *μ, e and jet* L1 trigger rates will greatly exceed 100kHz
  - Tracker data appears to be only extra info capable of improving selectivity
    - can increase latency, to 6.4μs, but must maintain 100kHz for compatibility

Single electron trigger rate

$<p_T> \approx$ few GeV/bx/trigger tower

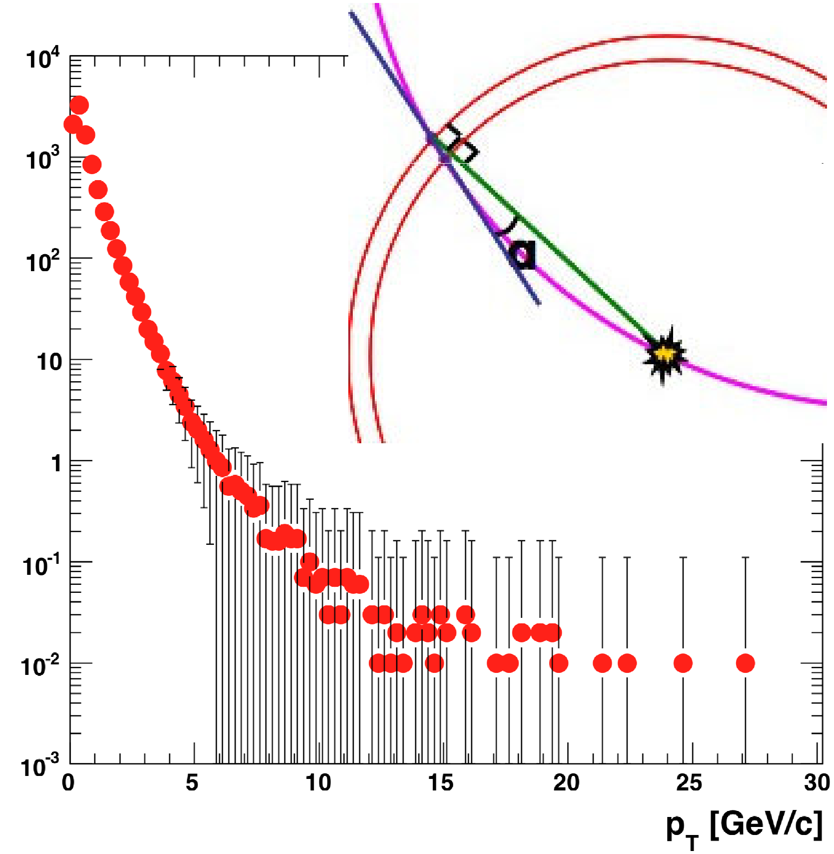
Isolation criteria alone are insufficient to reduce rate at L= *10^{35} cm^{-2}.s^{-1}*





The track-trigger challenge

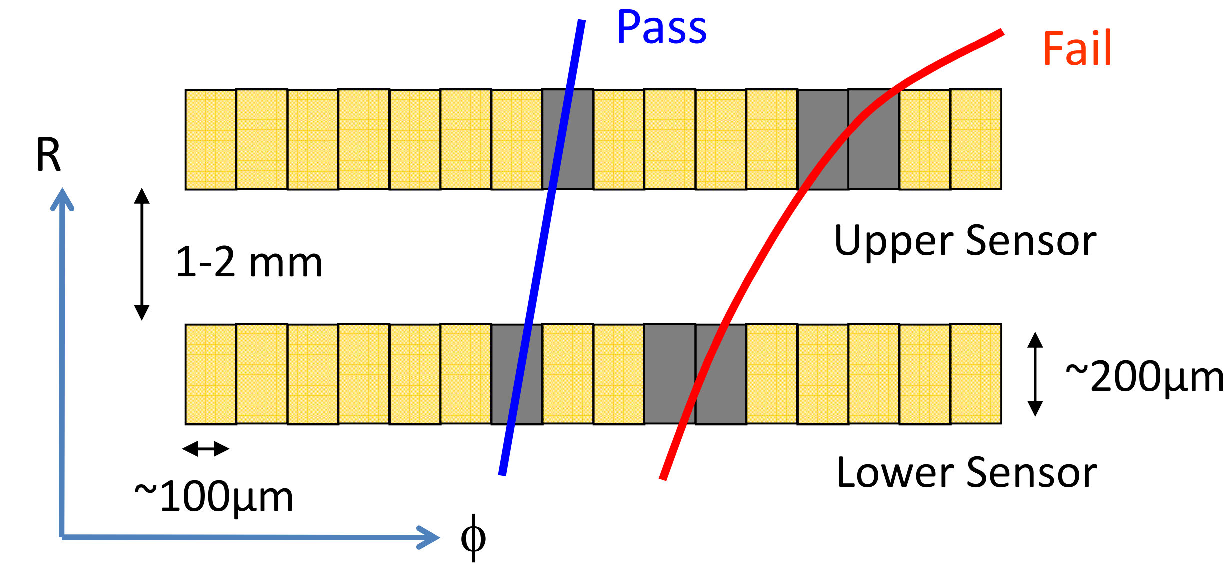
- Impossible to transfer all data off-detector for decision logic
  - eg ~0.5% occupancy at R ≈ 25cm at $10^{35}cm^{-2}s^{-1}$ in 2.5mm x 100µm pixels
  - => ~20Mpix x 24bits => ~96,000 Gb/s
  - on-detector data reduction (or selective readout) essential
- Large fraction of low p_T tracks
  - not useful for trigger
  - conceptually simple to measure
  - hit density means high combinatorials
- Double layer identifies "stubs"
  - pairs of nearby hits
  - in double layers
  - above a p_T threshold



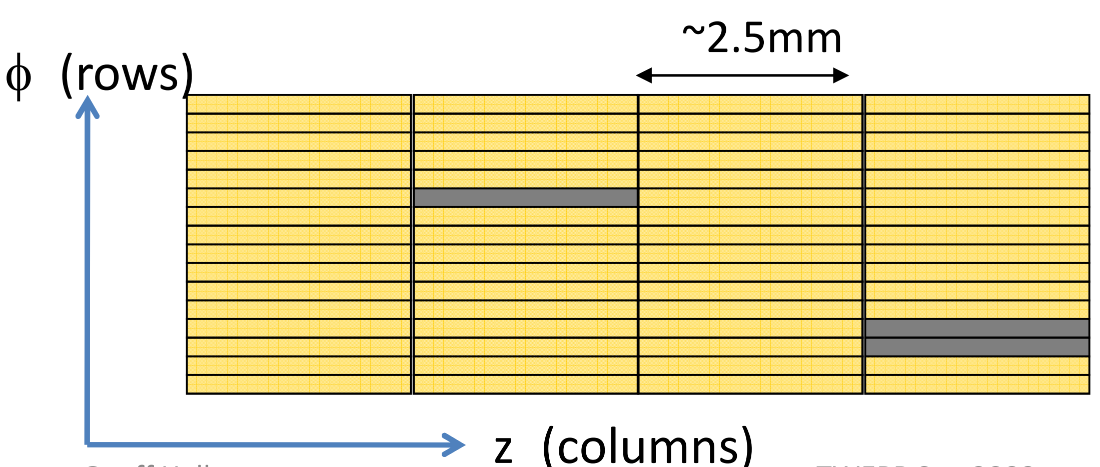
A Pixel Detector for Level-1 Triggering at SLHC
J. Jones, G. Hall, C. Foudas, A. Rose
CERN Report CERN-2005-011(2005) 130-134

Basic module requirements

- Compare binary pattern of hit pixels on upper and lower sensors



High p_T tracks can be identified if hits lie within a search window in R-ϕ (rows) in second layer

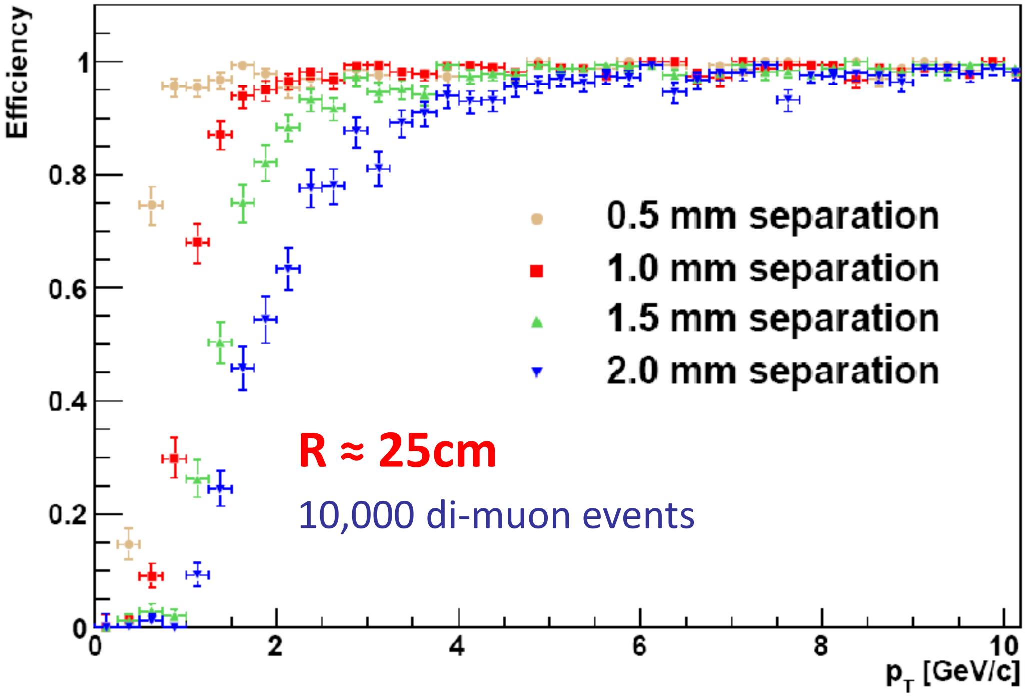


Sensor separation and search window determines p_T cut

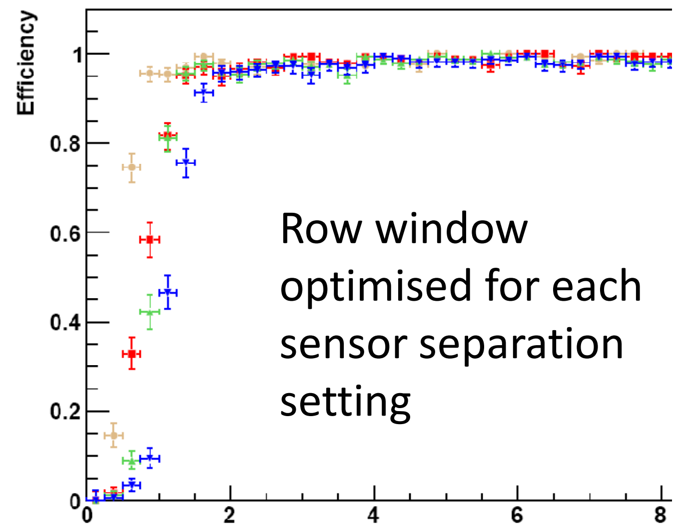
Simulation results

M Pesaresi

- Sensors untilted (no Lorentz compensation)



ΔR [mm]	ε_{max} [%]	Fake [%]	Reduction factor
0.5	99.0	0.7	8.0
1.0	99.4	4.1	22
2.0	97.7	17.8	96
3.0	96.0	39.0	210
4.0	92.9	47.2	254

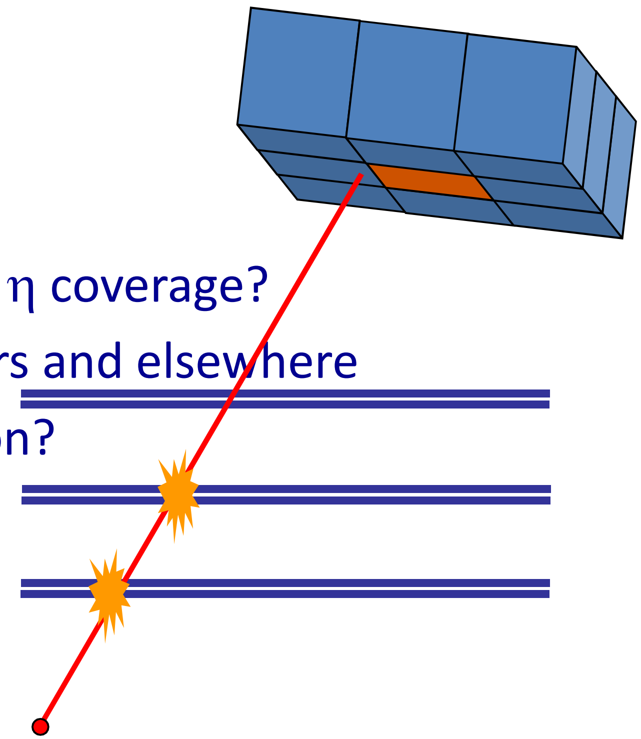


Row window optimised for each sensor separation setting

Row window = 3 pixels
Column window = 2 pixels @ 0.5mm;
3 pixels @ 1mm- 2mm

Making a trigger

- Stubs provide track trigger <u>primitives</u>
- Not yet proven how these contribute to trigger
  - and rate reduction achievable
  - many simulation studies under way
  - expect to match a series of stubs to a calorimeter or muon object
    - using off-detector processors
- Questions to answer include
  - how many layers are needed?
  - what is the optimal location, allowing sufficient η coverage?
  - what is the impact of material? – in trigger layers and elsewhere
  - how important is z-measurement, and resolution?
  - what is the impact on tracking performance?
  - cost, power and material budget?
  - L0 trigger to guide?

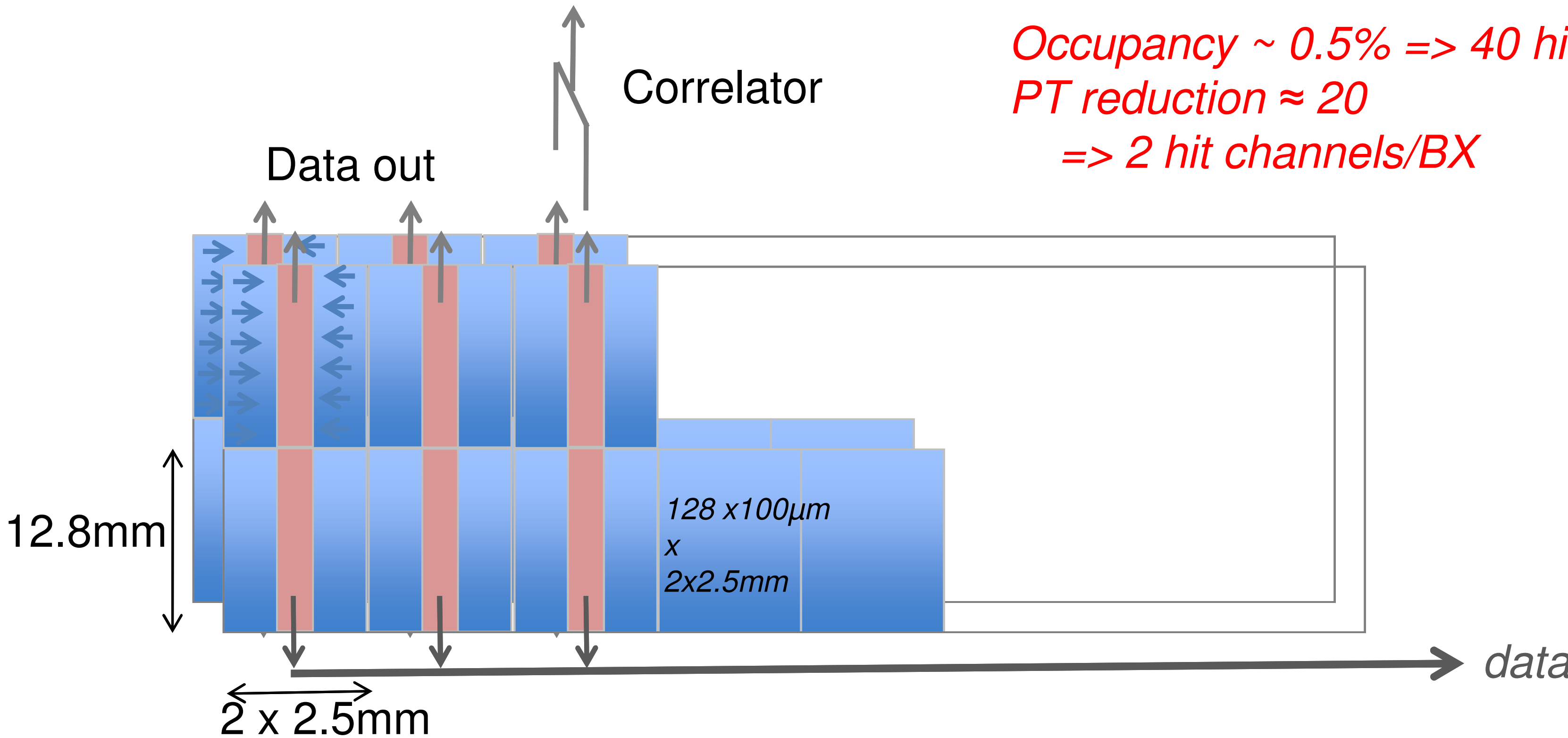


Schematic PT module (1)

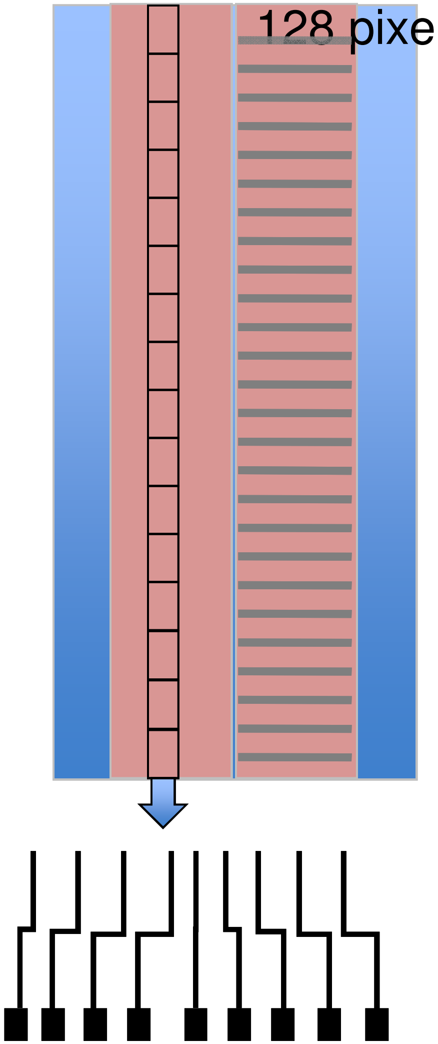
- Transfer hits to edge – if possible with minimal power – for comparison logic
  - also store hits on pixel for L1 readout

Module 25.6mm x 80mm
256 x 32 sub-units = 8192 channels

Occupancy ~ 0.5% => 40 hit pixels
PT reduction ≈ 20
=> 2 hit channels/BX



Possible PT layer readout



- shift register ruled out: 128/25ns = 5.12Gb/s

- divide column into 32 x 4 channel groups
  - eg logic sets 9 address lines:
  - 5 bit group + 4 bit pattern +1 bit spare
  - provide more information than single channel address
  - ignore combinations consistent with wide clusters

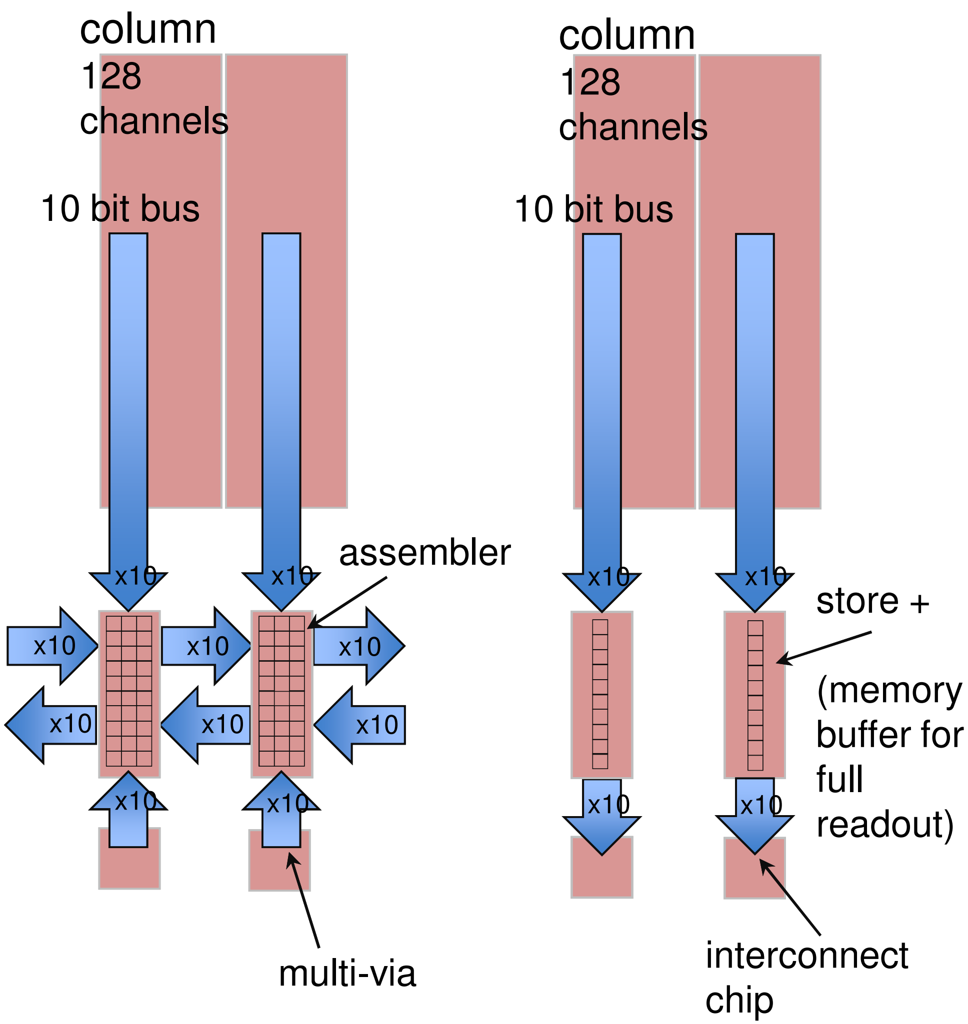
- a moderate number of address lines should be sufficient
  - Nearest neighbour logic to avoid group boundaries

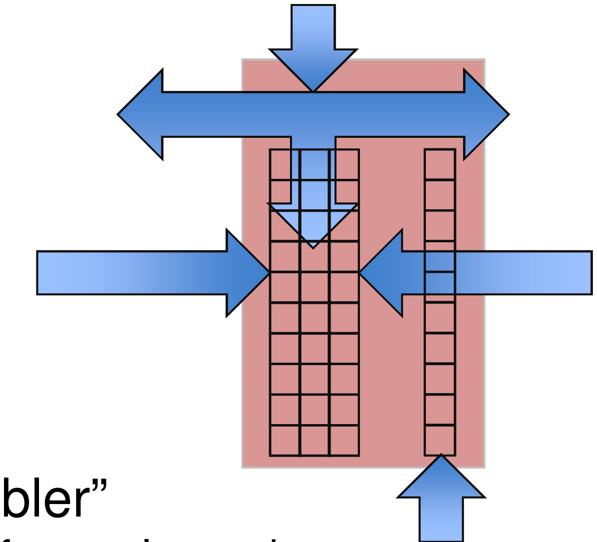
- worst case occupancy may mean >1 hit/BX
  - could read out 2/BX @ 80MHz
  - NB jets don't have much impact

Track stub generation by matching layers

upper layer

lower layer



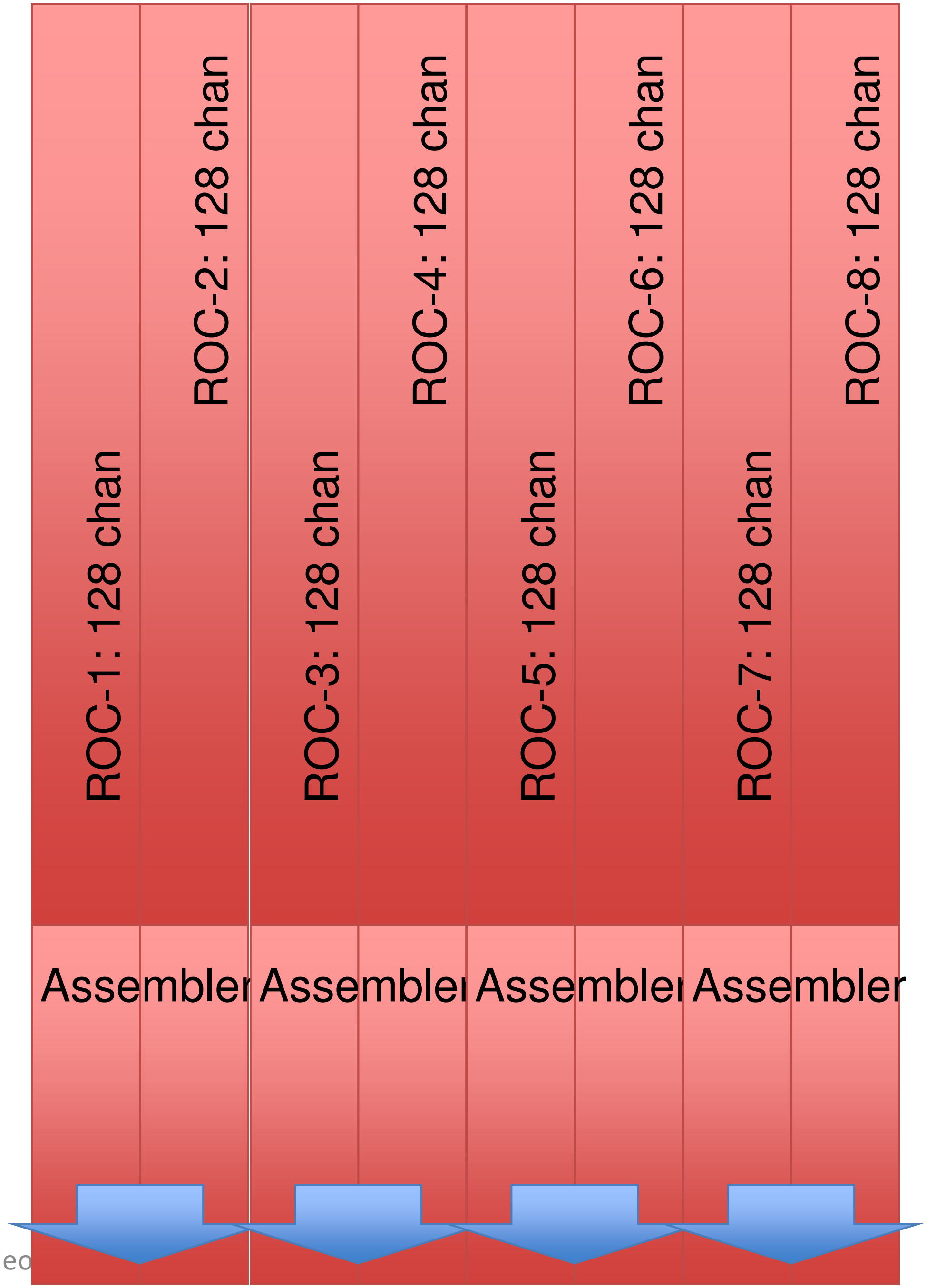


“assembler”

- 10 bits from column above
- transmits column to each neighbour
- receives 10 inputs from each neighbour and stores
- receives 10 inputs from module below

compares pattern from module below with three (10 bit) stored patterns

Layout



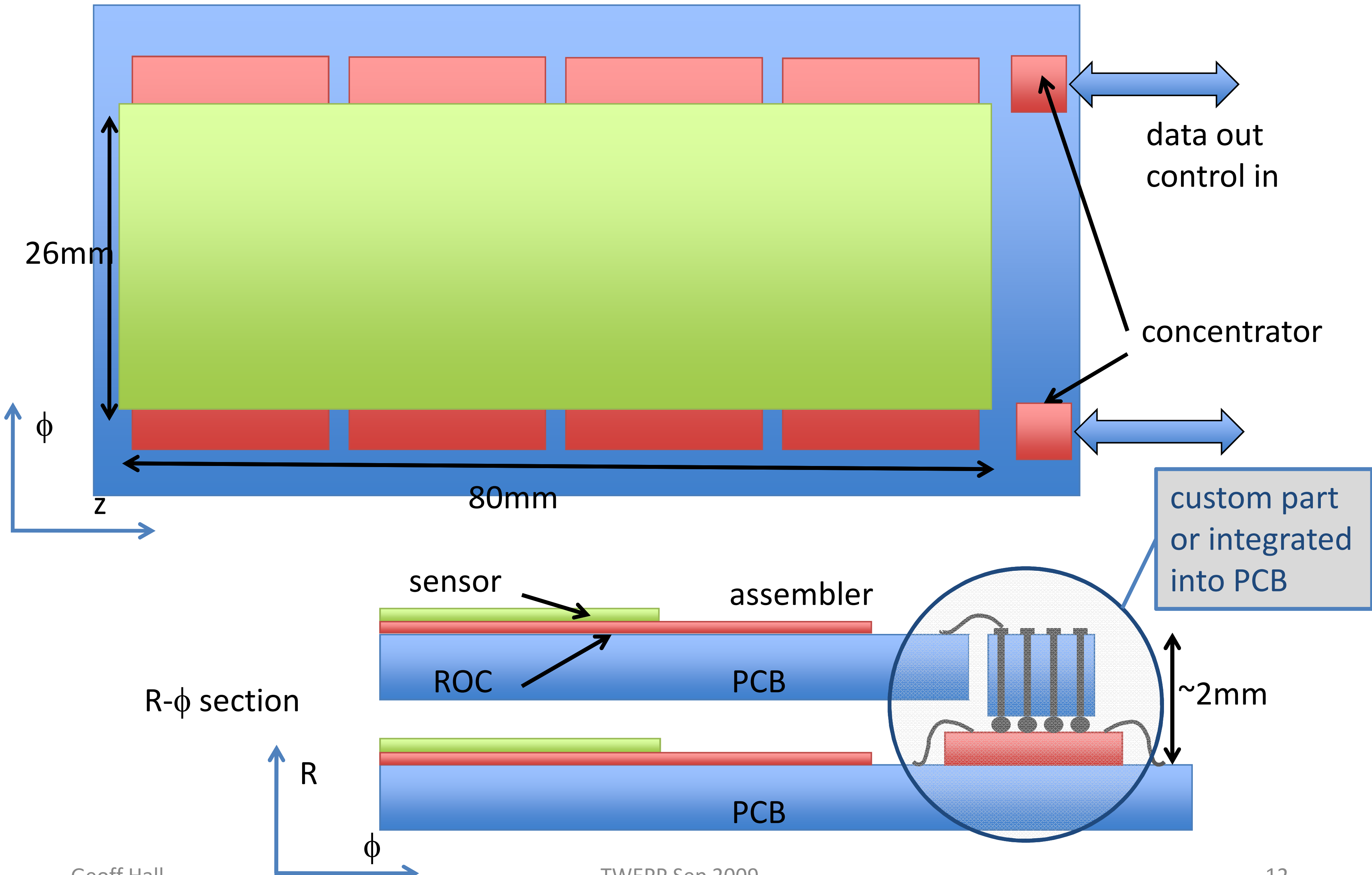
Make ROC + Assembler as single ASIC
identical for both layers
may switch off elements

Most practical to produce a chip to serve several columns which eases data transfer and line density

e.g
Width: 8 x 1.5mm + 1mm to read 8 x 2.5mm

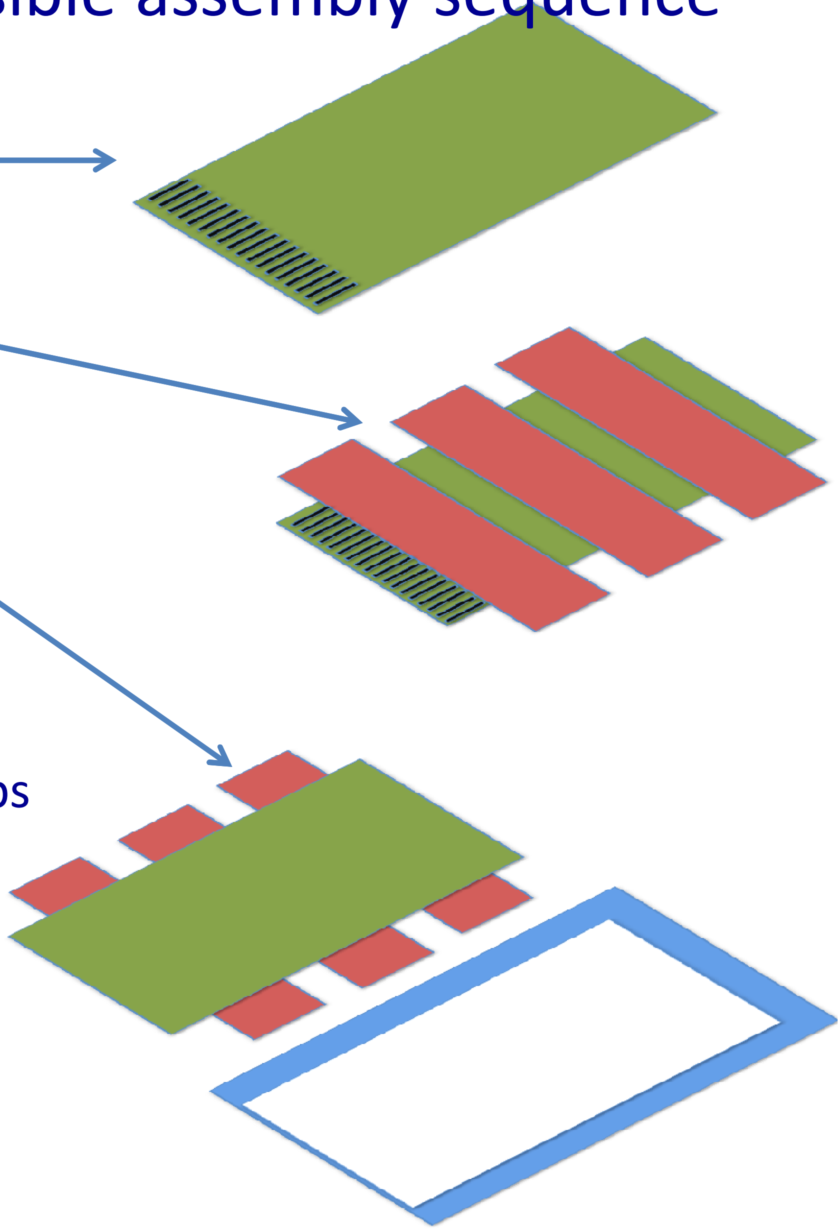
Chip size ≈ 18mm x 13mm

Module schematic



Possible assembly sequence

- Sensor
- ROCs bump bonded to sensor
- Invert sensor-ROC object
  - Exposed ROC areas then face up
- Place assembly on hybrid
  - hybrid has pre-mounted ancillary chips
  - Wire bond ROCs to hybrid
- Prepare partner module
  - assemble and connect together

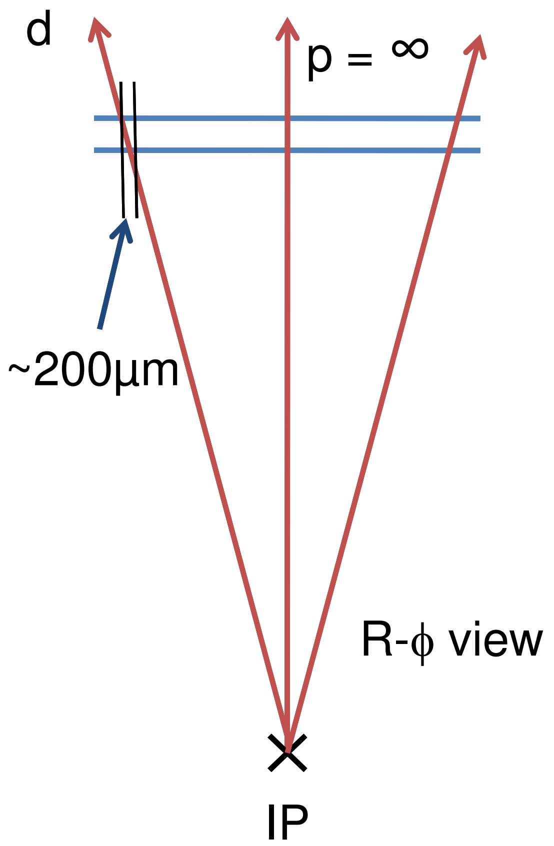


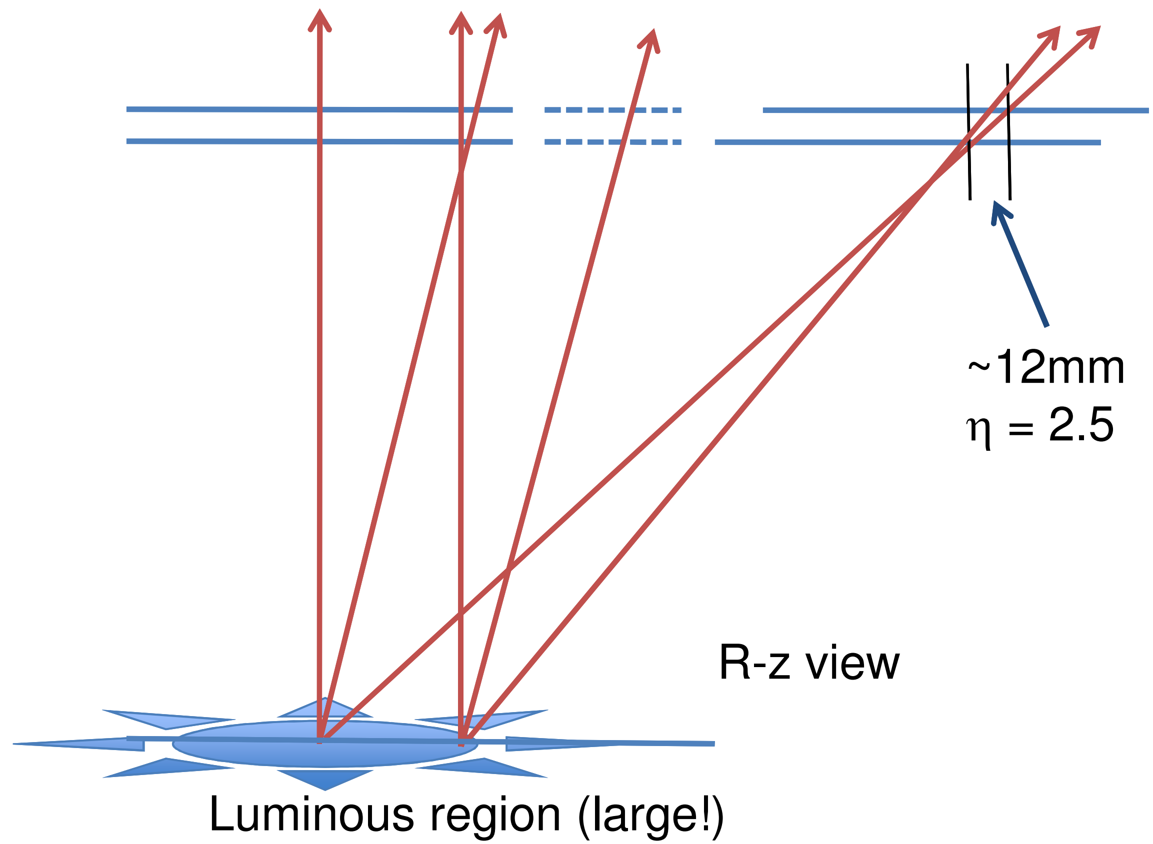
Comparison logic

- Modules are flat, not arcs
- Compensate for Lorentz drift
- Orientation of module

=> position dependent logic

- z offset η dependent
- search window to allow for luminous region and quantization => 3 pixels (if not tiny)





- Family of modules with offsets in z

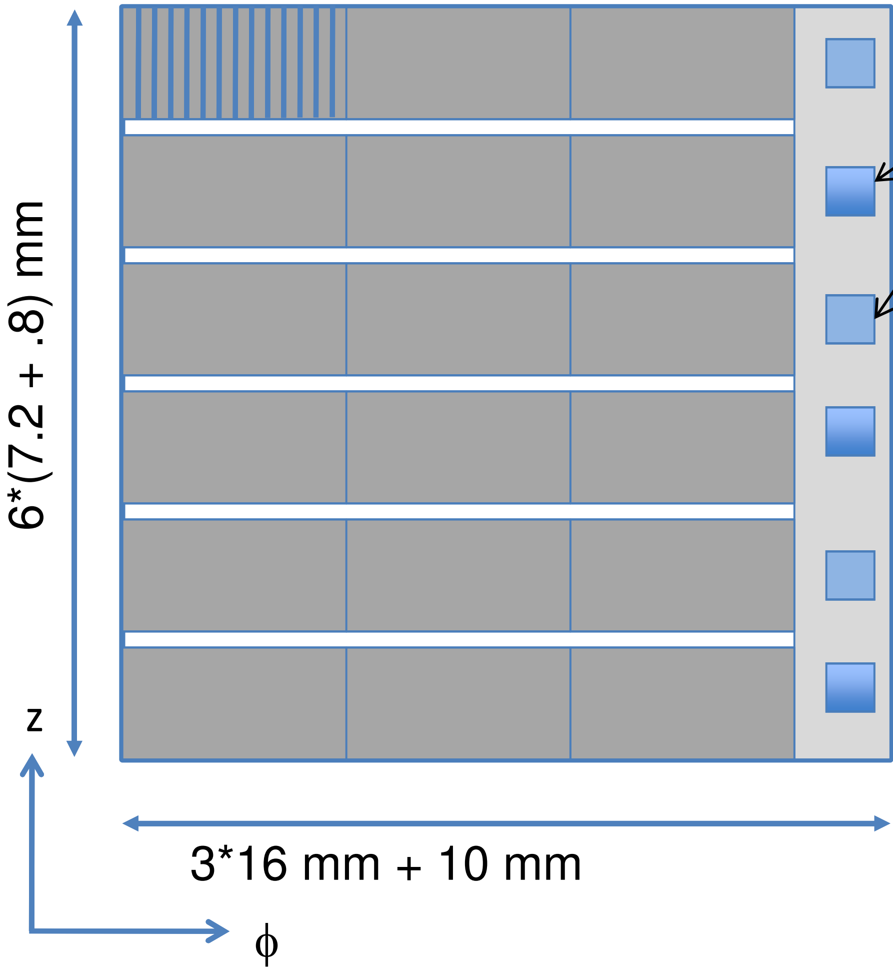
Large scale manufacture

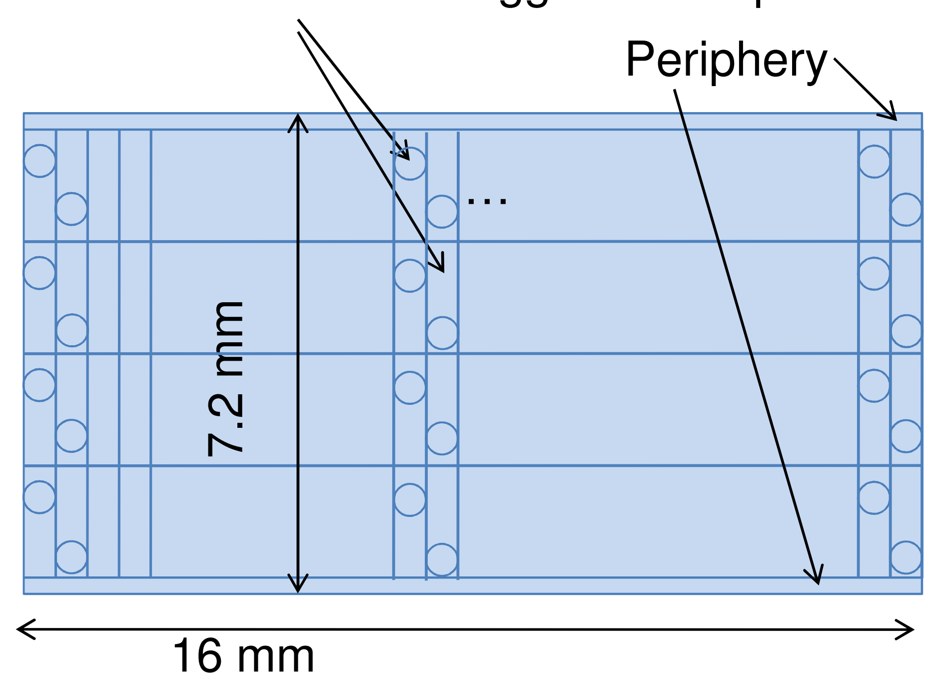
- Previous concept should be buildable using conventional technologies, with coarse pitch bump bonding
  - upgrade will probably require a large number of modules to be constructed uniformly to high standard in a short time
    - at least pixels, PT and short strip outer tracker (≥3 types)
  - CMS has experience of automated assembly but it will be highly desirable to optimise construction to take full advantage of commercial manufacturing
- It may be possible to design a module with more advanced technologies, and transfer much of the assembly issues to industry
  - requires different approach to logic
  - careful evaluation of commercial manufacturing
  - multi-layer technologies continue to advance significantly

Schematic PT module (2)

A Marchioro

- Basic module: ROC ASICs bump bonded to sensor

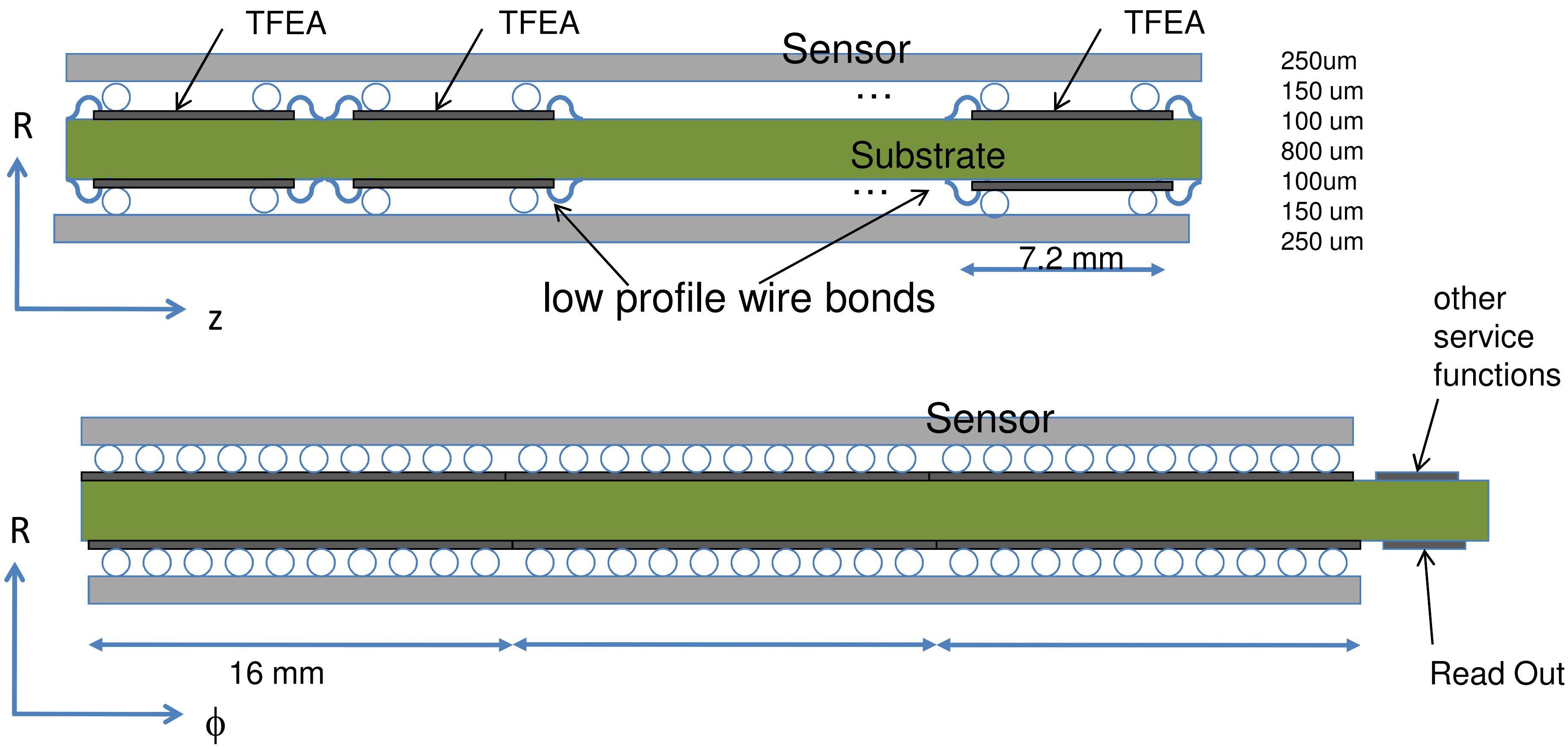




Cross-section

A Marchioro

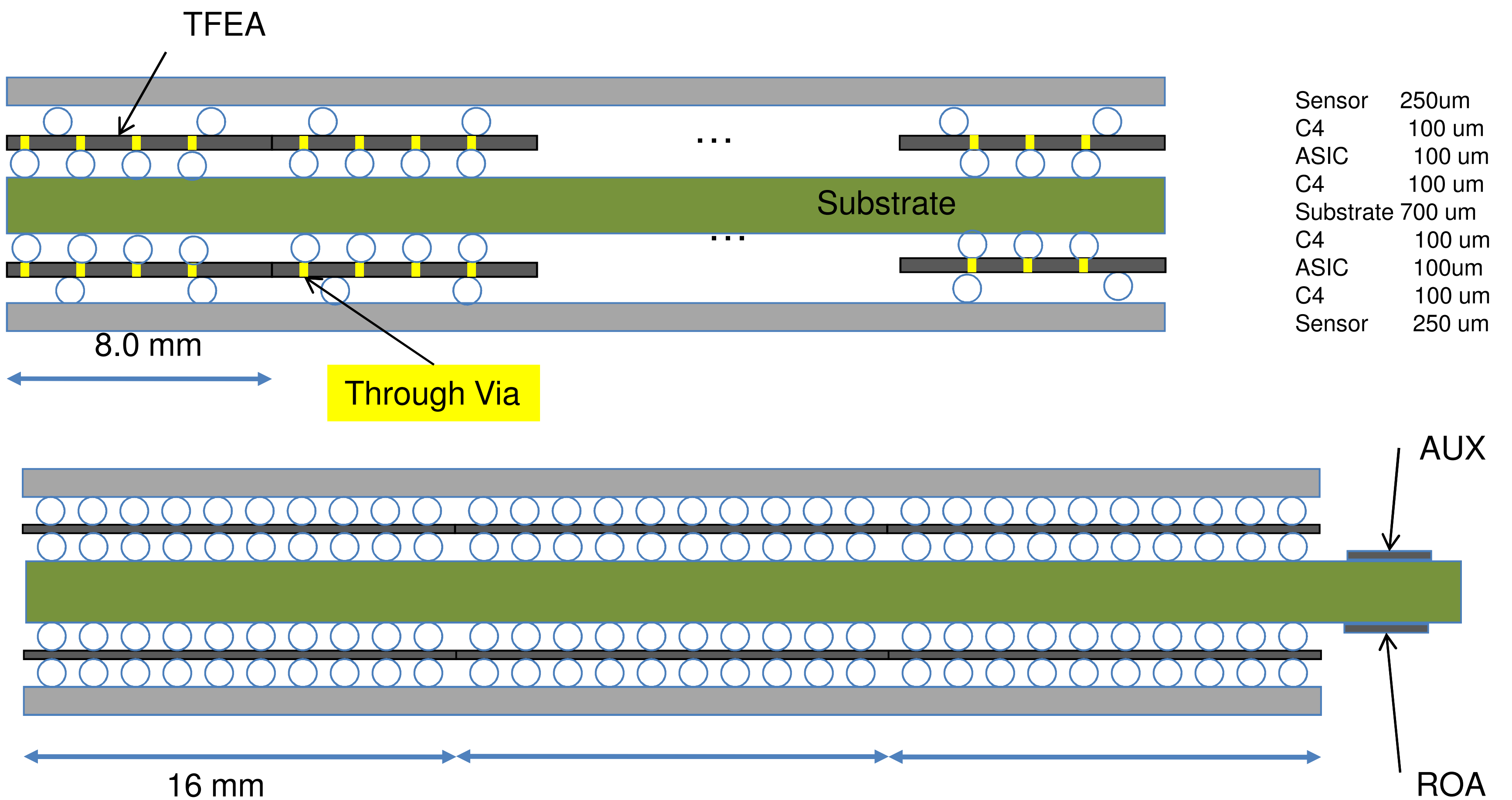
- Assembly may need to be in unconventional order
  - is it possible to place sensors at last stage?



Double bump assembly

A Marchioro

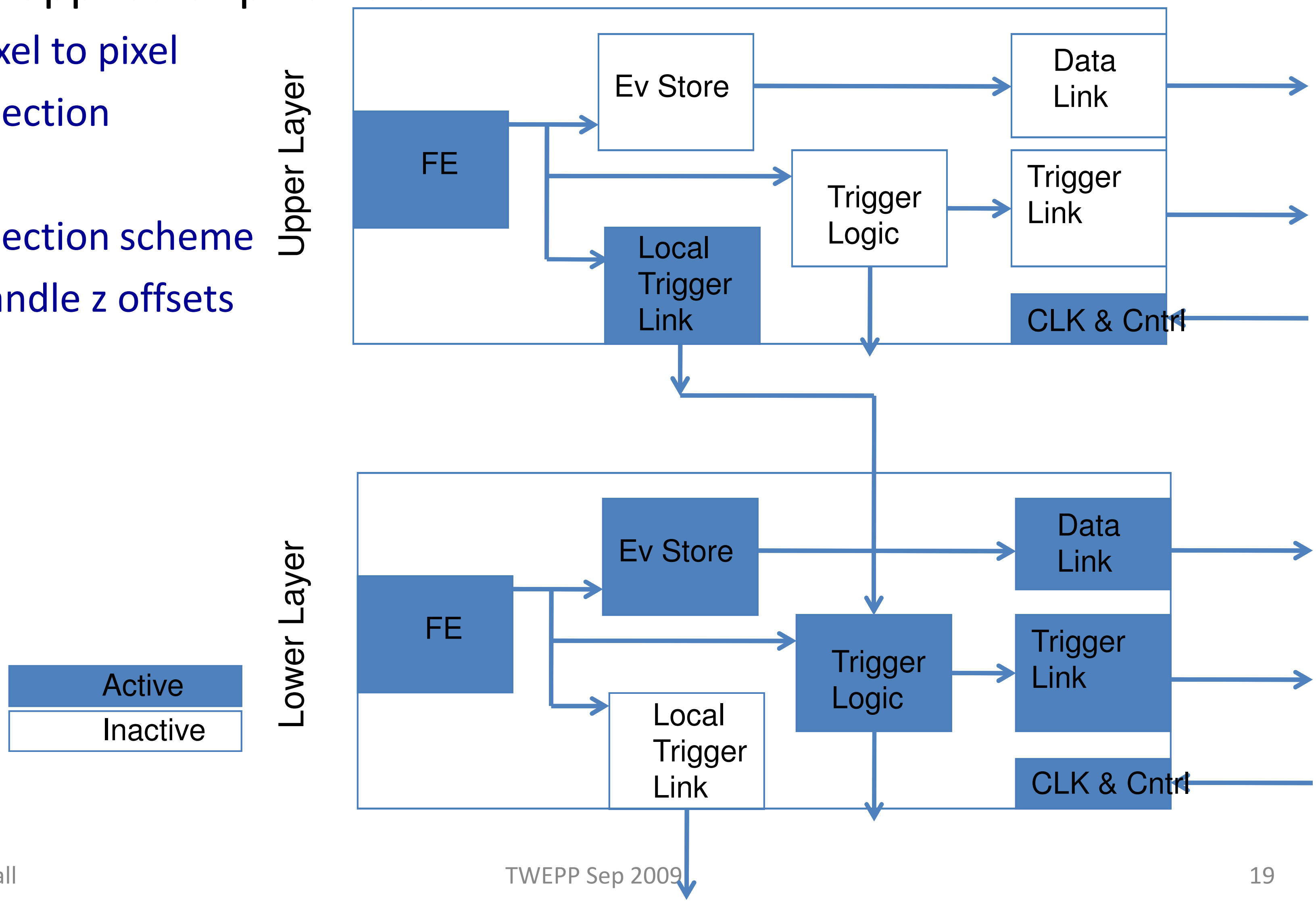
- Such techniques are becoming available
  - eg for high density non-volatile memories and telecom applications



Functional logic block diagram

A Marchioro

- Logic applied at pixel level
  - pixel to pixel connection plus connection scheme to handle z offsets



Data volumes and link requirements

- Assume 24 bits/hit to transfer in each 25ns BX
  - includes time stamp and error coding
  - send trigger data from **one** layer of stack

for 40M channels in stacked layer $L = 10^{35}$ $cm^{-2}s^{-1}$	
Channels/chip	128
Occupancy	0.005
PT data reduction	0.050
Channels above PT cut/BX/layer	5,000
bits/channel	24
No links @ **3.2**Gbps	1,500
Power/link [W]	2.0
Link Power [kW]	3.0
Power/chan [µW]	75

NB – 75µW is minimal estimate, assumes 100% use of bandwidth

50% may be realistic estimate

– following trigger reading out all data requires 6.4µs storage on each FE pixel and additional links

subject of detailed layout studies

Power estimate for PT module_1

	P [µW] per pixel	Functions
Front end	25	amplifier, discriminator local logic, cf ATLAS 130nm pixel
Control, PLL	10	1 PLL/ROC @ 5mW, x 2
Digital logic	8	comparison logic and transfer to edge: 1mW/column
Data transfer	2.5	few cm across module
Data transfer	10	transmission to remote GBT: 80mW/module @ 10pJ/bit
Concentrator	5	buffer to and from GBT: 2 ASICs @ 20mW
Full readout	20	following L1 trigger, extrapolate from CMS pixel
Sub-total	~80	
Total with DC-DC	**~106µW**	75% efficiency for DC-DC conversion

NB big uncertainties and several figures most likely to be **underestimates**

eg SEU-robustness, full control and timing, data volumes,….all required

essential to improve on this with real design work

Approximate parameters of trigger layers

For stacked layer (doublet)	
Pixel size	100µm x 2.5mm
ROC	8 x 128 channels
<Power>/pixel	175µW (250µW)
$\|\eta_{MAX}\|$	2.5
Bandwidth efficiency	100% (50%)

R [cm]	L [m]	A [m^2]	N_{face}	N_{chan}	N_{ROC}	N_{module}	N_{links}	P [kw]
25	3.0	9.6	64	38.5M	38k	4700	1440 (2880)	6.7 (9.6)
35	4.2	18.7	88	75M	73k	9200	2810 (5610)	13.1 (18.7)

With overlaps in R-ϕ or η expect additional 10-15%

present tracker ~35kW

Next steps

- Plan is to investigate these two basic ideas in a common activity
- Compare and contrast pros and cons of approaches, e.g.:
  - understand impact on material budget
  - understand implications of different choices for power or logic
  - identify building block circuits
  - understand requirements for commercial manufacture
    - including costs and scale of technological challenges
  - issues for module construction
    - especially power and cooling
  - practical issues
    - handling of z-offset, implementation of comparison logic,…
- Arrive at single concept for prototyping

Conclusions

- Modules which will provide trigger primitives look feasible
  - they will provide a new part in detector toolbox
  - but will contribute large fraction of future Tracker power and material
  - physics objectives will become clearer in 2-3 years and may evolve
- Crucial to improve understanding of power consumption
  - this is sensitive to occupancy and rejection factor
  - expect benefits from technology shrink but no magic solution
- Off-detector processing of huge data volumes may also not be straightforward – as well as trigger algorithms…
  - so prototype module development is now timely
- "Conventional" assembly may be feasible
- Commercial manufacture, exploiting technology progress, may have important role