# Commissioning and performance of the Preshower off-detector readout electronics in the CMS experiment

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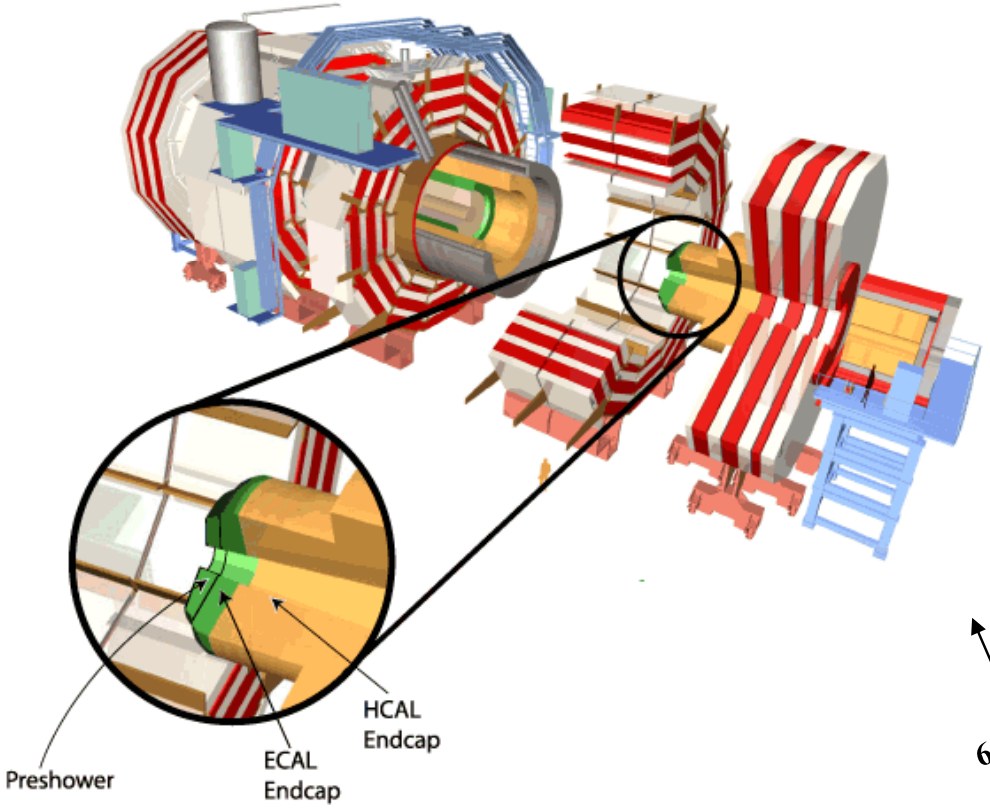
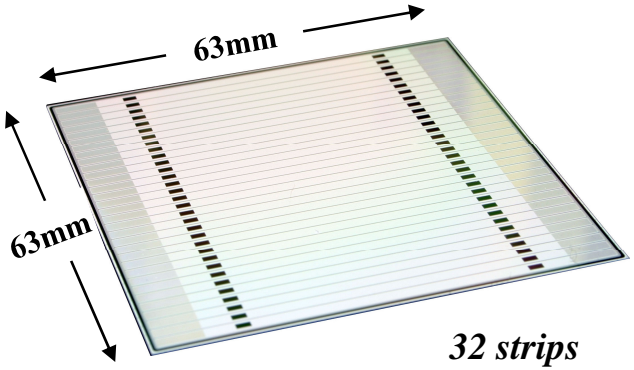
6: **University of Ioannina**, *Ioannina, Greece*

# CMS Preshower location & objective



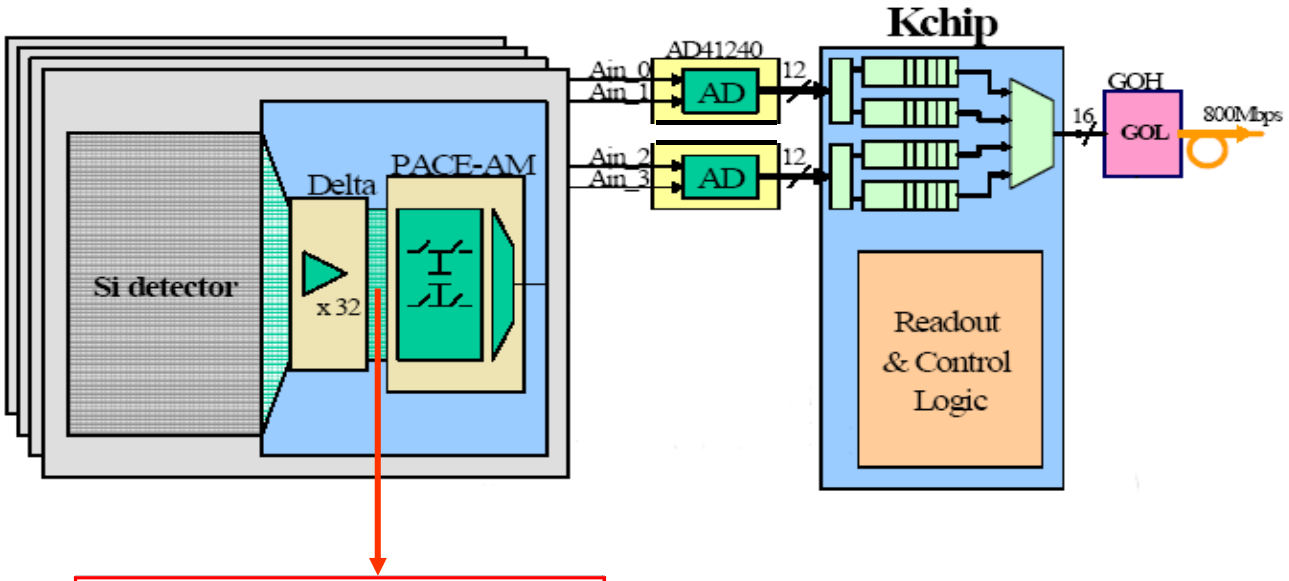
- ✓ fine grain detector placed in front of the endcap ECAL.
- ✓ detects photons with good spatial resolution in order to perform $\pi^0$ rejection.
- ✓ comprises ~4300 32-strip silicon sensors (~ 130 000 strips in total).

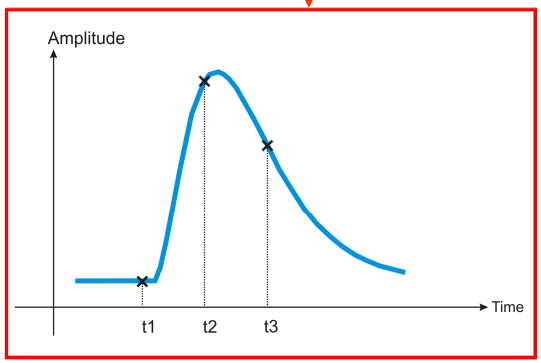


# On-detector electronics readout scheme






The signals from each strip are:
- amplified, shaped (Delta)
- sampled continuously every 25ns &
  stored in an analogue memory (PACE-AM)

On reception of a L1 trigger 3 consecutive samples are:
- recalled from the analog memory
- digitized by 12-bit ADCs (AD41240).
- organized in 299 16-bit word packets (K-chip)
- transmitted through an 800Mbps optical link (GOL).

In total, 1208 data links need to be readout

# The CMS Preshower Data Concentrator Card (ESDCC)



✓ What: multi-FPGA 9U VME boards that read out up to 36 GOL fibres.

✓ How: based around two major FPGA-based components:
the 9U VME "host board" & the optical receiving plug-in modules ("optoRx")

✓ 40 ESDCCs (4 VME crates) are used for the readout of the Preshower detector.

✓ The ESDCCs should perform significant data reduction (at least factor of 10) since the total available downstream bandwidth of the central DAQ system is ~8GB/s and the data flow from the detector is ~72GB/s.

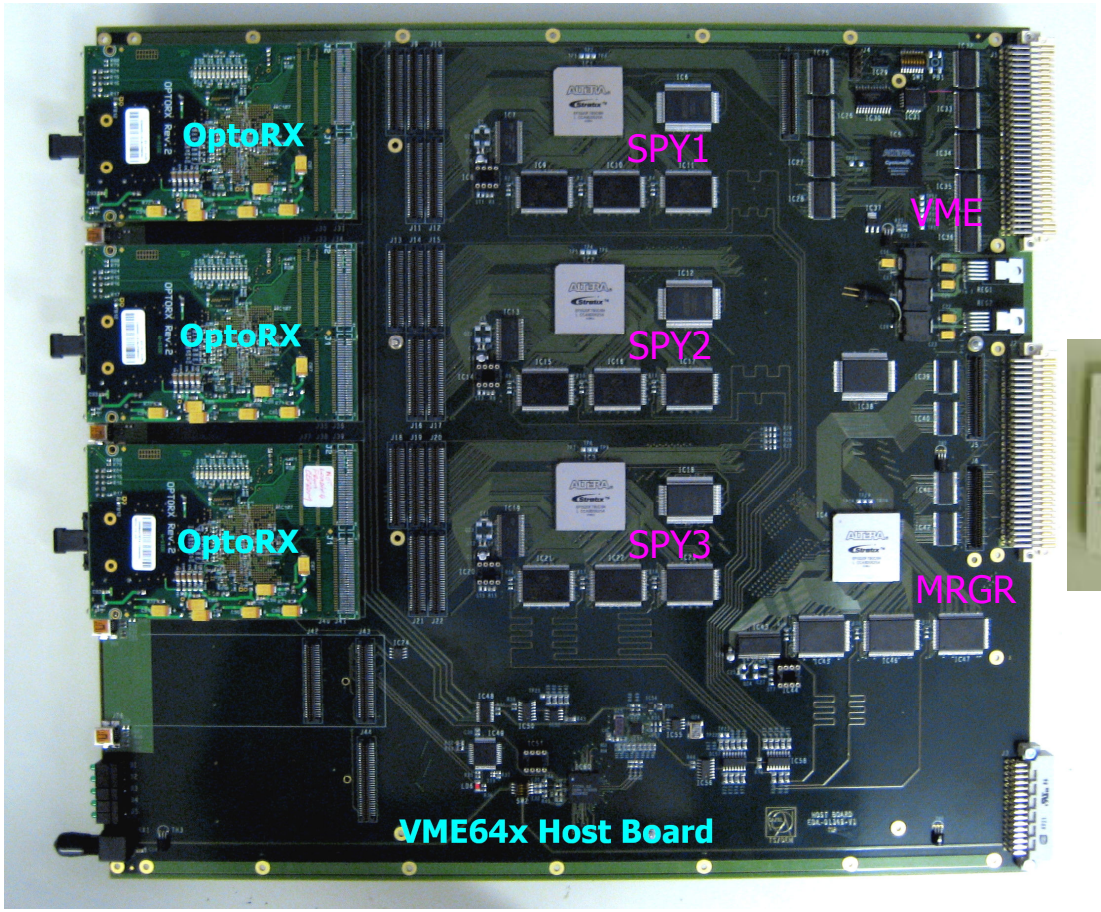
✓ The data reduction includes pedestal subtraction, gain adjustment, common mode rejection, bunch crossing identification & threshold application

✓ The required level of data reduction is feasible because the Preshower has relatively low occupancy of 2% (maximum average occupancy)

✓ Developed in collaboration with TOTEM

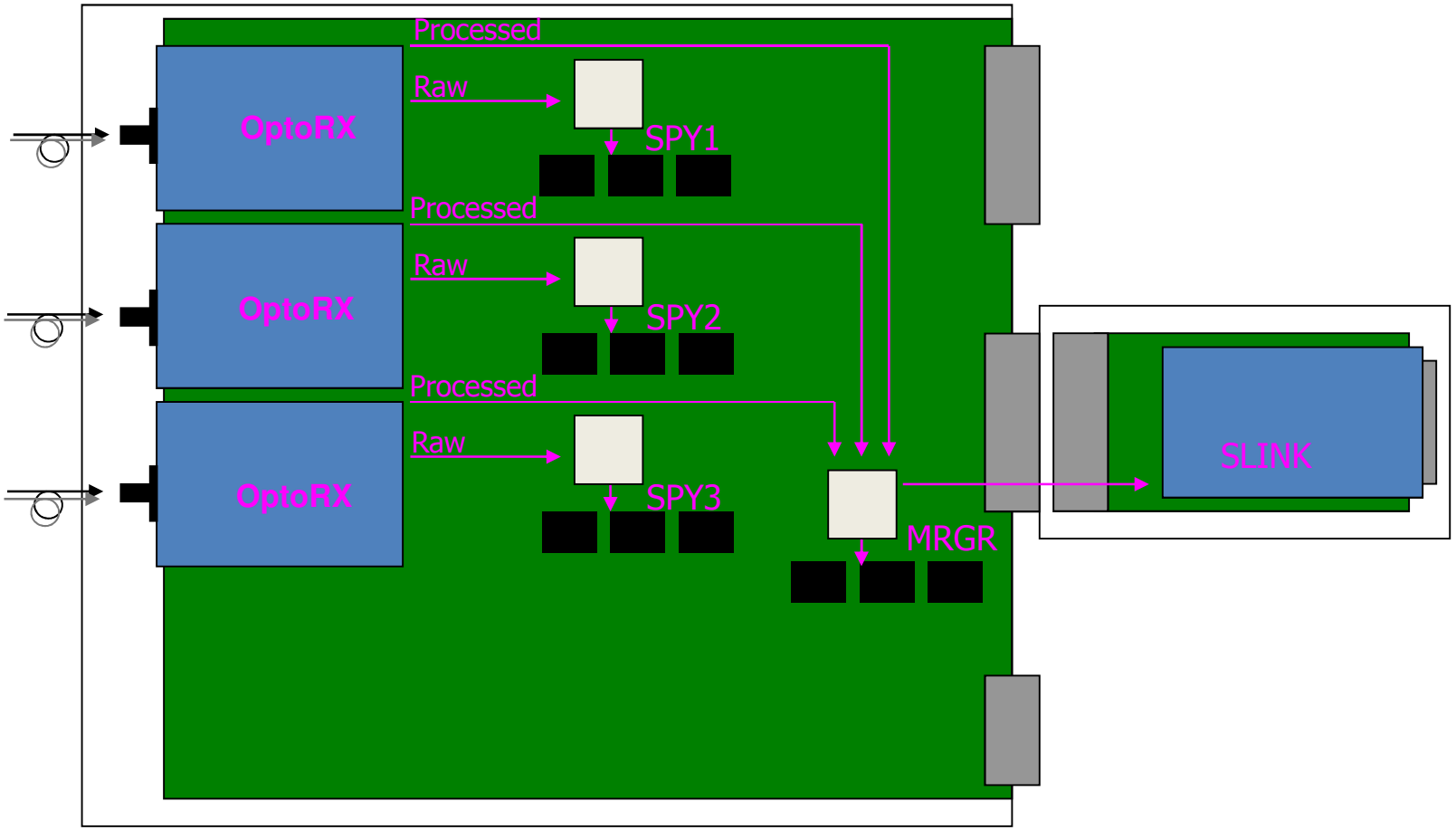
# The CMS Preshower Data Concentrator Card (ESDCC)






# The CMS Preshower Data Concentrator Card (ESDCC)






OptoRX FPGAs: Gigabit link reception, Data Reduction/Zero Suppression

MRGR FPGA: interface to DAQ

SPY FPGAs: raw data spying (on-demand)

# Outline



A. Hardware commissioning (after production) of the "host board" & the "optorx" modules

B. Hardware & Firmware commissioning of the ESDCC as a whole

C. Overall performance of the ESDCC (Hardware, Firmware & Software) at CMS

# ESDCC HW commissioning - introduction



- ✓ Motivation: To have a system for the verification of the hardware production.
- ✓ Experience with system comprising modern FPGAs (~1000pin BGA packages) has shown that connectivity tests between components on-board is essential.
- ✓ Since the two major components have been developed separately, two independent systems performing connectivity tests have been developed.
- ✓ Targeted for tests at production site & reception tests at CERN.

# Connectivity testing - concept

To verify one connection line, the line must be toggled from the one end and read/verified on the other end.

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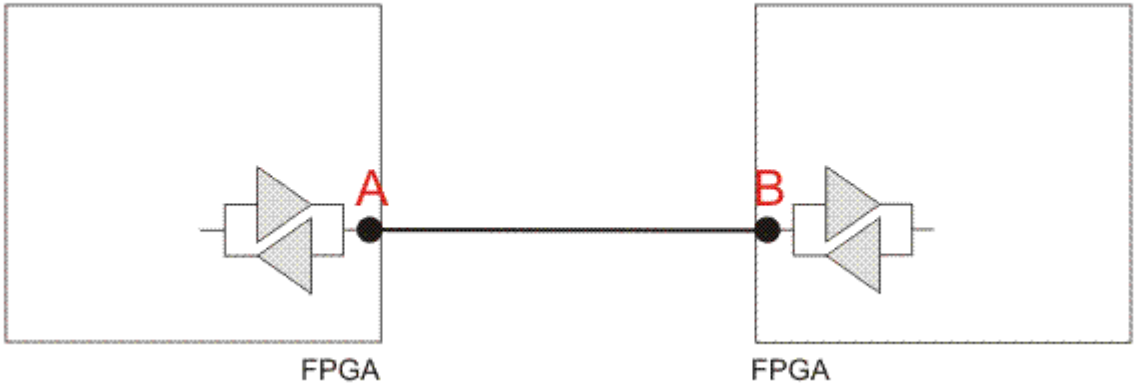
# Connectivity testing - concept

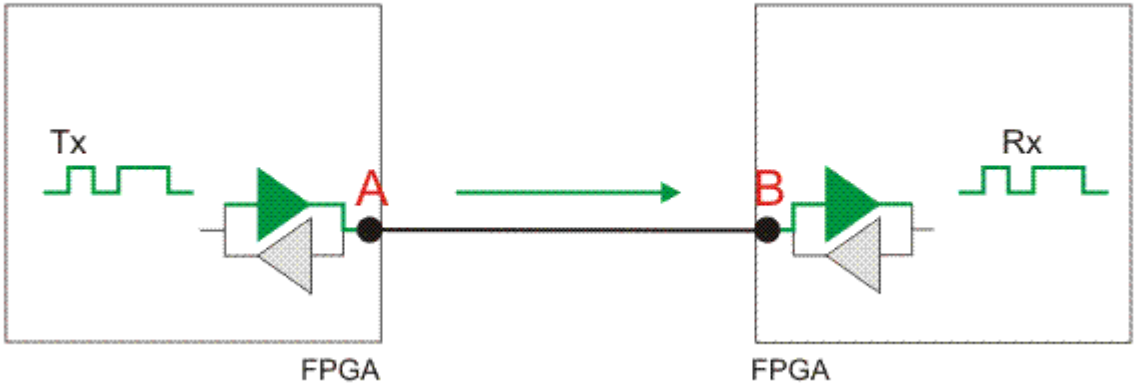


CLOSED LOOP: A=FPGA I/O, B=FPGA I/O



# Connectivity testing - concept

CLOSED LOOP: A=FPGA I/O, B=FPGA I/O
When bidirectional path, Tx & Rx can be freely defined



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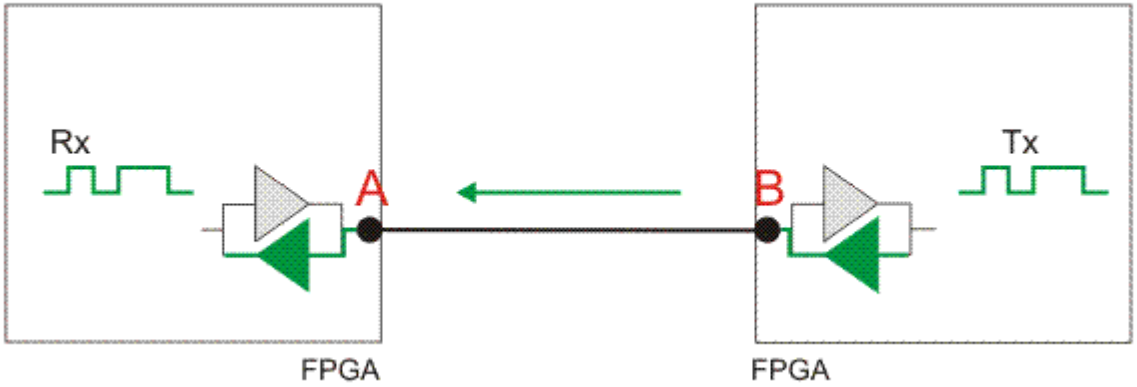
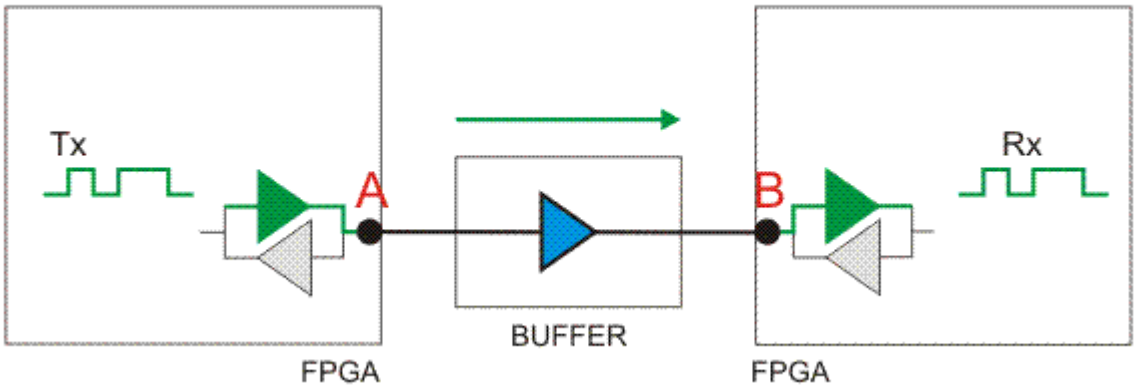


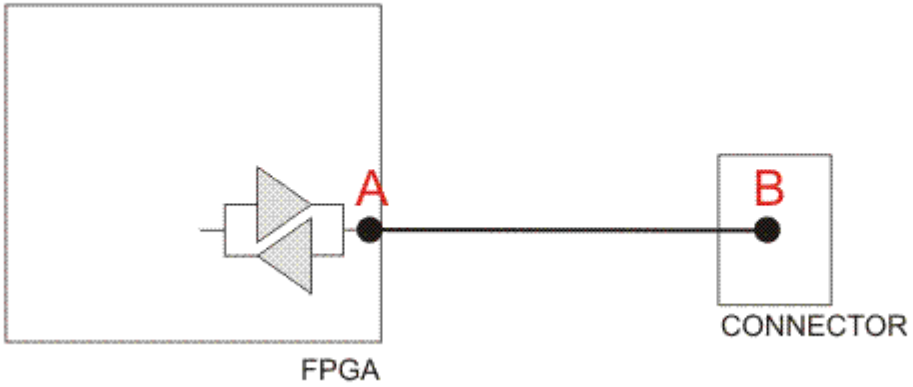
CLOSED LOOP: A=FPGA I/O, B=FPGA I/O
When unidirectional path, Tx & Rx defined appropriately



# Connectivity testing - concept

OPEN LOOP: A=FPGA I/O, B=connector pin

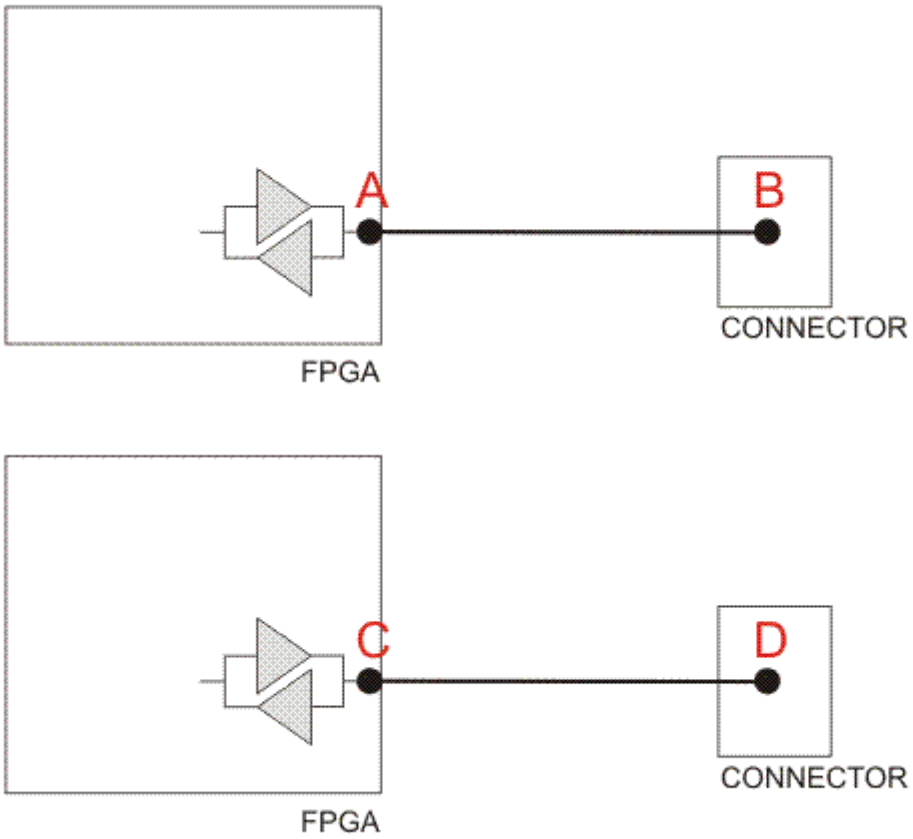
Problem: How to test?



# Connectivity testing - concept

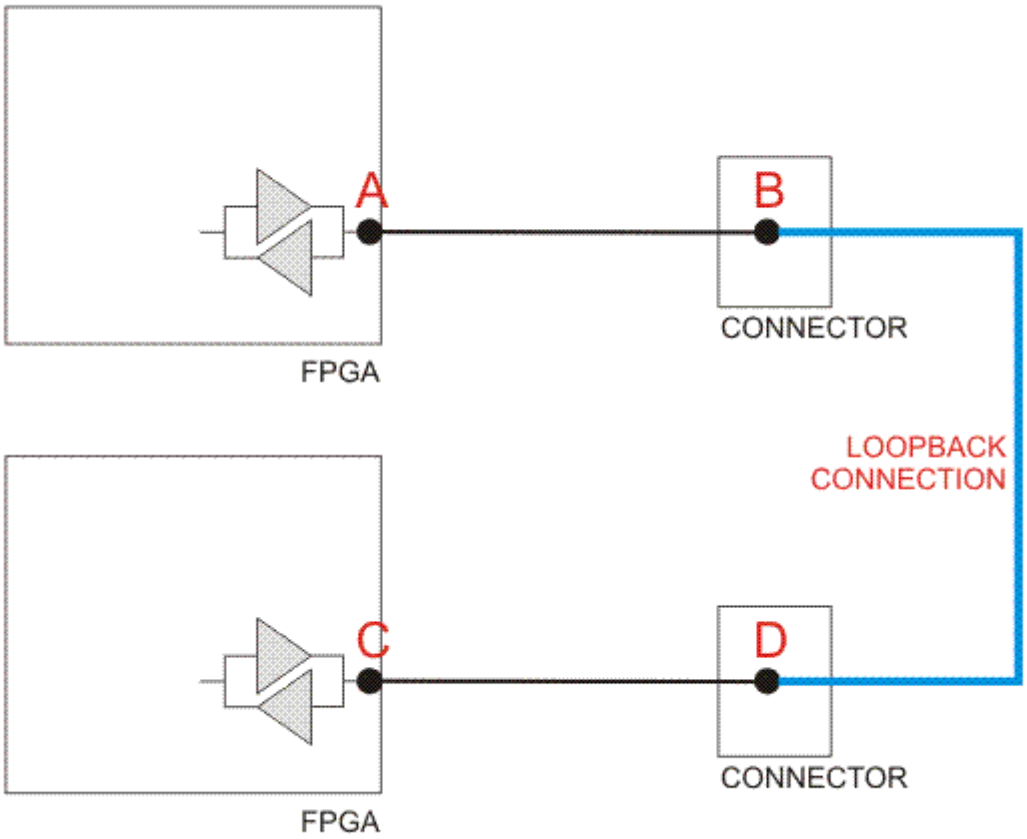


OPEN LOOP: A=FPGA I/O, B=connector pin
Solution: Testing in pairs

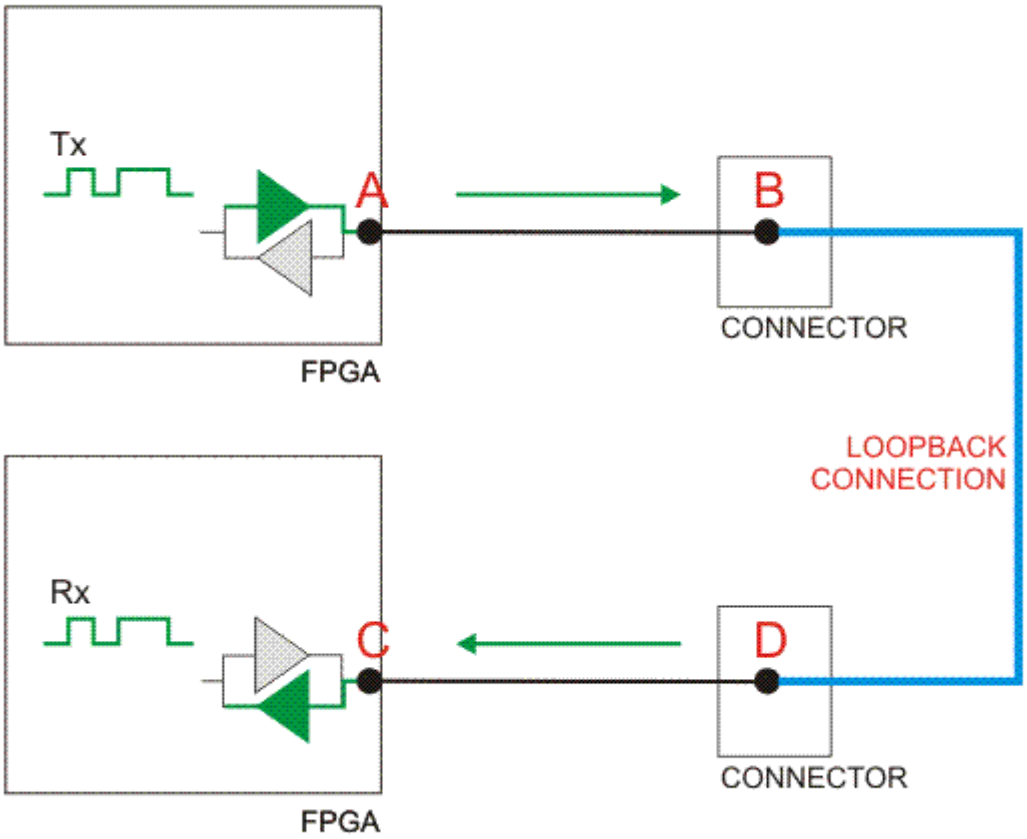


OPEN LOOP: A=FPGA I/O, B=connector pin

How: by adding connections (cable or PCB) that close the open loops

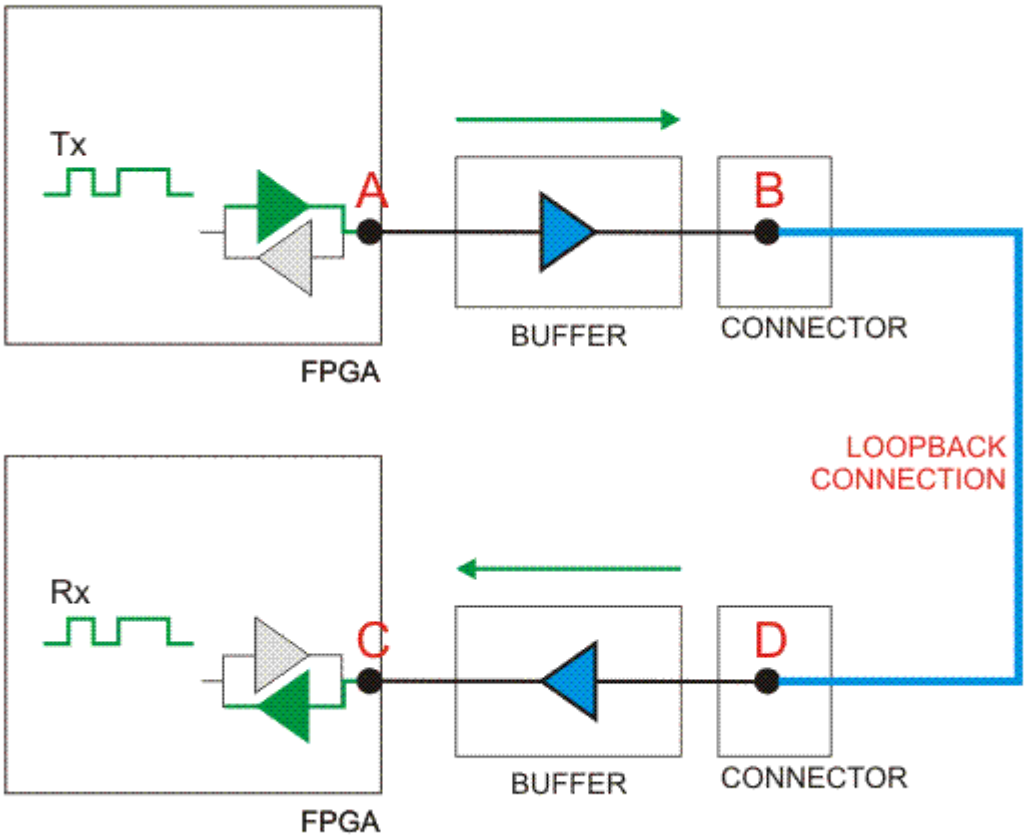


OPEN LOOP: A=FPGA I/O, B=connector pin
Then: Treated as closed loops



OPEN LOOP: A=FPGA I/O, B=connector pin

Restriction: When unidirectional paths, pairs must be defined appropriately



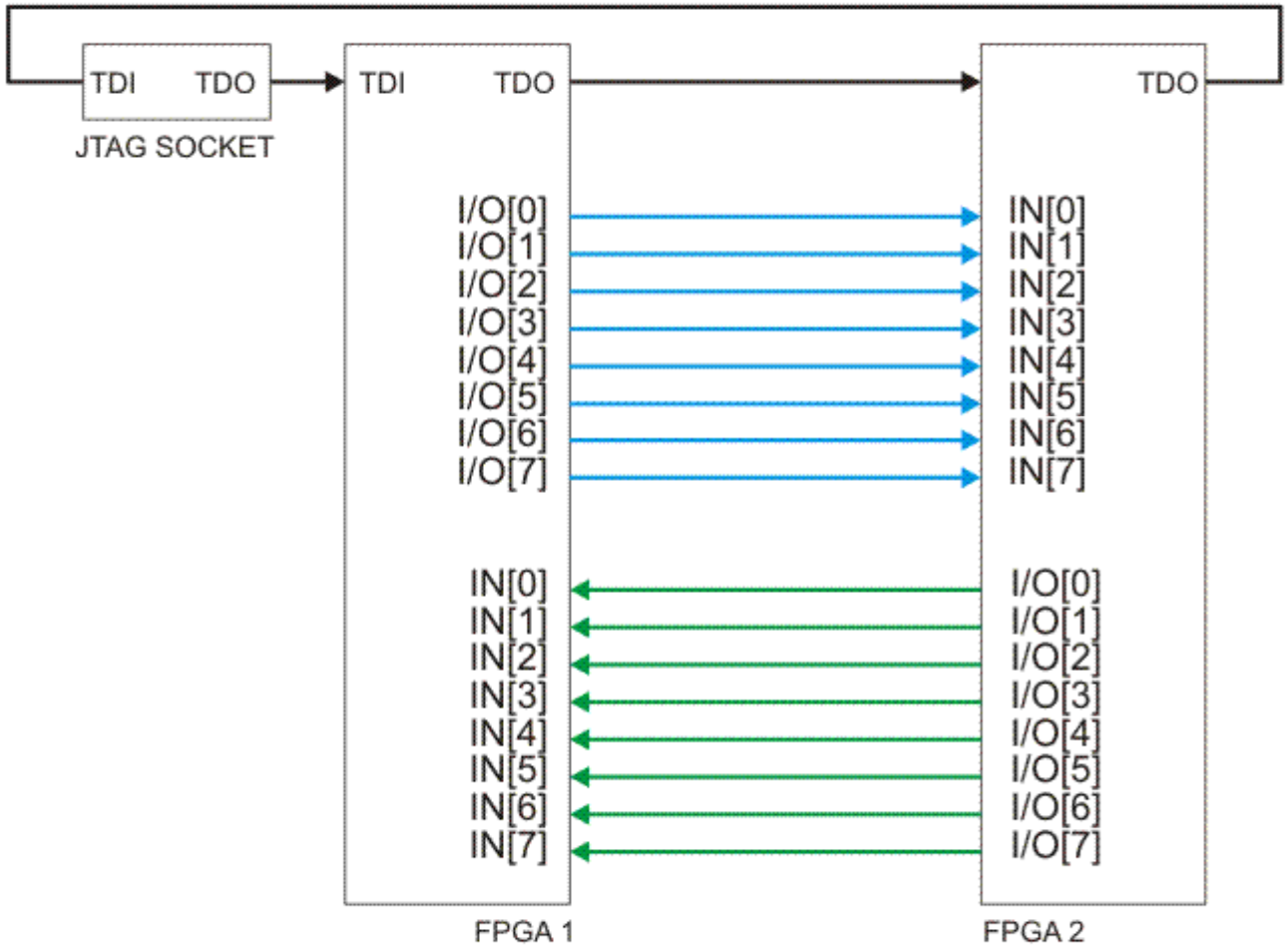
Which tools are needed?

- ✓ FPGA Embedded Logic Analyzers through JTAG, part of the FPGA development package.
- ✓ Typical JTAG FPGA download cable.

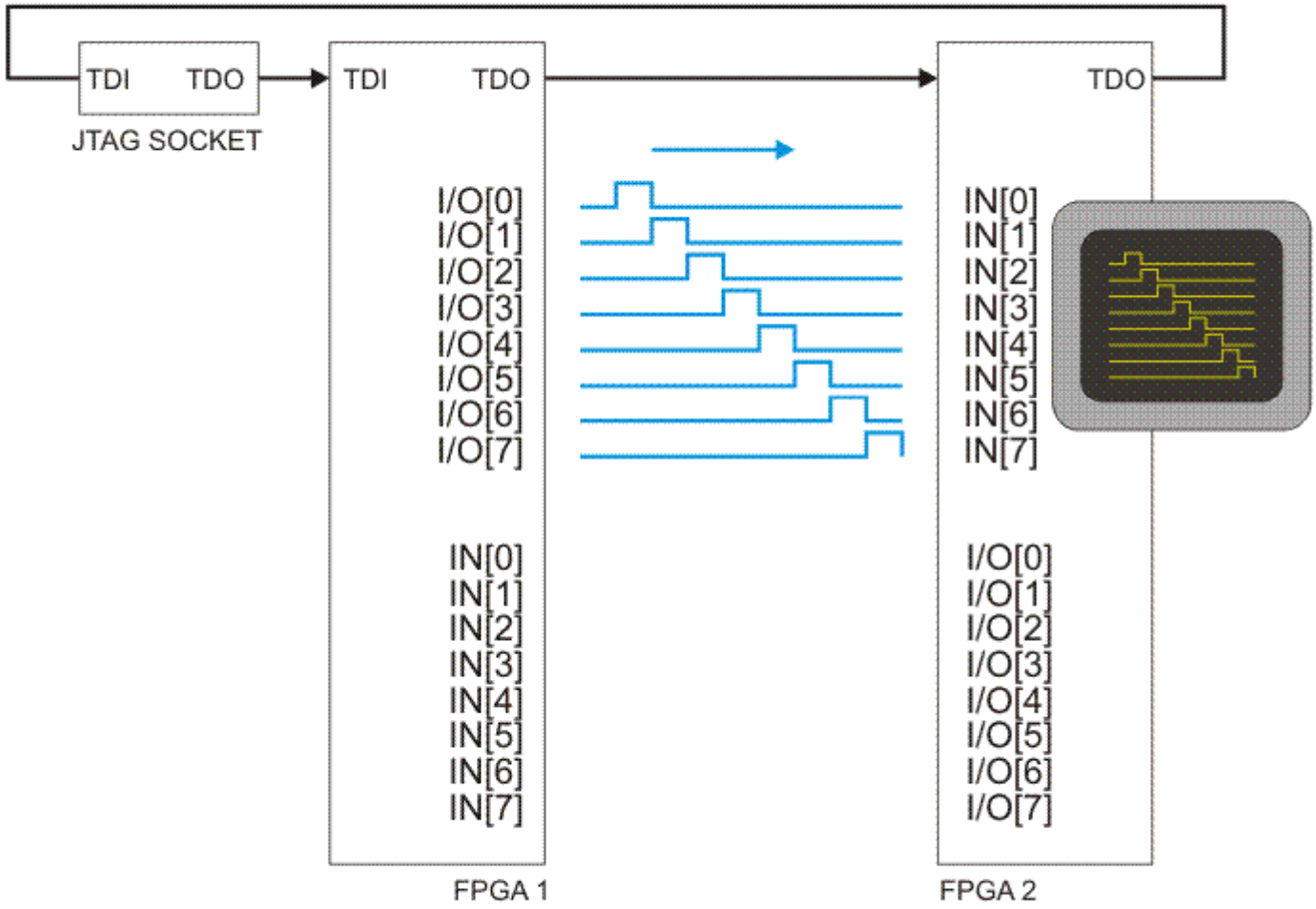
How to readout the expected Rx pattern?

- ✓ Configure the "Tx" FPGA to generate patterns in the output bus.
- ✓ Configure the "Rx" FPGA to attach a logic analyzer to its input bus.
- ✓ Enable the logic analyzer, trigger in one of the inputs and get results.
- ✓ Analyze the results & compare with expected.

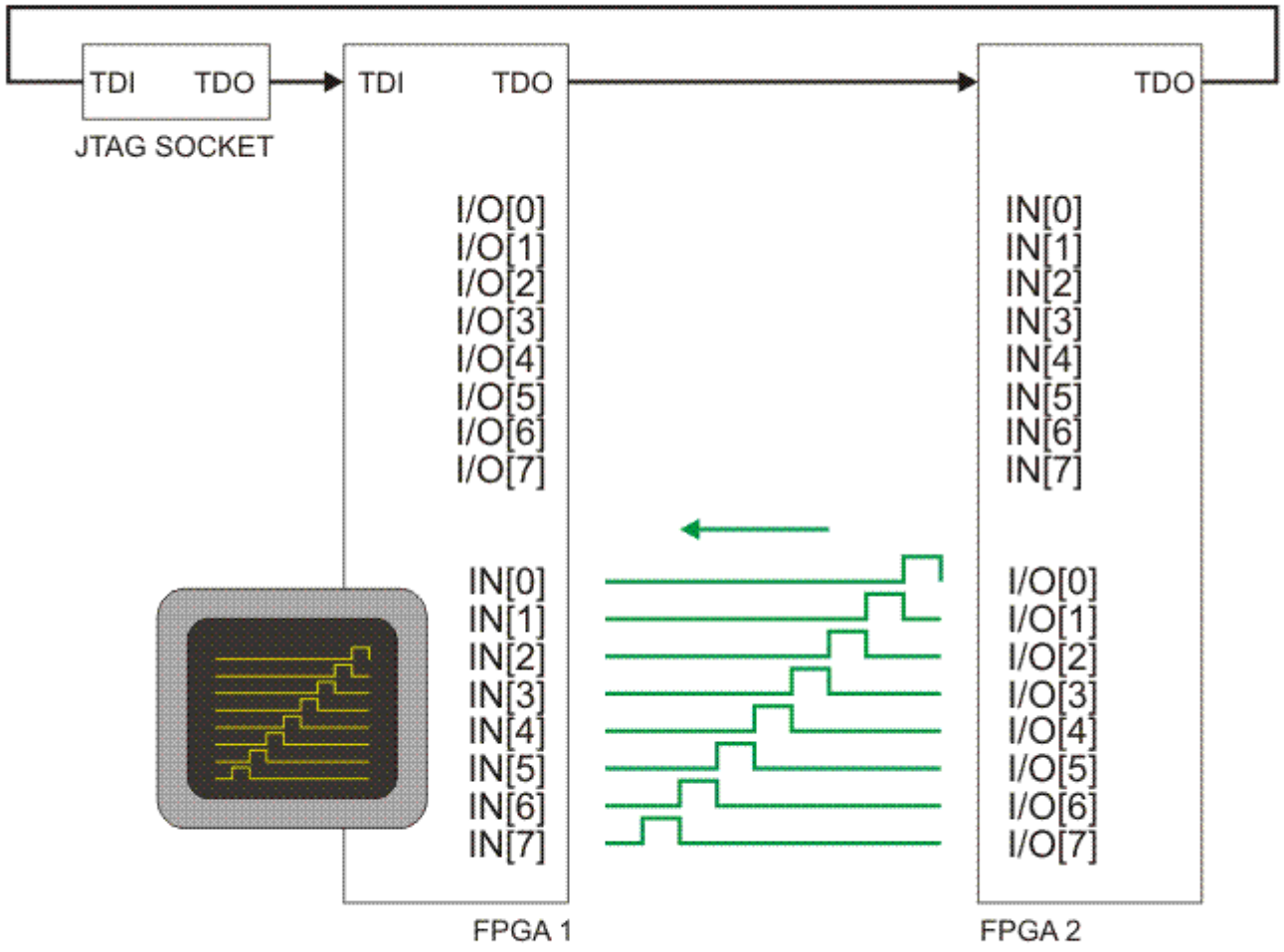
Two FPGA example: two unidirectional buses to test
Bus A: FPGA1 → FPGA2, Bus B: FPGA2 → FPGA1



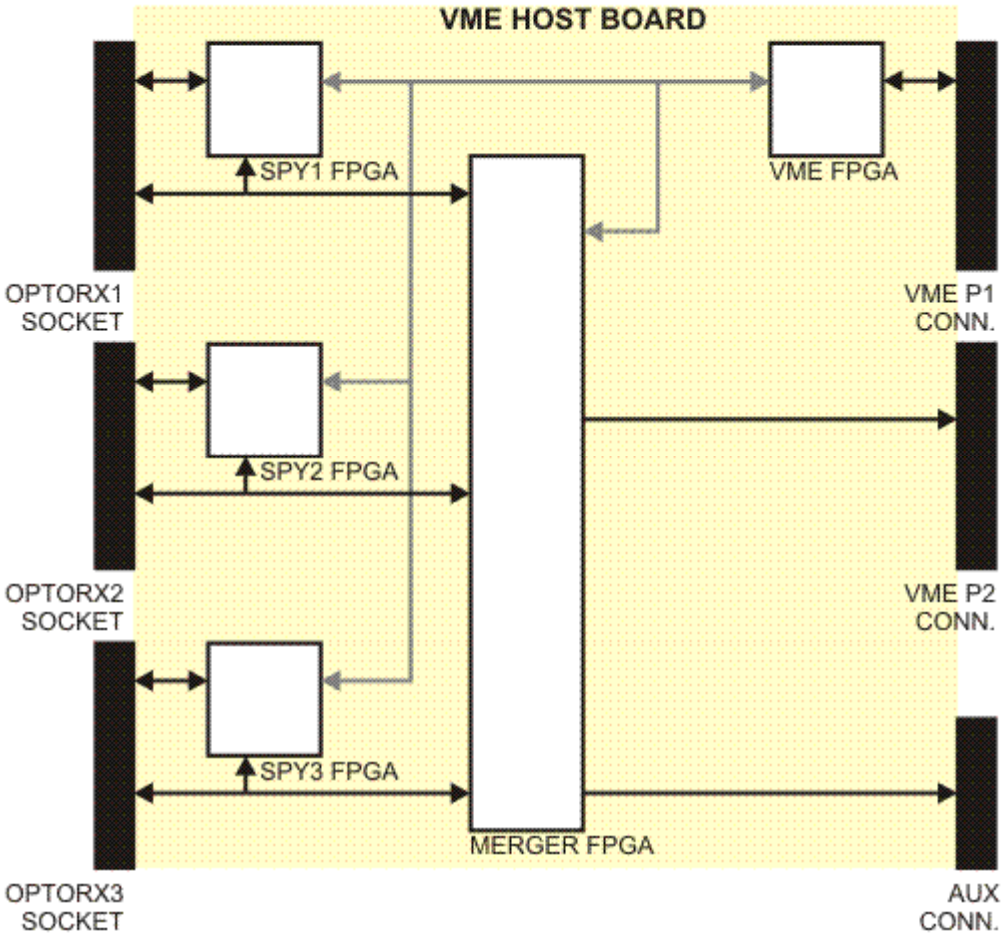
Phase1:Tx: FPGA1. Rx: FPGA2 (with embedded logic analyzer)



Phase2: Tx: FPGA2. Rx: FPGA1 (with embedded logic analyzer)



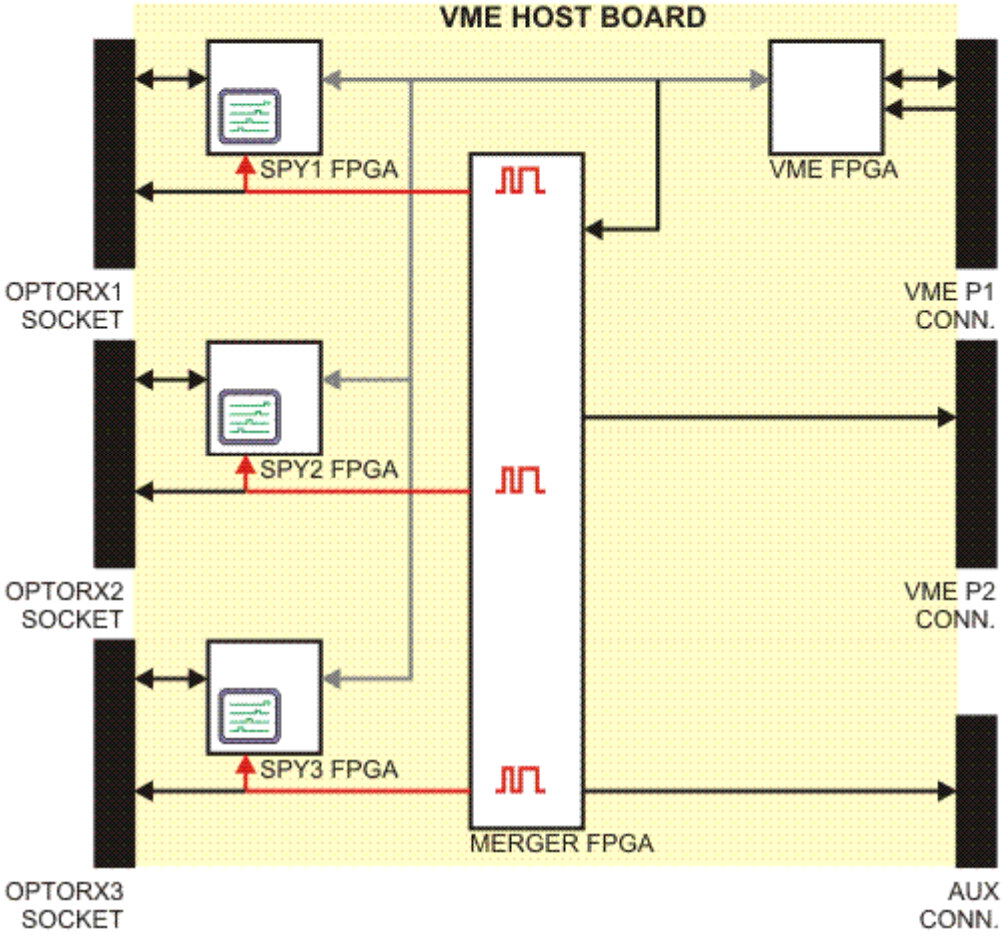
Testing in 4 phases (4 different sets of firmware)



# Connectivity testing - VME host board: implementation

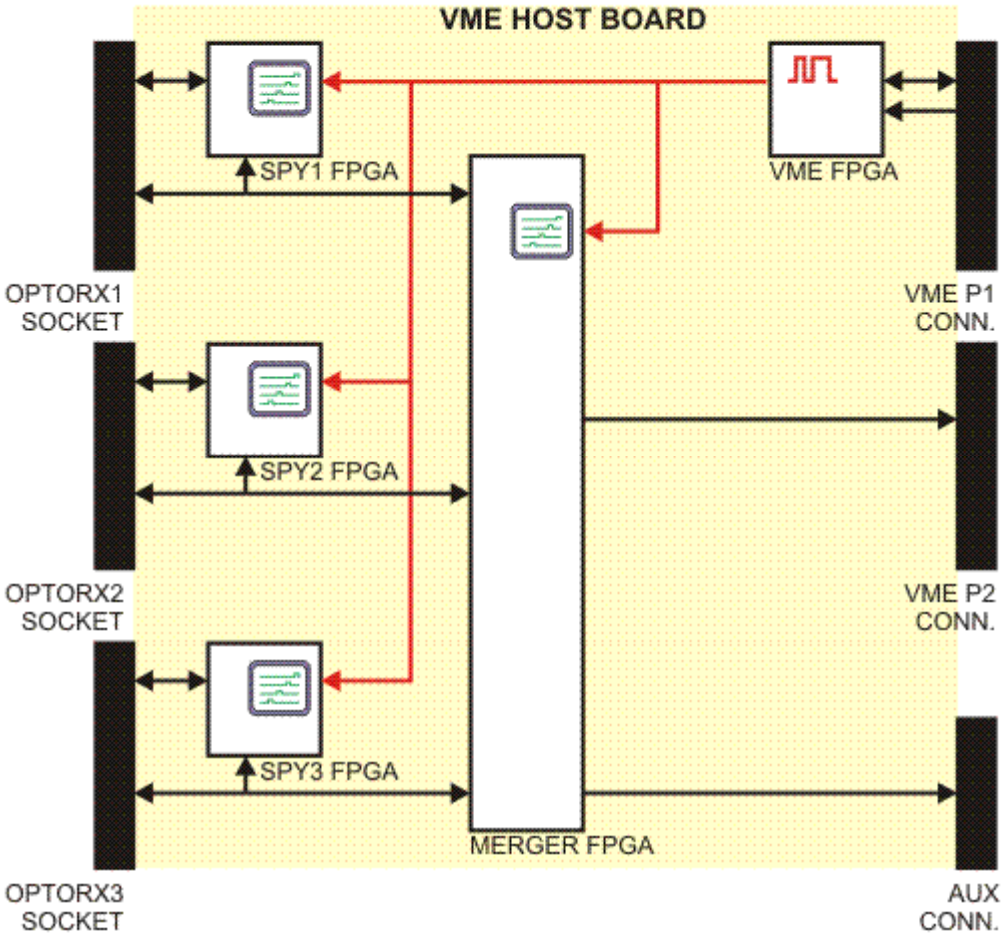


Phase1: CLOSED LOOP
Tx: MERGER. Rx: SPY1, SPY2, SPY3

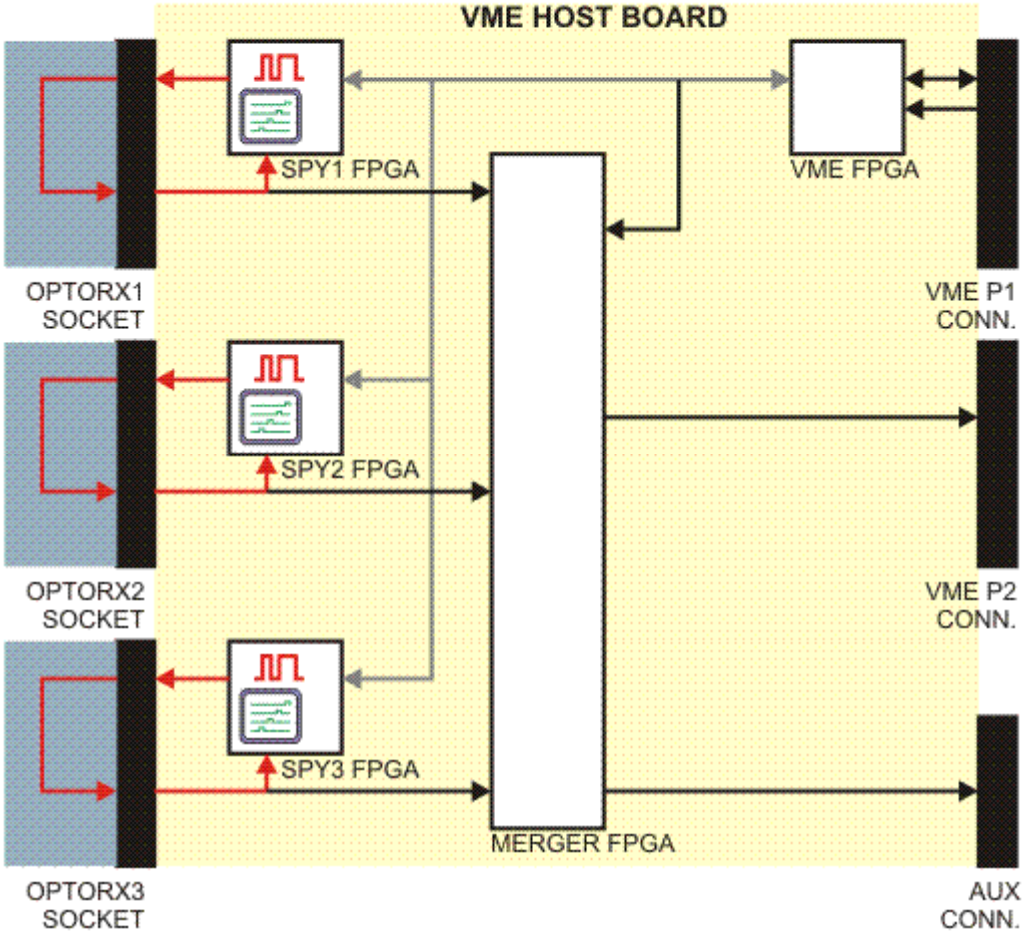


Phase2: CLOSED LOOP

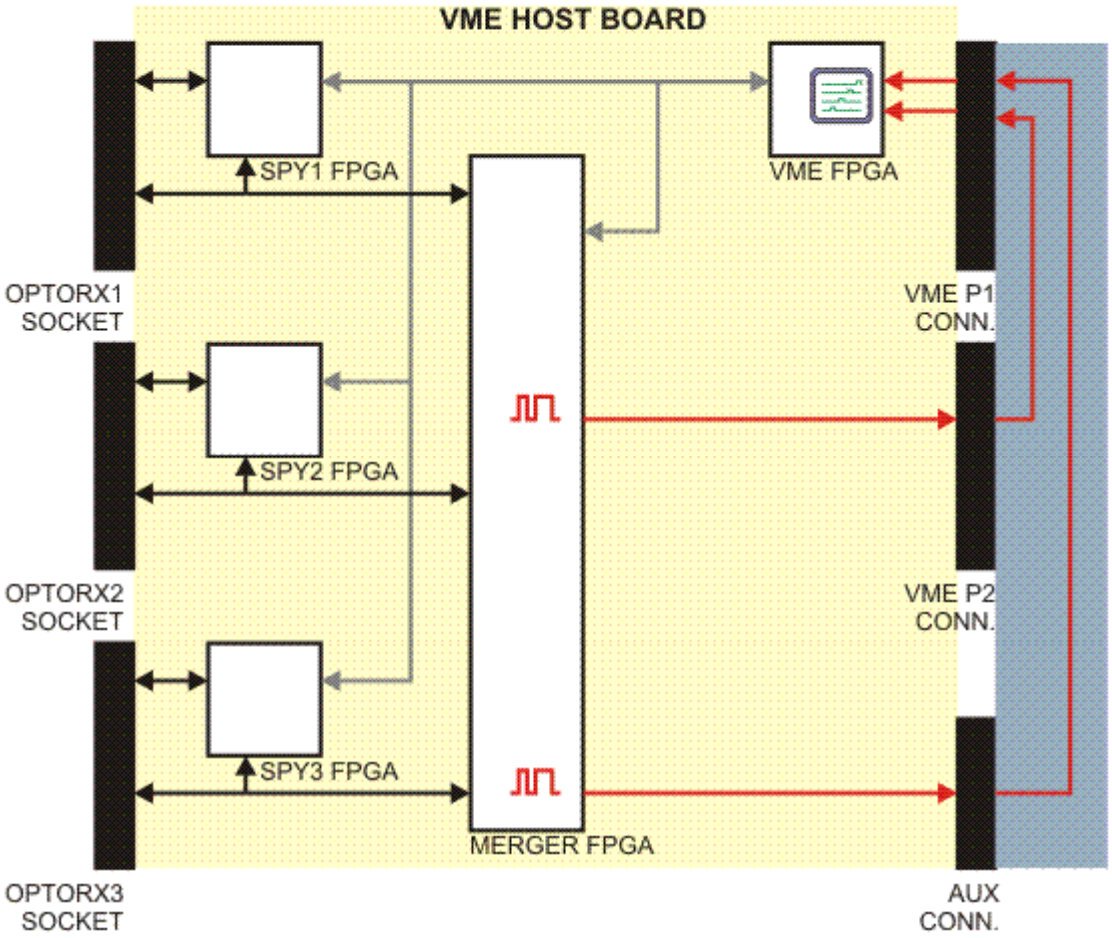
Tx: VME. Rx: SPY1, SPY2, SPY3, MERGER



Phase3: OPEN LOOP (loopback connections used)
Tx: SPY1, SPY2, SPY3. Rx: SPY1, SPY2, SPY3

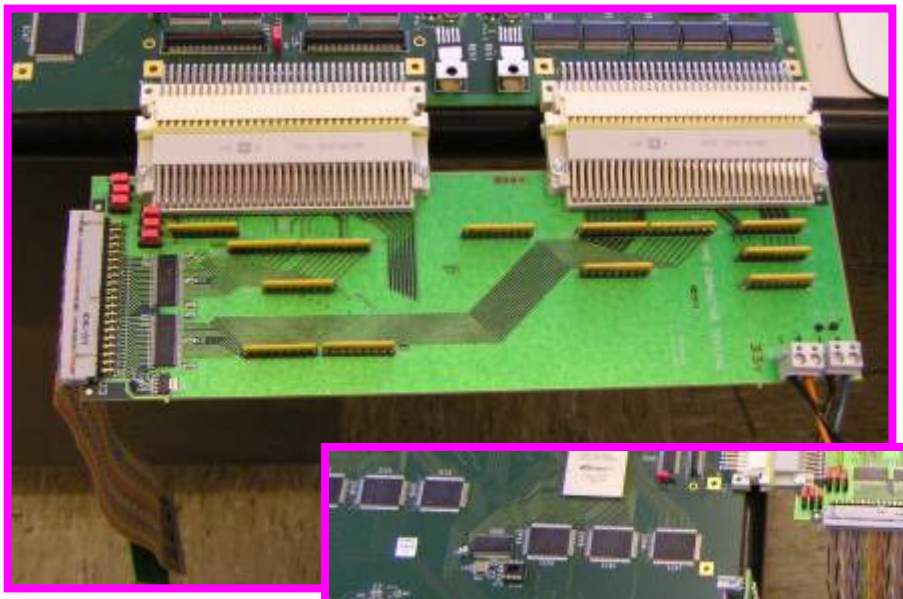


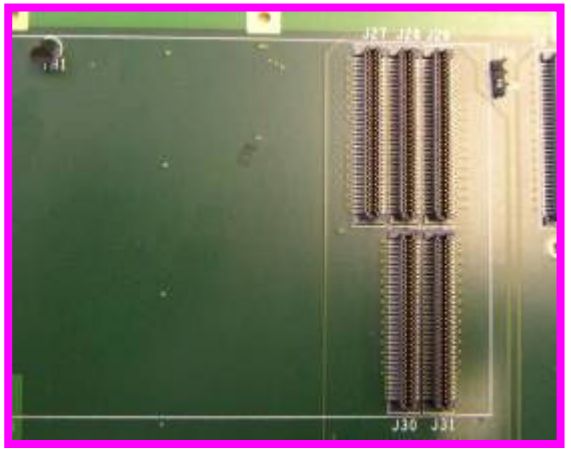
Phase4: OPEN LOOP (loopback connections used)
Tx: MERGER. Rx: VME

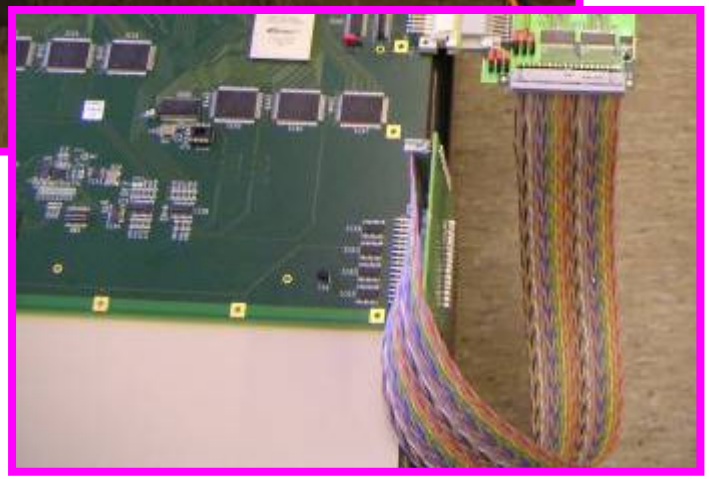


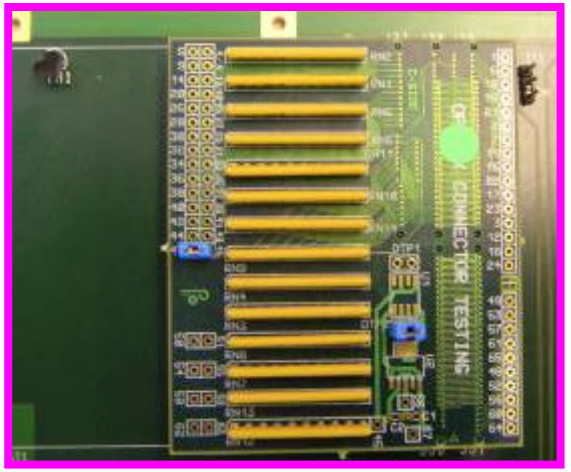
# Connectivity testing - VME host board: pictures



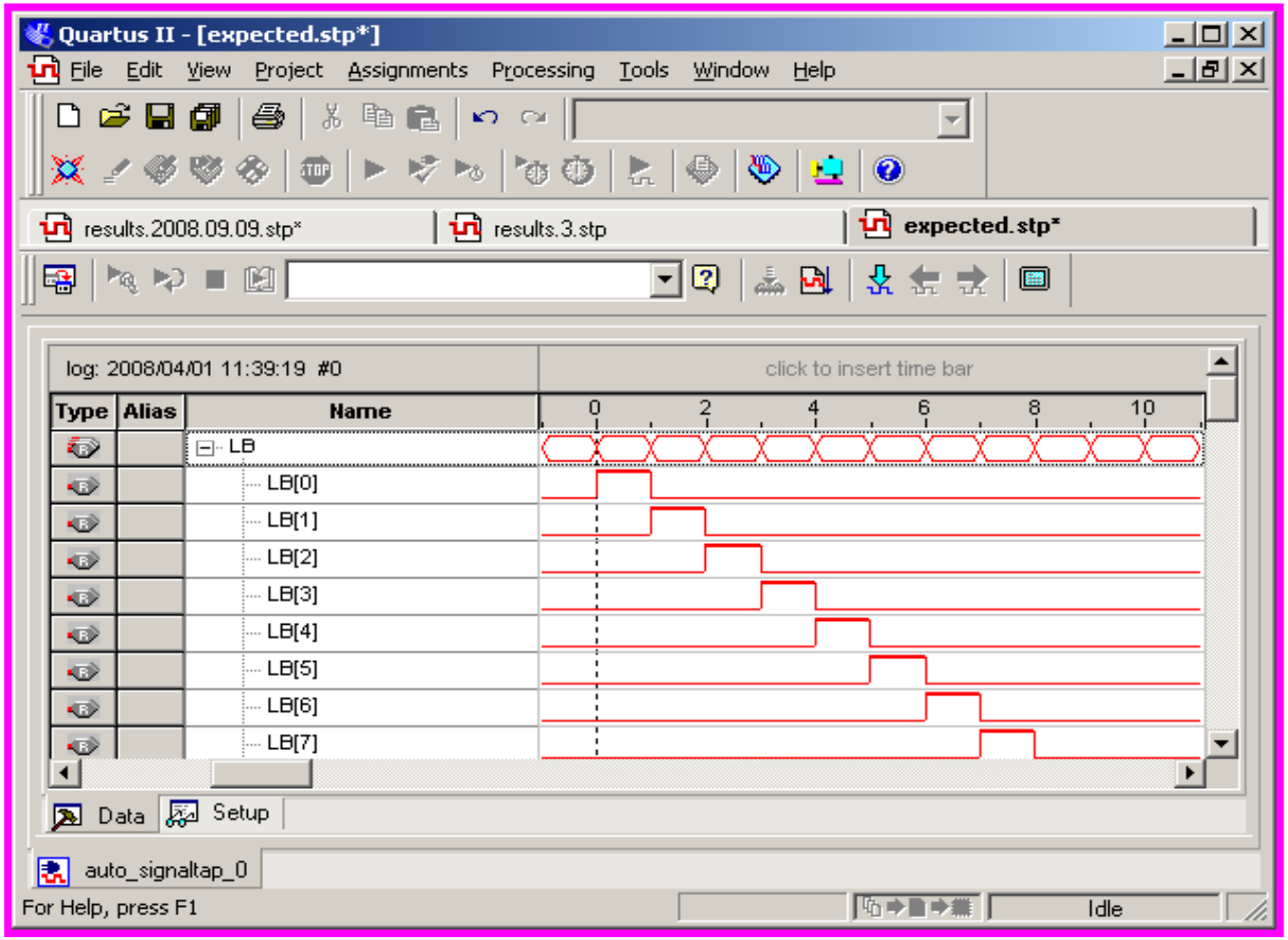








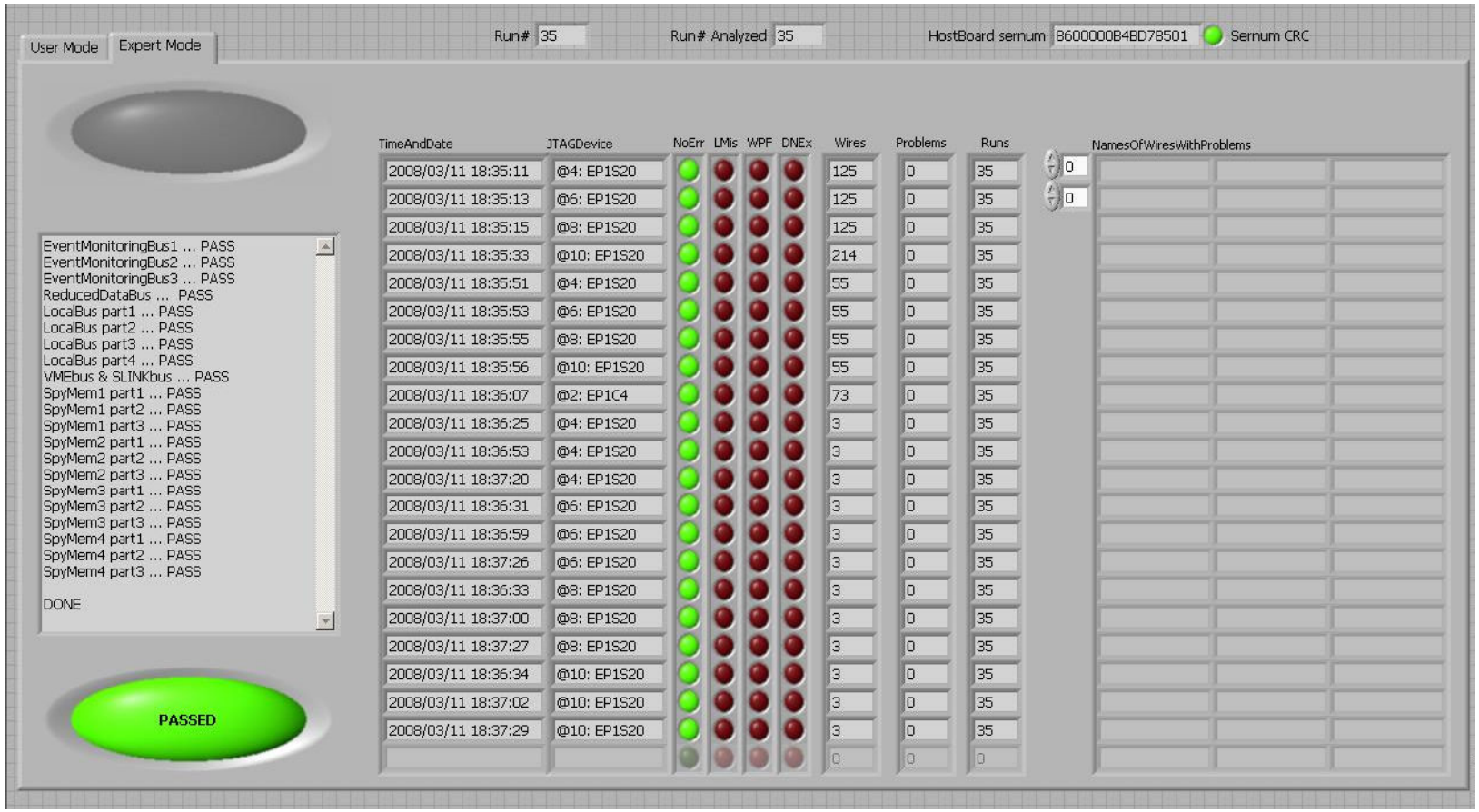

## The FPGA vendor Embedded Logic Analyzer GUI



# Connectivity testing - VME host board: software



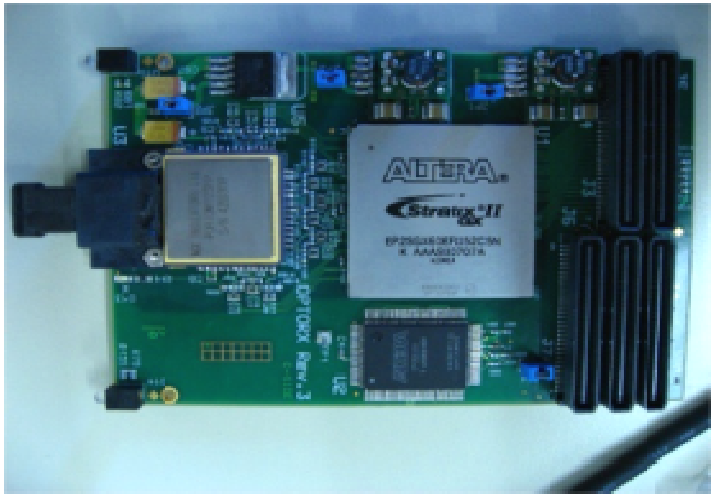
## The top level testbench application (LabVIEW)



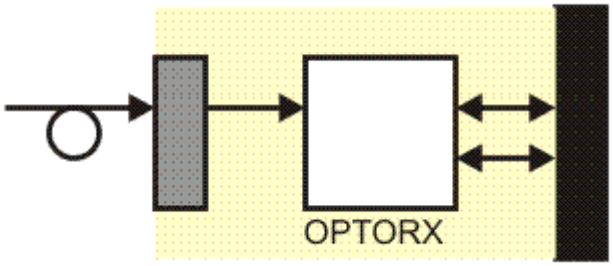

- ✓ Efficiency: 97% of connections tested (In total, ~2000 connections)
- ✓ Test Duration: 300s
- ✓ Results: Serious problems found in first production – improved the process for final production

# Connectivity testing - OptoRx

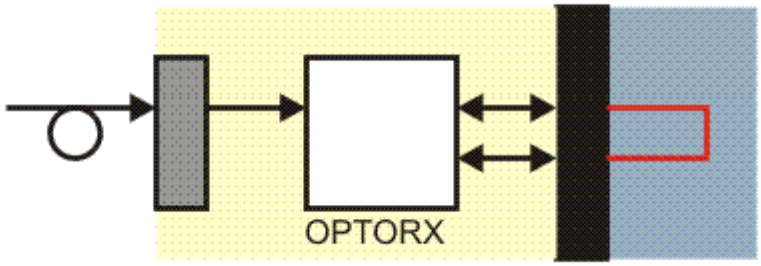




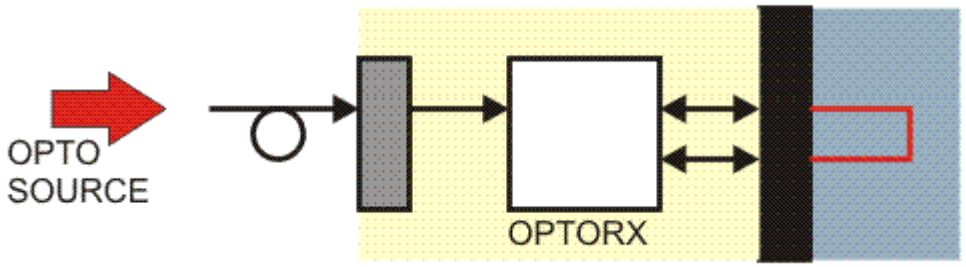
TWO OPEN LOOPS:
1: FPGA I/O to connector. 2: Optical Receiver to FPGA IN



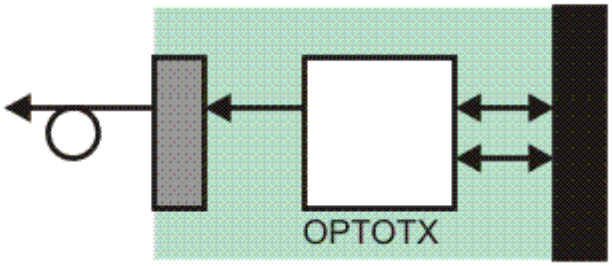
OPEN LOOP1:
Loopback connection



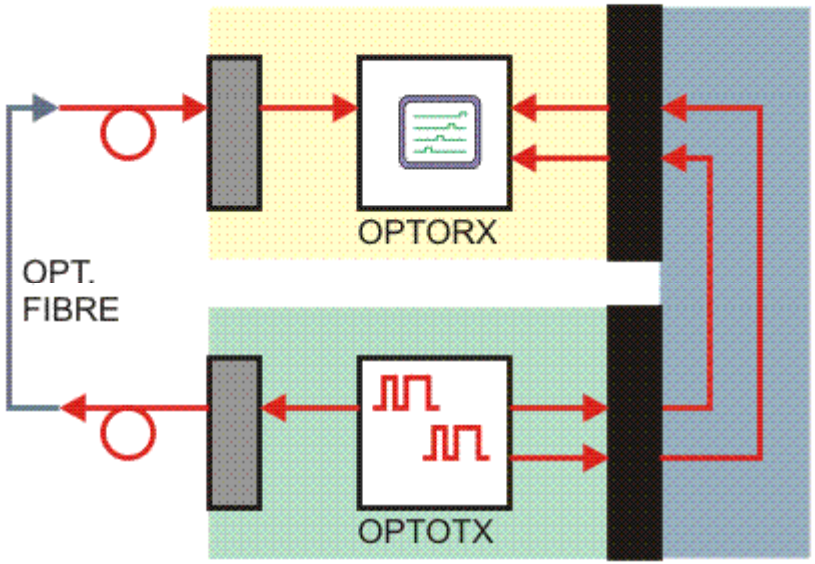
OPEN LOOP2:
Multichannel optical source needed



Different approach:
Develop new Module (pin-to-pin) but with optical transmitters

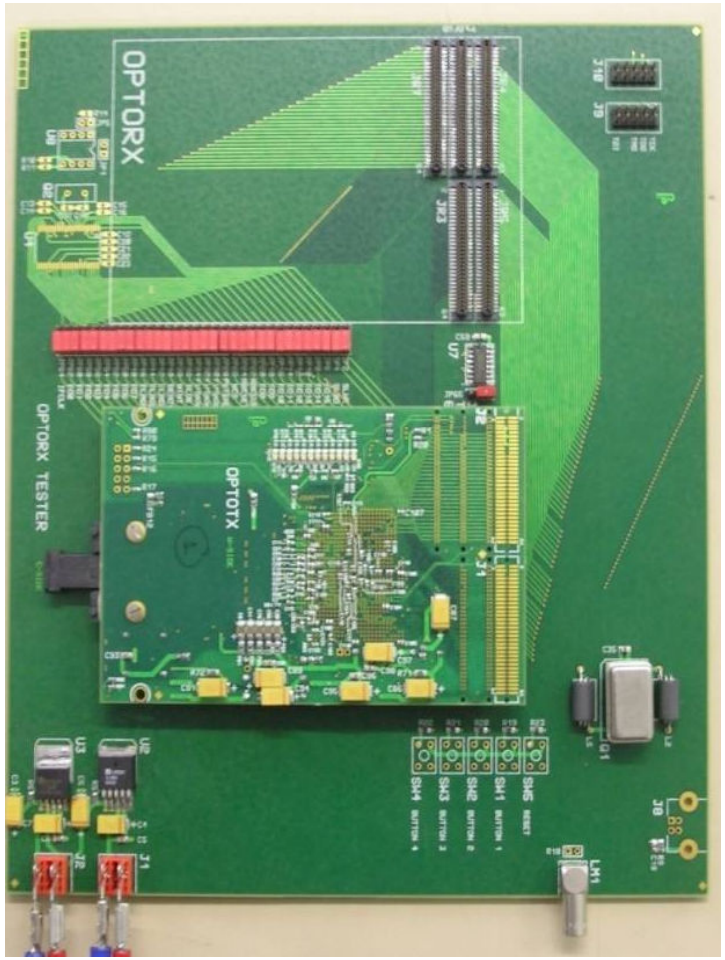


Testing Scheme:
Tx: OPTOTX. Rx: OPTORX



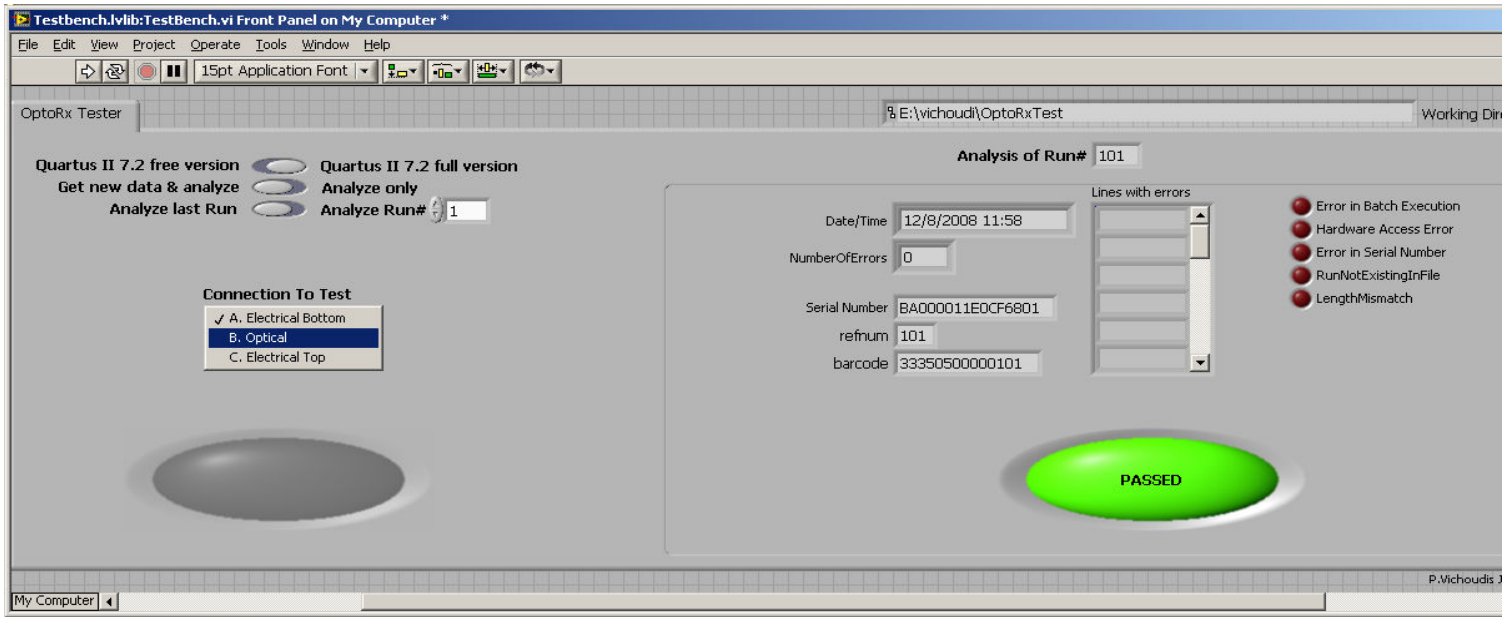
# Connectivity testing - OptoRx: pictures

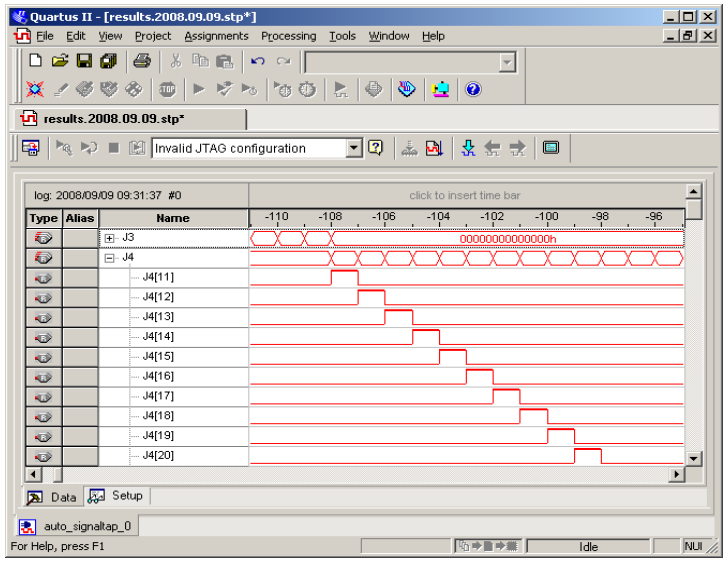




# Connectivity testing - OptoRx: software






- ✓ Efficiency: 100% of connections tested (out of ~400 connections)
- ✓ Test Duration: 60s
- ✓ Results: ~5% defective modules found (out of ~150 modules produced)

- For the commissioning of the ESDCC, functional tests need to be performed.
- To verify its functionality, 36-ch optical source needed.
- Instead of real Preshower hardware, the ESDTE (ES Data Traffic Emulator) was developed and used.

ESDTE

✓ What? a multi-FPGA optical VME-based system that drives the ESDCC

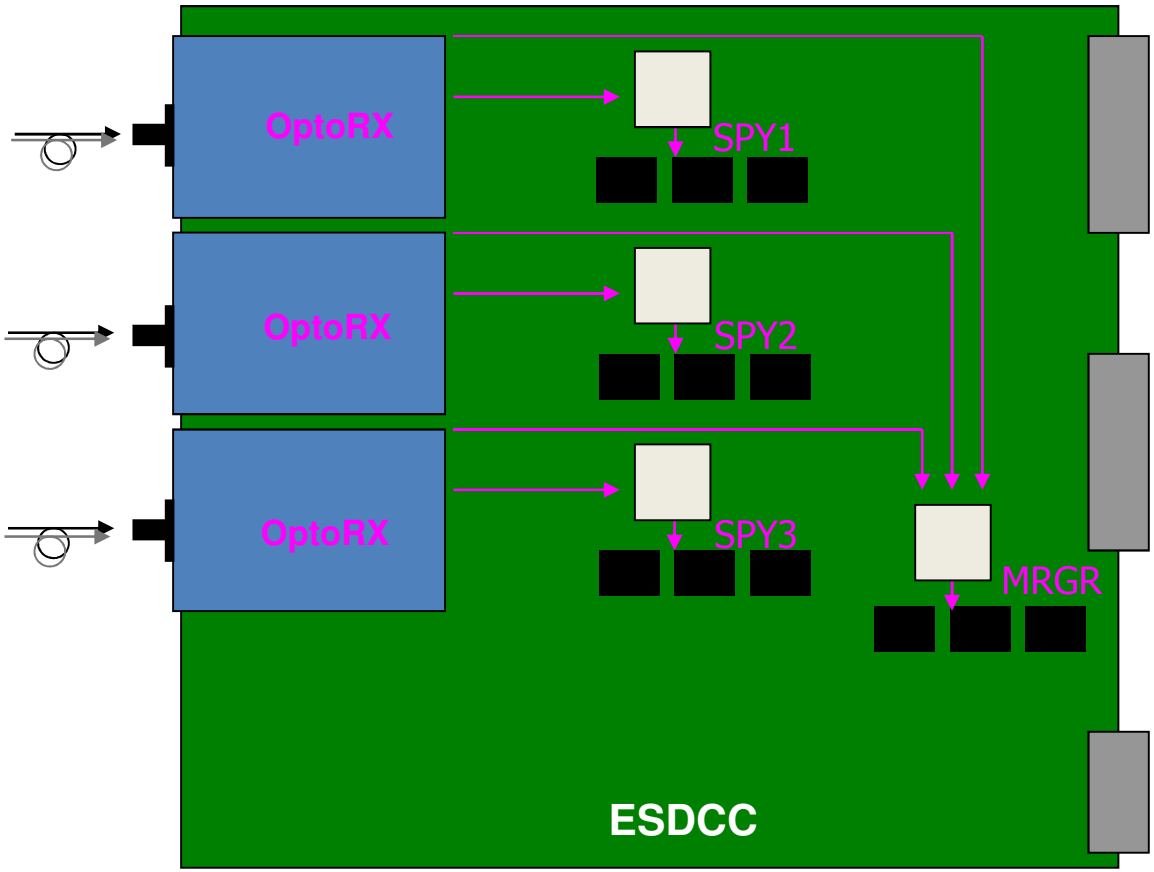
✓ Why? ability of producing special sequences & error conditions
(not easy to produce them systematically with real hardware)

- Data integrity errors
- Synchronization problems
- Interrupt packet transmission
- Do not send a packet (emulate missing triggers)
- Send a packet w/out trigger (emulate spurious triggers)

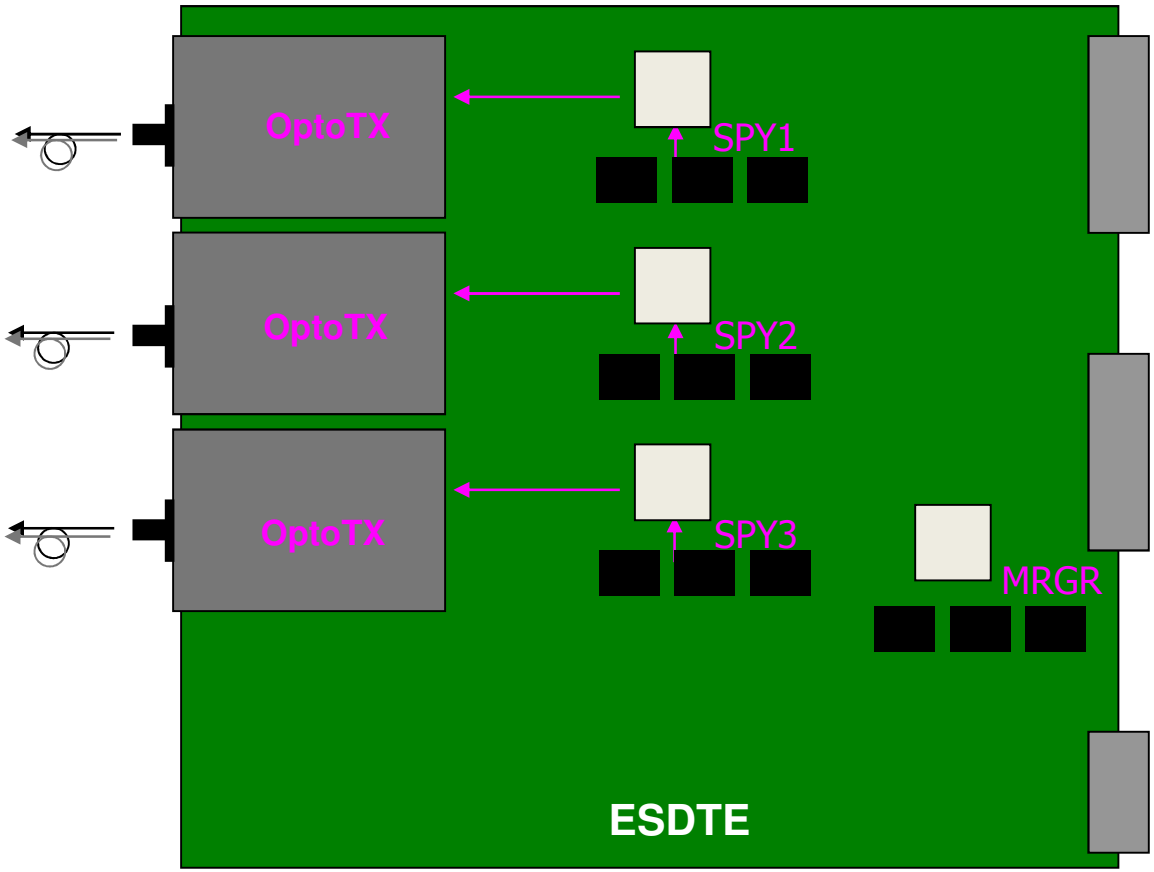
✓ How? Reusing existing components

- OptoTx (developed for the OptoRx commissioning)
- VME host board.

From the ESDCC, by "inverting" its operation …

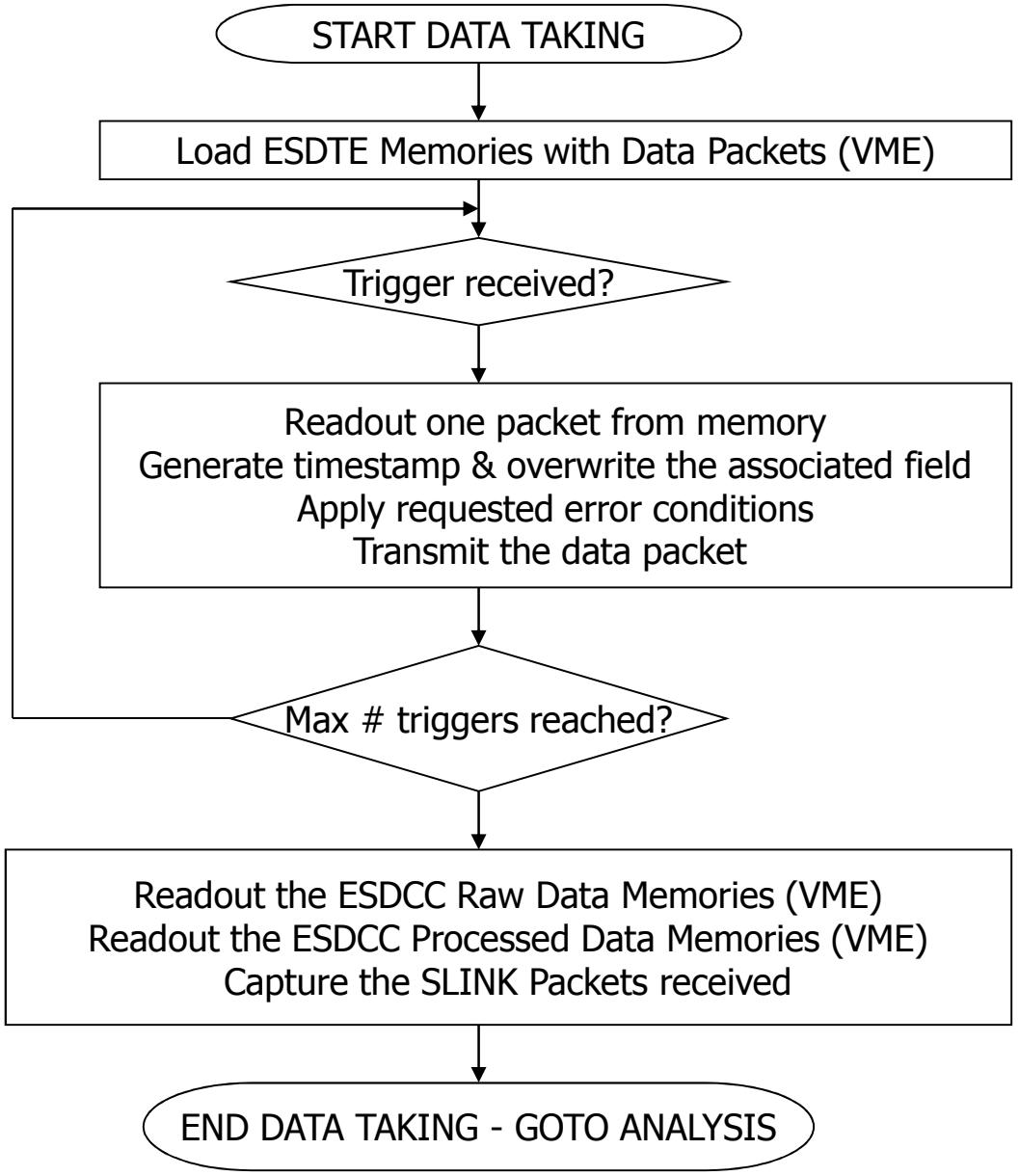


… we get the ESDTE!



# data taking procedure



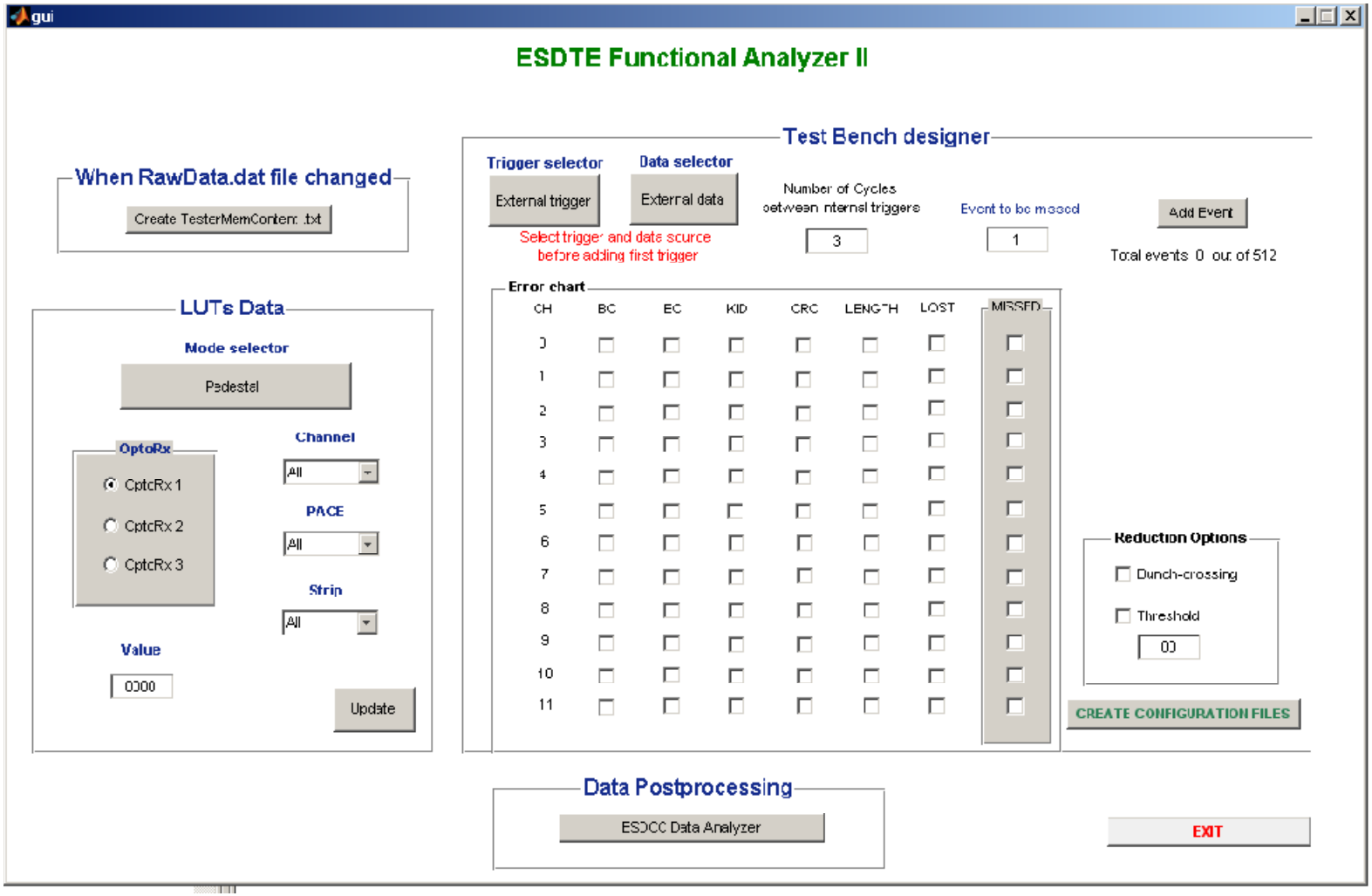



Note1:
Variable trigger rate
(based on trigger source)

Note2:
Max Pattern Length=512 ev.
(due to memory size)

- ✓ Check the integrity of the ESDCC raw data packets
- ✓ Check the integrity of the ESDCC processed data packets
- ✓ Compare the ESDTE & ESDCC raw data packets
- ✓ Calculate the expected processed data
- ✓ Compare the expected with the received processed data (VME)
- ✓ Compare the expected with the received processed data (SLINK)
- ✓ Report all errors

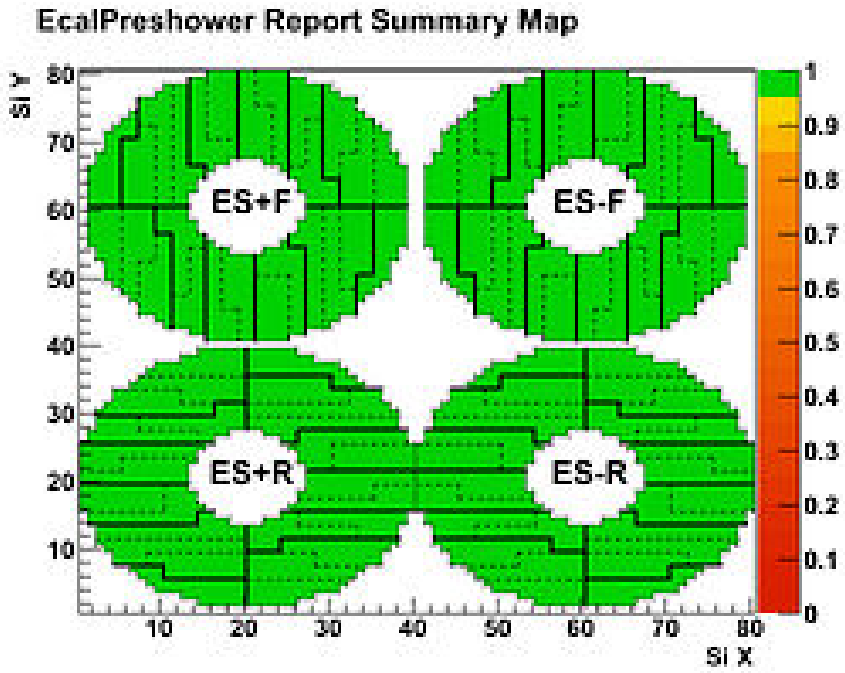
Note:
The data taking & analysis are repeated several times with different ESDCC settings (The ESDCC is a configurable object)

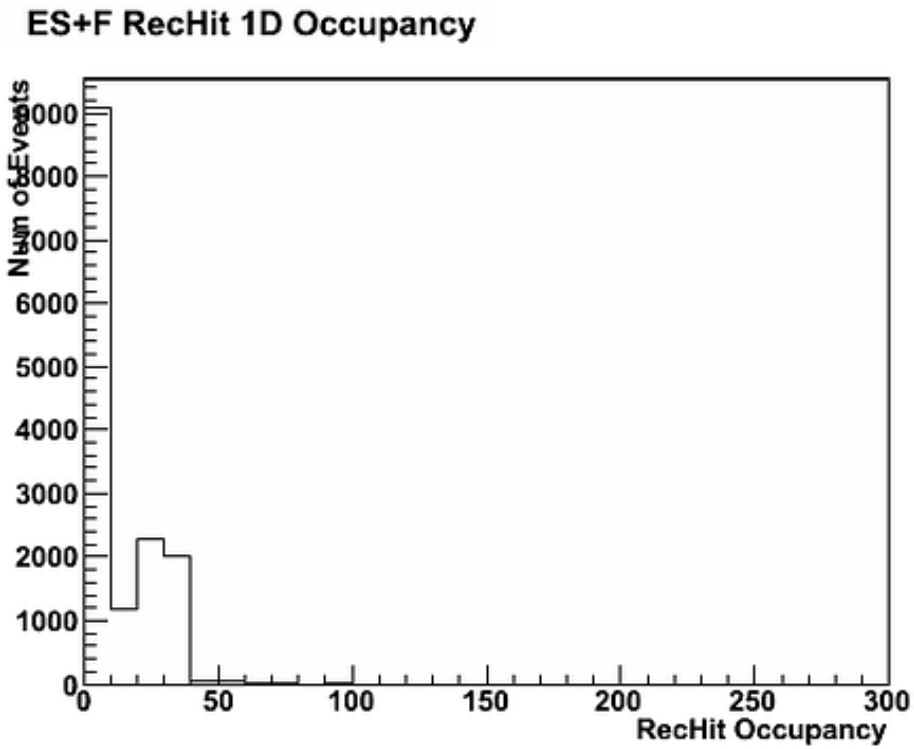



✓ Test Duration: 60min

✓ Results: functionality seems fine (some bugs found & corrected).
all error conditions handled correctly

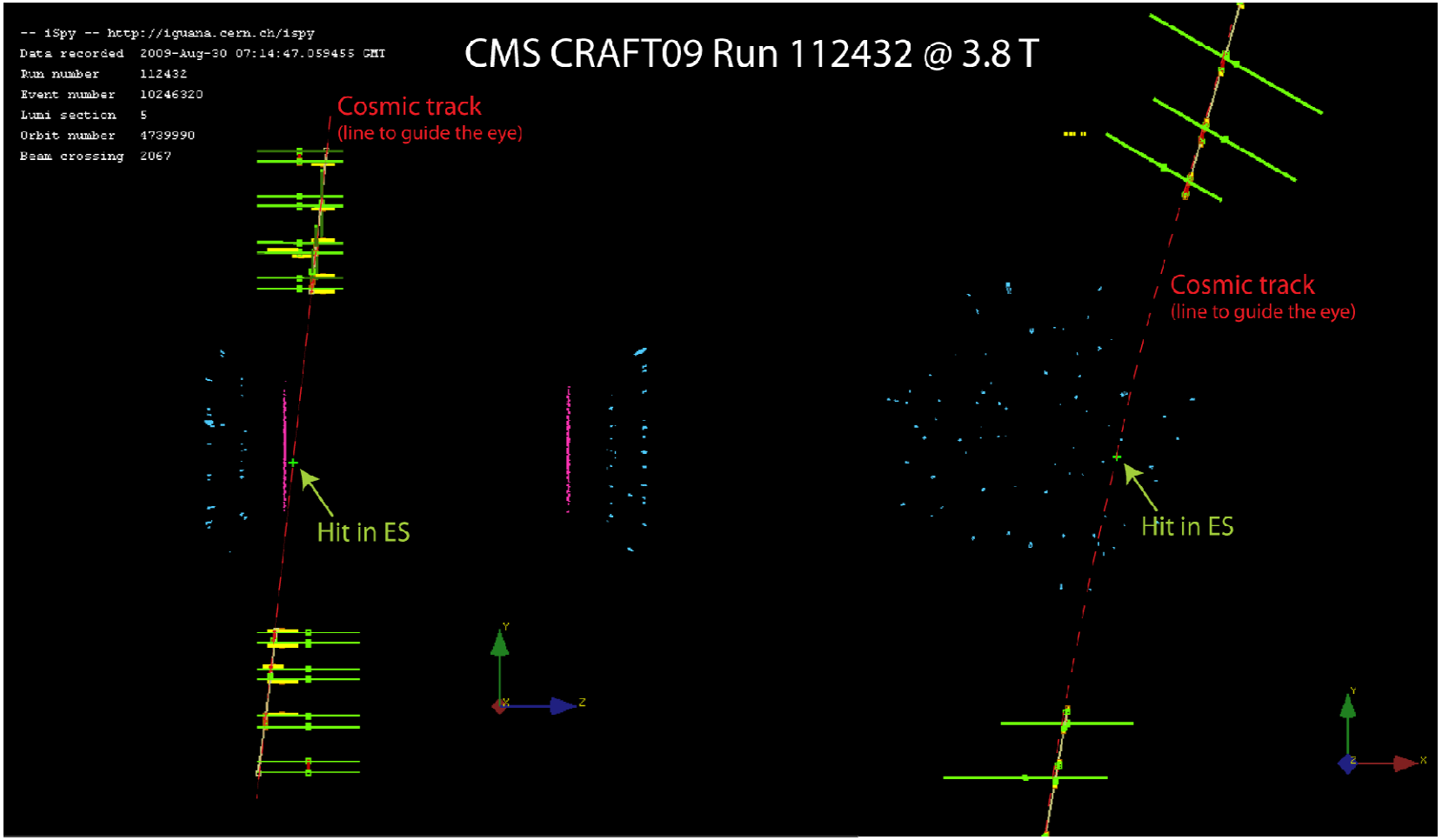
- CMS-ES is installed.
- CRAFT09 was mostly with ES+F (1/4 of ES) only while ES-F running privately for ESDCC firmware development.
- Installed 20 ESDCCs on the week of Aug. 17th to complete ES off-detector electronics.
- Since Aug. 28, all 40 ESDCCs are operational at CMS.



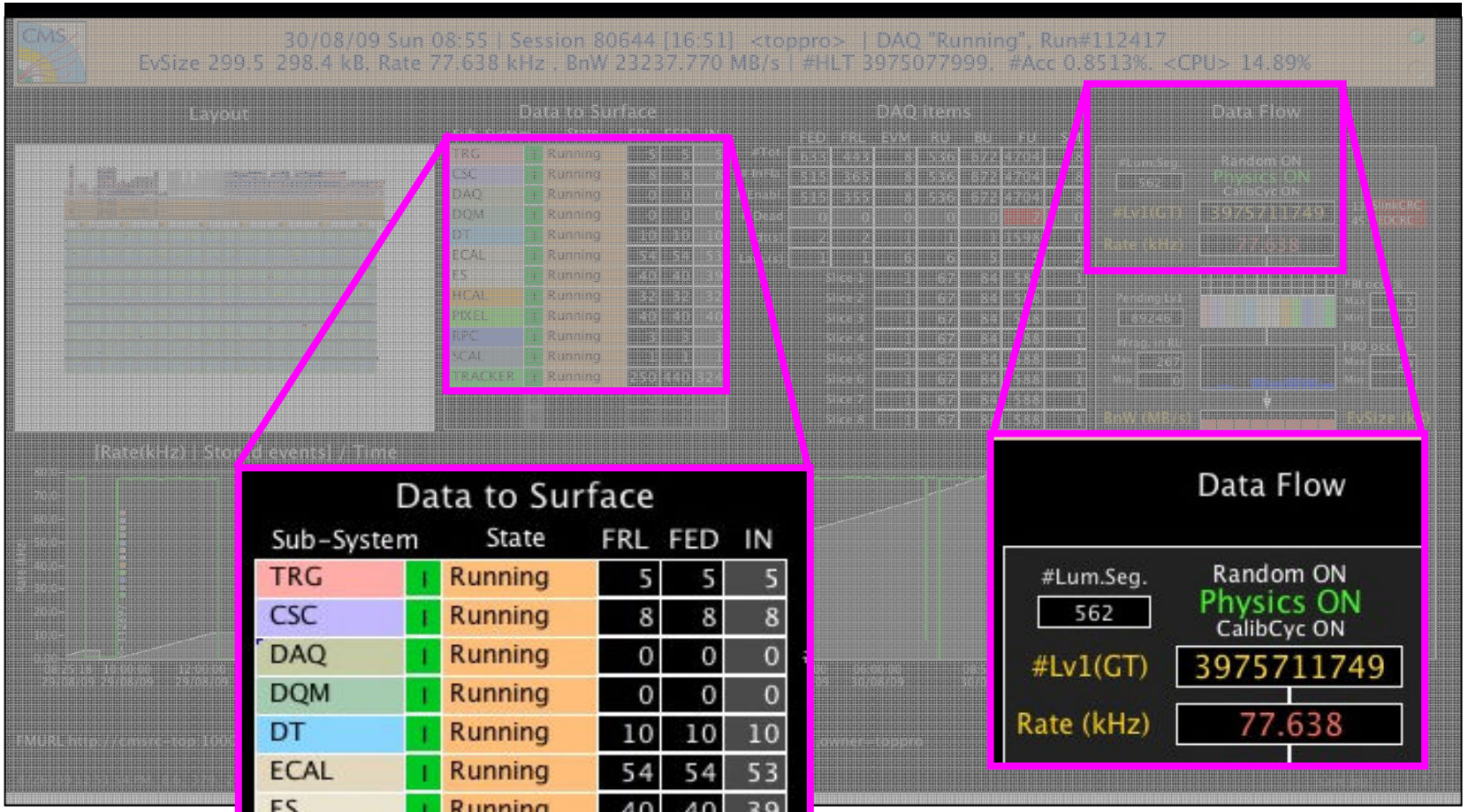


# ESDCC at CMS – Cosmic Ray Detection





Trigger rate: ~1kHz cosmics + 100Hz Calibration + ~80kHz random




Note: The payload size is compatible with low $L$ (only cosmics & noise are producing signals)

A. Produce "high $L$"-like payloads during Global Run at high-rates.

Method: by setting some pedestals to zero.
Note: similar tests have been done but not during Global Run

B. Perform Raw Data Spying during Global Run at high rates.

Target
study the behaviour of the detector (CM noise),
verify the Zero Suppression algorithm operation.

# SUMMARY



✓ HW commissioning systems for the main components of ESDCC developed.

- ❖ Custom connectivity tests applied
- ❖ Allowed testing of the HW at the firm's site & at CERN.
- ❖ Fast, Reliable & Efficient.
- ❖ Revealed production problems - lead to improvement of final production process

✓ HW+FW commissioning system reusing existing components developed.

- ❖ ESDCC commissioning in the lab
- ❖ ESDCC functionality has been validated
- ❖ Revealed reliability issues on few cards & firmware bugs
- ❖ Minimized the integration time at CMS
  (reception → operation of last 20 cards took around two weeks)

✓ All necessary Preshower readout hardware installed at CMS

✓ Still to replace old production VME host boards with new ones

✓ HW+FW+SW performance of the ESDCC with "low $\mathcal{L}$"-like data payloads is satisfactory (cosmics seen, high trigger rate of ~80KHz without problems)

✓ Still to emulate the ESDCC operation with "high $\mathcal{L}$"-like data payloads