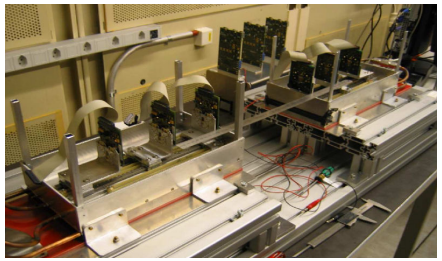
Monolithic Active Pixel Sensors (MAPS): A Long Term R&D

- **Main objective: ILC, with staggered performances**
  - *MAPS applied to other experiments with intermediate requirements*

EUDET 2007/2009

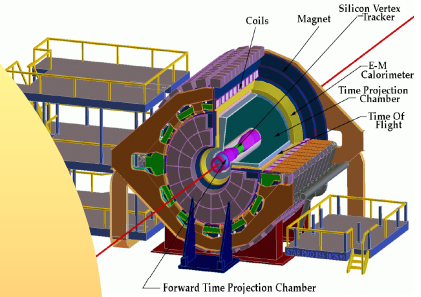
Beam Telescope



- **FP6 EUDET Project (DESY-Hamburg, Germany)**
  - **Surface** — **6 x 2 cm²**
  - **Read-out speed** — **A. 20 MHz → D. at 100 MHz**
  - **Temp. & Power:** — **No constraints**

STAR 2010

Solenoidal Tracker at RHIC

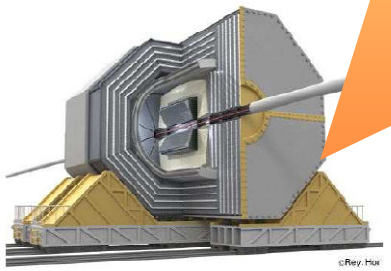


- **STAR Experiment (RHIC – Brookhaven, USA)**
  - **Surface** — **~1600 cm²**
  - **Read-out speed** — **A. 50 MHz → D. up to 250 MHz**
  - **Temp. & Power** — **30°C, ~100mW/cm²**

- **CBM Experiment (GSI – Darmstadt, Germany)**
  - **Surface** — **~500 cm²**
  - **Read-out speed** — **D. 15 x 10^9 pixels/sensor/s**
  - **Rad Tol** — **1 MRad, > 10^{13} N_{eq}/cm²**

ILC >2012

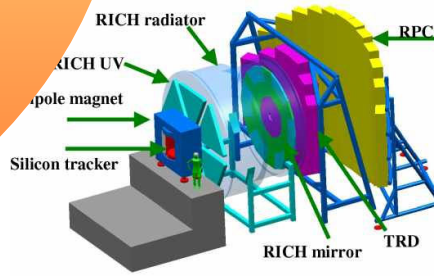
Internatinal Linear Collider



- **ILC Experiment**
  - **5-6 layers of detection** — **~3000 cm²**
  - **Read-out speed** — **D. 15 x 10^9 pixels/sensor/s**
  - **Temp. & Power** — **30°C, ~100 mW/cm²**
  - **Rad Tol** — **~300 kRad, ~10^{12} N_{eq}/cm²**

CBM 2012

Compressed Baryonic Matter



➔ *Spinoff: Interdisciplinary Applications, biomedical, …*

- *Partnerships: GIS IN2P3/Photonis & GIS IN2P3/SAGEM & Ohio University & Michigan University…*

10 k Frames per Second Readout MAPS for the EUDET Beam Telescope

Christine Hu-Guo (IPHC)

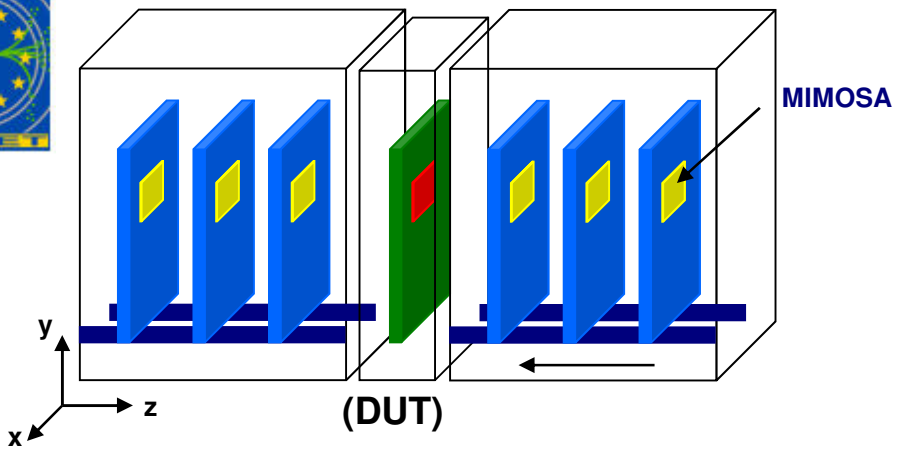
on behalf of IPHC (Strasbourg) & IRFU (Saclay) collaboration

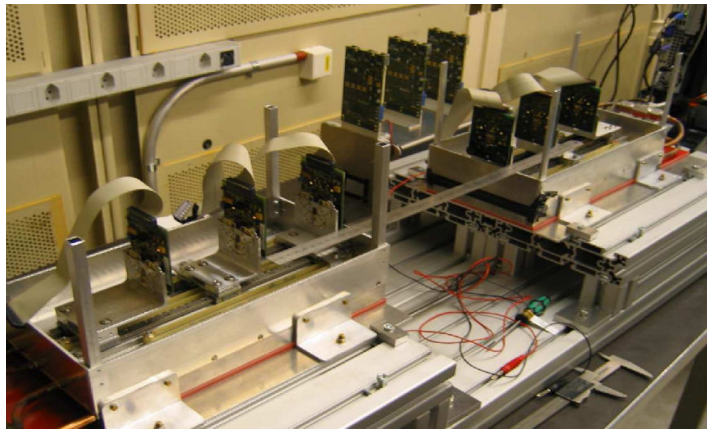
Outline

- *EUDET – JRA1 Pixellised Beam Telescope Design & Specifications*
- *MAPS (Monolithic Active Pixel Sensors) Development*
- *MIMOSA26 Sensor Design*
- *Preliminary Test Results*
- *Summary & Perspectives*

EUDET: Detector R&D towards the International Linear Collider

- *EUDET supported by the European Union in the 6th Framework Programme*
  - *Provide to the scientific community an infrastructure aiming to support the detector R&D for the ILC*
  - *JRA1 (Joint Research Activity): High resolution pixellised beam telescope*
    - *Two arms each equipped with three layers of pixel sensors (MIMOSA)*
    - *DUT is located between these arms and moveable via X-Y table*





Demonstrator telescope using MIMOSA with analogue read-out (2007)

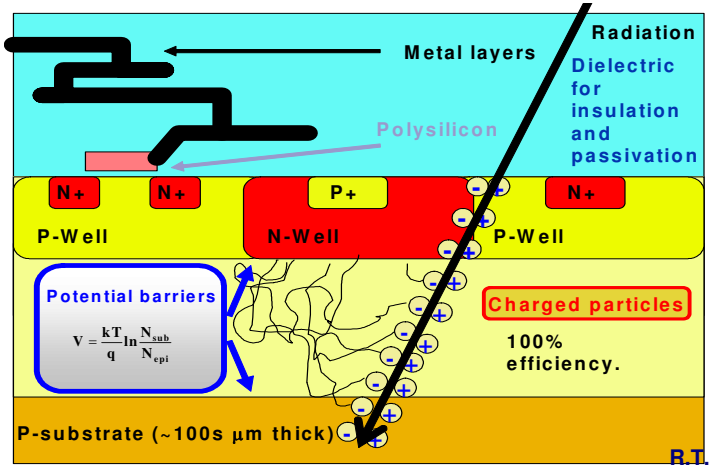
  - *Final telescope:*
    - *High extrapolated resolution ~< 2 µm*
    - *Large sensor area ~ 2 cm², in one dimension it has to be larger than 20 mm*
    - *High binary read-out speed ~ 10 k frame/s*
    - *Hit density: up to 10^6 hits/s/cm², Running at DESY, (CERN SPS)*

➔ *Research motivation to develop a new generation MAPS*

Development of MAPS for Charged Particle Tracking

- ***In 1999, the IPHC CMOS sensor group proposed the first CMOS pixel sensor (MAPS) for future vertex detectors (ILC)***
  - *Numerous other applications of MAPS have emerged since then*
  - *~10-15 HEP groups in the USA & Europe are presently active in MAPS R&D*

- ***Original aspect: integration sensitive volume (EPI layer) and front-end readout electronics on the same substrate***
  - *Charge created in EPI, excess carries propagate thermally, collected by N_{WELL}/P_{EPI}, with help of reflection on boundaries with P-well and substrate (high doping)*
    - *Q = 80 e^-h / µm ➔ signal < 1000 e^-*
  - *Compact, flexible*
  - *EPI layer ~10–15 µm thick*
    - *thinning to ~30–40 µm permitted*
  - *Standard CMOS fabrication technology*
    - *Cheap, fast multi-project run turn-around*
  - *Room temperature operation*

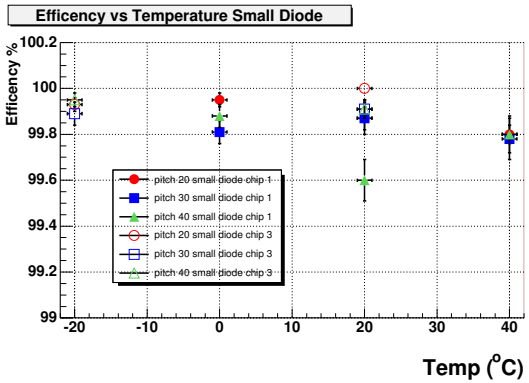


- ***➔ Attractive balance between granularity, material budget, radiation tolerance, read out speed and power dissipation***

  BUT
  - *Very thin sensitive volume → impacts signal magnitude (mV!)*
  - *Sensitive volume almost un-depleted → impacts radiation tolerance & speed*
  - *Commercial fabrication (parameters) → impacts sensing performances & radiation tolerance*
  - *N_{WELL} used for charge collection → restricts use of PMOS transistors*

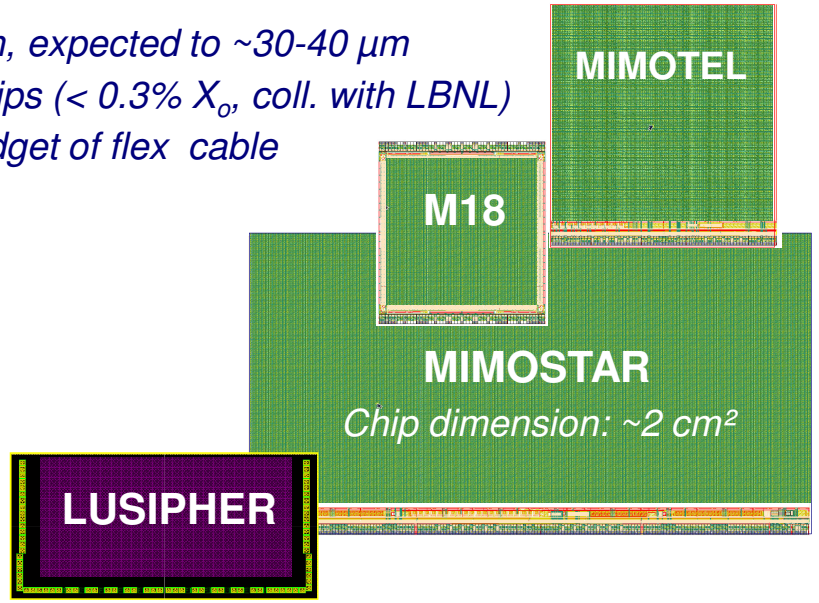
Achieved Performances with Analogue Readout

- ***MAPS provide excellent tracking performances***
  - *Detection efficiency ~100%*
    - *ENC ~10-15 e^- , S/N > 20-30 (MPV) at room temperature*
  - *Single point resolution ~ µm, a function of pixel pitch*
    - *~ 1 µm (10 µm pitch), ~ 3 µm (40 µm pitch) ➔ analogue output!*
  - *Radiation tolerance:*
    - *Ionising radiation tolerance: O(1 M Rad)*
    - *Non ionising radiation tolerance: 2x10^{12} N_{eq}/cm^2 (20 µm pitch) → 10^{13} N_{eq}/cm^2 (10 µm pitch)*
  - *System integration*
    - *Thinning (via STAR collaboration at LBNL) ~50 µm, expected to ~30-40 µm*
    - *Development of ladder equipped with MIMOSA chips (< 0.3% X_o, coll. with LBNL)*
    - *Edgeless dicing / stitching → alleviate material budget of flex cable*



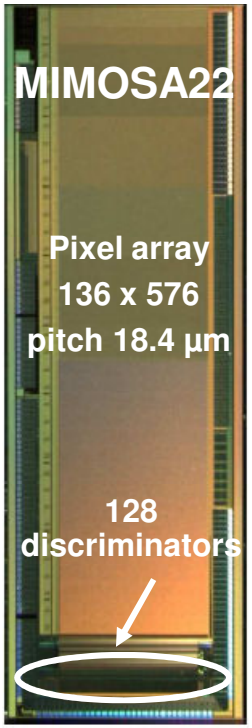
MAPS: Final chips:

- *MIMOTEL (2006): ~66 mm², 65k pixels, 30 µm pitch*
  EUDET Beam Telescope (BT) demonstrator
- *MIMOSA18 (2006): ~37 mm², 262k pixels, 10 µm pitch*
  High resolution EUDET BT demonstrator
- *MIMOSTAR (2006): ~2 cm², 204k pixels, 30 µm pitch*
  Test sensor for STAR Vx detector upgrade
- *LUSIPHER (2007): ~40 mm², 320k pixels, 10 µm pitch*
  Electron-Bombarded CMOS for photon and radiation imaging detectors



❑ **BUT: moderate readout speed for larger sensors with smaller pixel pitch!**

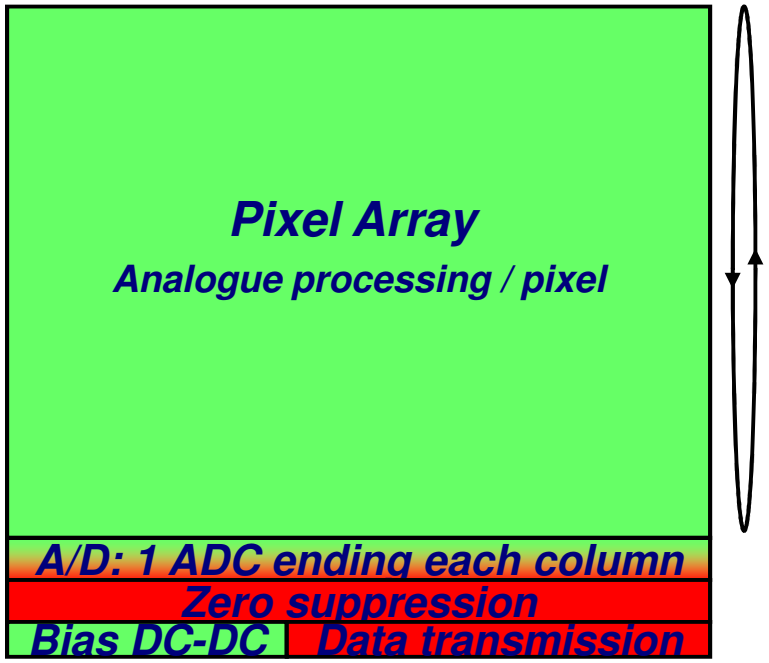
MAPS performance Improvement

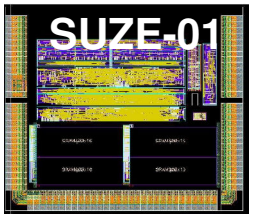


➔ *R&D on high readout speed, low noise, low power dissipation, highly integrated signal processing architecture with radiation tolerance*

❶ ***Architecture of pixel array organised in // columns read out:***

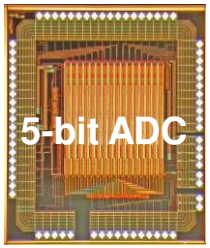
- *Pre-amp and CDS in each pixel*
- *A/D: 1 discriminator / column (offset compensation)*
- *Power vs Speed*
  - *Power ➔ Readout in a rolling shutter mode*
  - *Speed ➔ All pixels belonging to the same row are read out simultaneously*
- *MIMOSA8 (2004), MIMOSA16 (2006),* ***MIMOSA22 (2007/08)***





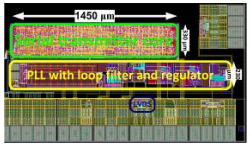
❷ ***Zero suppression logic:***

- *Reduce the raw data flow of MAPS*
- *Data compression factor ranging from 10 to 1000, depending on the hit density per frame*
- ***SUZE-01 (2007), see poster A. HIMMI***



❹ ***4–5 bits ADCs (~10³ ADC per sensor)***

- *LPCC, LPSC, IRFU, IPHC collaboration*
- *Potentially replacing column-level discri.*
- *5 bits: σ_{sp} ~1.7–1.6 µm*
  4 bits: σ_{sp} < 2 µm for 20 µm pitch
- *Next step: integrate ADCs with pixel array*



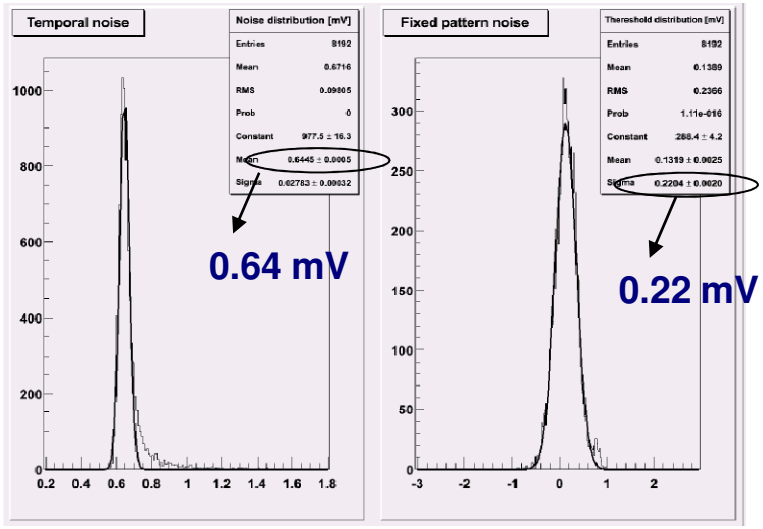
❸ ***Serial link transmission with clock recovery***

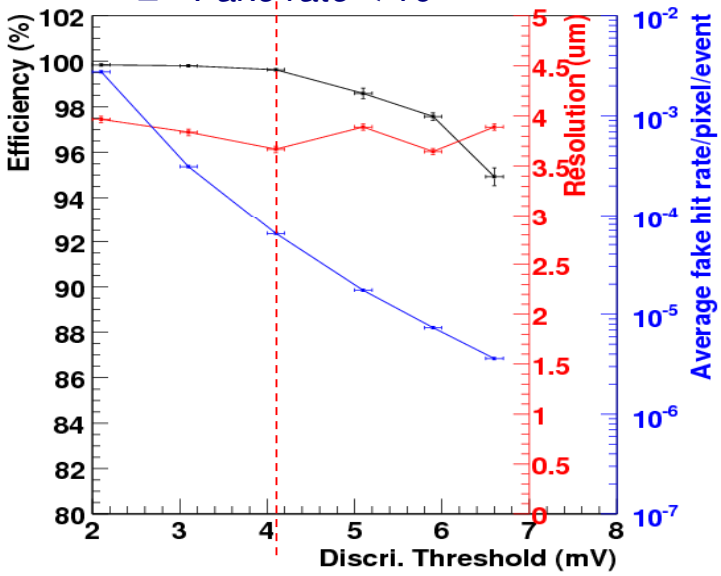
- *Prototype (2008-2009)*
- ***See poster I. VALIN***

❺ ***Voltage regulator & DC-DC converter***

MIMOSA22 & SUZE-01 Test Results

- ***MIMOSA22:*** ***(15 µm EPI) 136 x 576 pixels + 128 column-level discriminators***
  - **Laboratory test:**
    - *Temporal Noise: 0.64 mV ➔ 12 e⁻*
    - *FPN: 0.22 mV ➔ 4 e⁻*
  - **Beam test at CERN SPS (120 GeV pions)**
    - *Threshold ~ 4 mV ➔ 6 x σ noise*
      - *Detection Efficiency > 99.5%*
      - *Single point resolution < 4 µm*
      - *Fake rate < 10^{-4}*





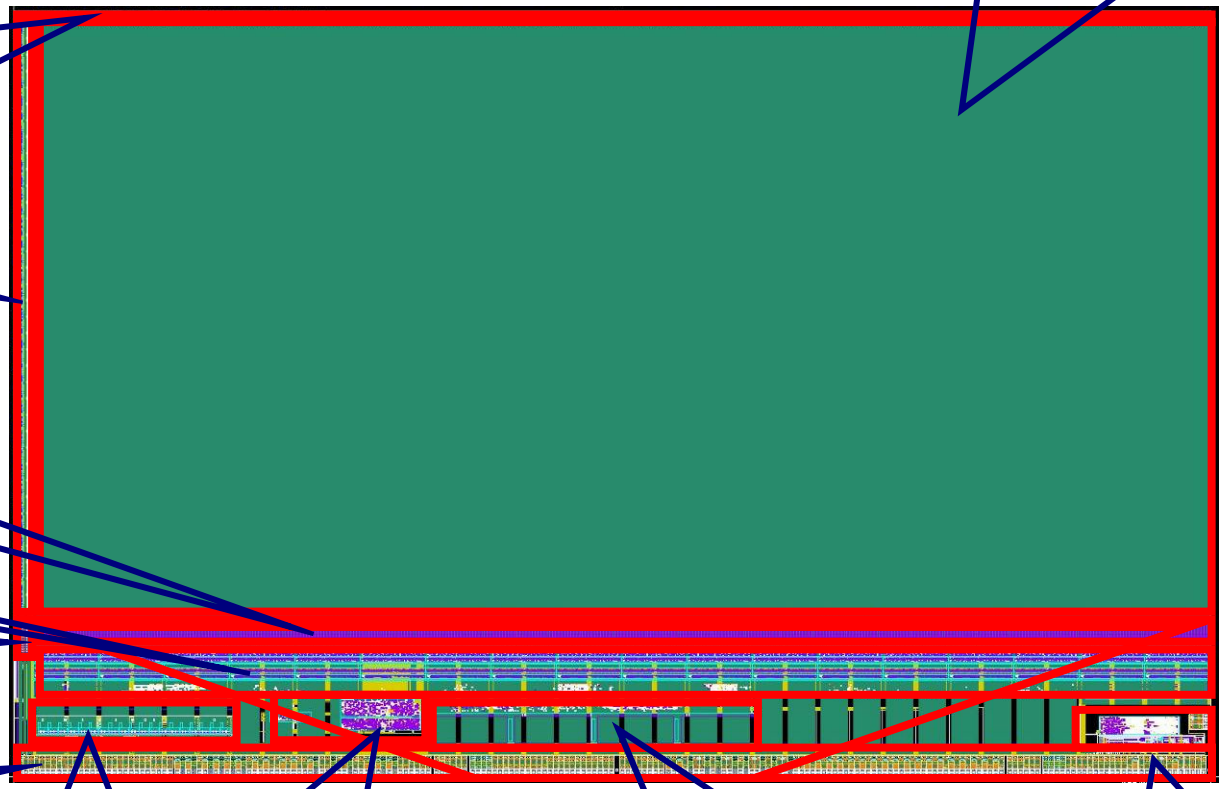
- ***SUZE-01:***
  - **Lab. test :**
  - *Design performances tested at the nominal frequency with safety margin of 20%, at* room *Temp*
    - *No pattern encoding error, can handle > 100 hits/frame at rate ~200 ns per pixel row*
  - **Still to do :** *improve radiation tolerance (SEU, SEL) of digital circuits (including memories)*

MIMOSA26: 1st MAPS with Integrated ∅

CMOS 0.35 µm OPTO technology
Chip size : 13.7 x 21.5 mm²

- Pixel array: 576 x 1152, pitch: 18.4 µm
- Active area: ~10.6 x 21.2 mm²
- In each pixel:
  - Amplification
  - CDS (Correlated Double Sampling)

- Testability: several test points implemented all along readout path
  - Pixels out (analogue)
  - Discriminators
  - Zero suppression
  - Data transmission



- Row sequencer
- Width: ~350 µm

- 1152 column-level discriminators
  - offset compensated high gain preamplifier followed by latch

- Zero suppression logic

- Reference Voltages Buffering for 1152 discriminators

- I/O Pads
  Power supply Pads
  Circuit control Pads
  LVDS Tx & Rx

- Current Ref.
- Bias DACs

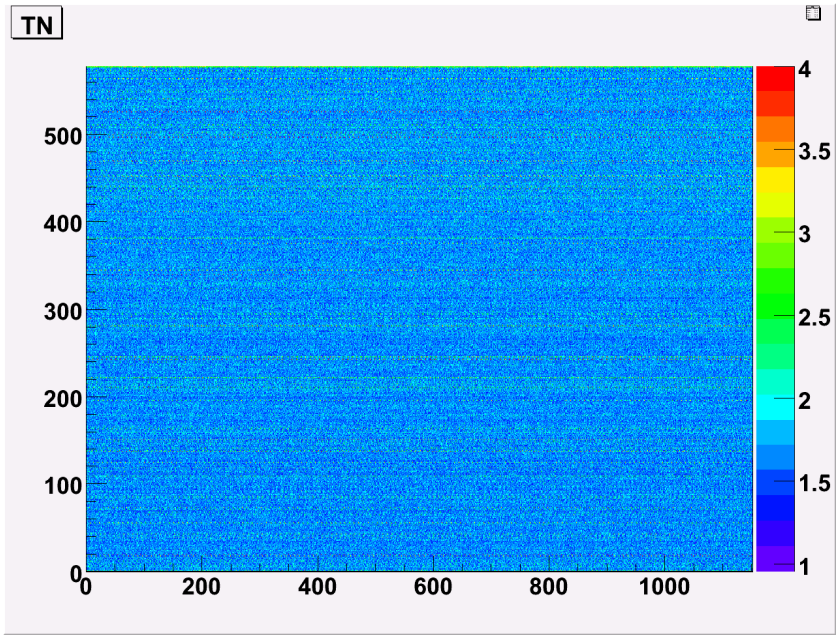
- Readout controller
- JTAG controller

- Memory management
- Memory IP blocks

- PLL, 8b/10b optional

MIMOSA26: Pixels Analogue Output Test Results

- ***Analogue response studied for 8 different sensors :***



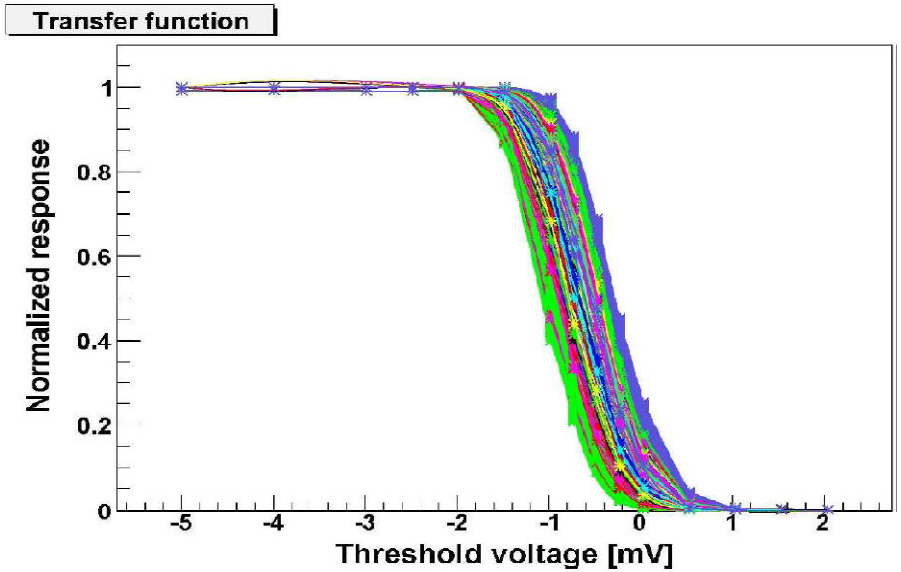
- ***Charge Collection Efficiency (CCE) with ^{55}Fe source : comparison with MIMOSA22***

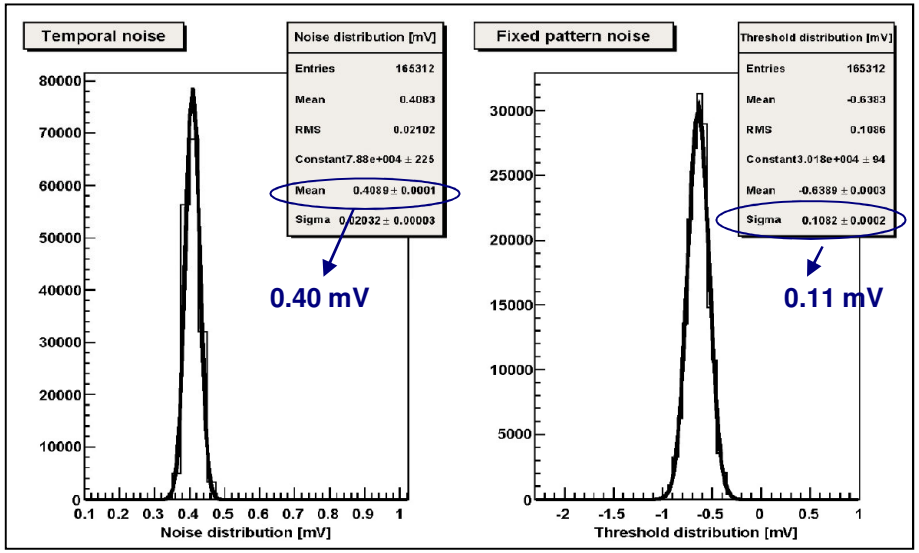
Cluster Size	seed	2x2	3x3	5x5
MIMOSA26	22 %	55 %	73 %	83 %
MIMOSA22	22 %	58 %	75 %	86 %

- *All pixels are alive (none is dead !)*
- *Noise is uniform across the ~2 cm² sensitive area*
- *Satisfactory operation from 80 MHz (nominal) down to 20 MHz (and below)*
- *Noise and CCE performances are ~ identical to those of MIMOSA-22*
- *All 8 sensors exhibit similar behaviours*

Discriminators Output Test Results

- ***Digital output studied on 21 (15 + 6) different sensors :***
  - *Noise performance assessed separately for each of the 4 groups of 288 columns (nominal r.o. speed)*
  - ***All discriminators are operational at nominal speed*** *(and below)*

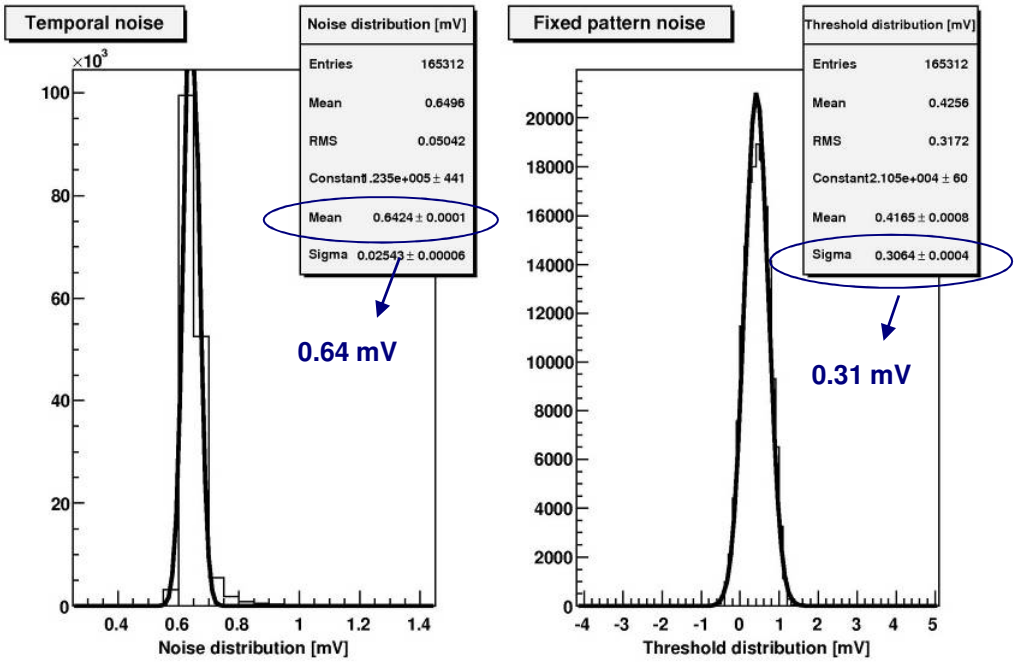




  - *Typical value of discriminator thermal noise ~ 0.3-0.4 mV*
  - *Discriminator FPN ~ 0.15 mV ➔ < 3 e^- ENC*
  - *Results are ~ identical to MIMOSA-22 values*

Pixel Array ⊕ Discriminated Output Test Results

- ***Studied on 15 (80 MHz) + 6 (20 MHz) different sensors :***
  - *example of sub-array A of chip-6 :*



  - *Typical value of total temporal noise ~ 0.6 - 0.7 mV*
  - *Typical value of total FPN noise ~ 0.3 - 0.4 mV*
  - *Results are ~ identical to MIMOSA22 values (N <~12 - 13 e^- ENC)*
  - *80 ➔ 20 MHz: pixel noise ↗ discri. Noise ↘ ⇛ mild overall change*

➔ ***Array of 660,000 pixels coupled to 1152 discriminators works ~ as expected***

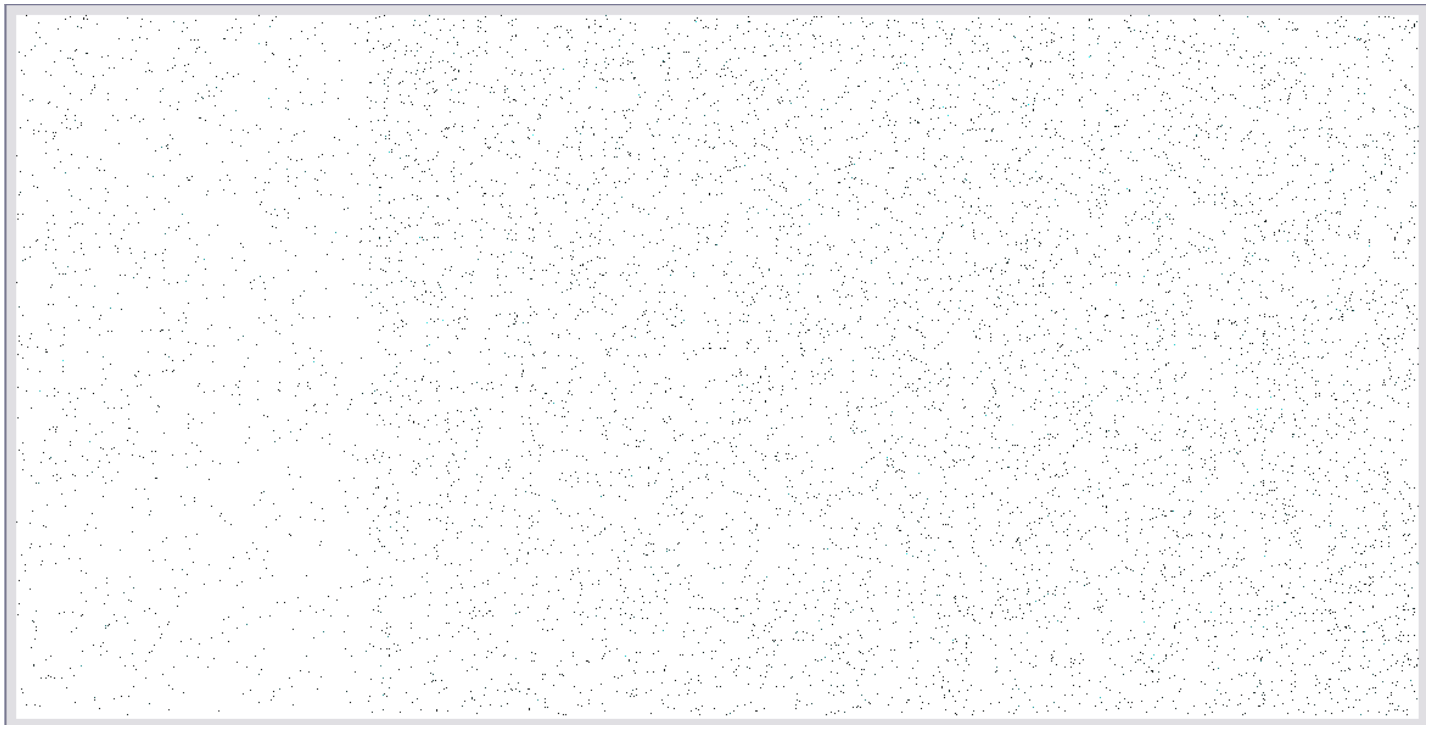
Zero-Suppression & Output Memories Test Results

- ***Functionality tests:***
  - *Encoding addresses (line, column) of the hit function (systematic and randomly),*
  - *Encoding of the states (0 to 9 STATES) in all column positions of the 18 banks (systematic and randomly),*
  - *Encoding of the shape of the state: 1 to 4 consecutive pixels (systematic and randomly),*
  - *Checking of the continuity between blocks,*
  - *Encoding patterns with more than 9 states detected (overflow)*
  - *Working Frequency range: 10 MHz to 115 MHz.*
  - *Output modes: 2 outputs 80 MHz, 1 Output 80 MHz, 2 outputs 40 MHz.*
- ***3 critical patterns tested 7 millions times without errors***
- ***Robustness test: 199 frames x 10 000 random patterns test at 80 MHz without errors.***

➔ ***Zero-suppression + output memories behave as expected***

Full Chain (Pixels + ADC + Ø + Data Transmission) Test Results

- ***Full chain signal delivery studied on several different sensors :***
  - *Ex: without illumination chip-24 output for 5 N threshold (**1000 frames**), 80 MHz, 20 °C*



  - *"Fake hit rate" due to pixel noise fluctuations at 80 MHz*

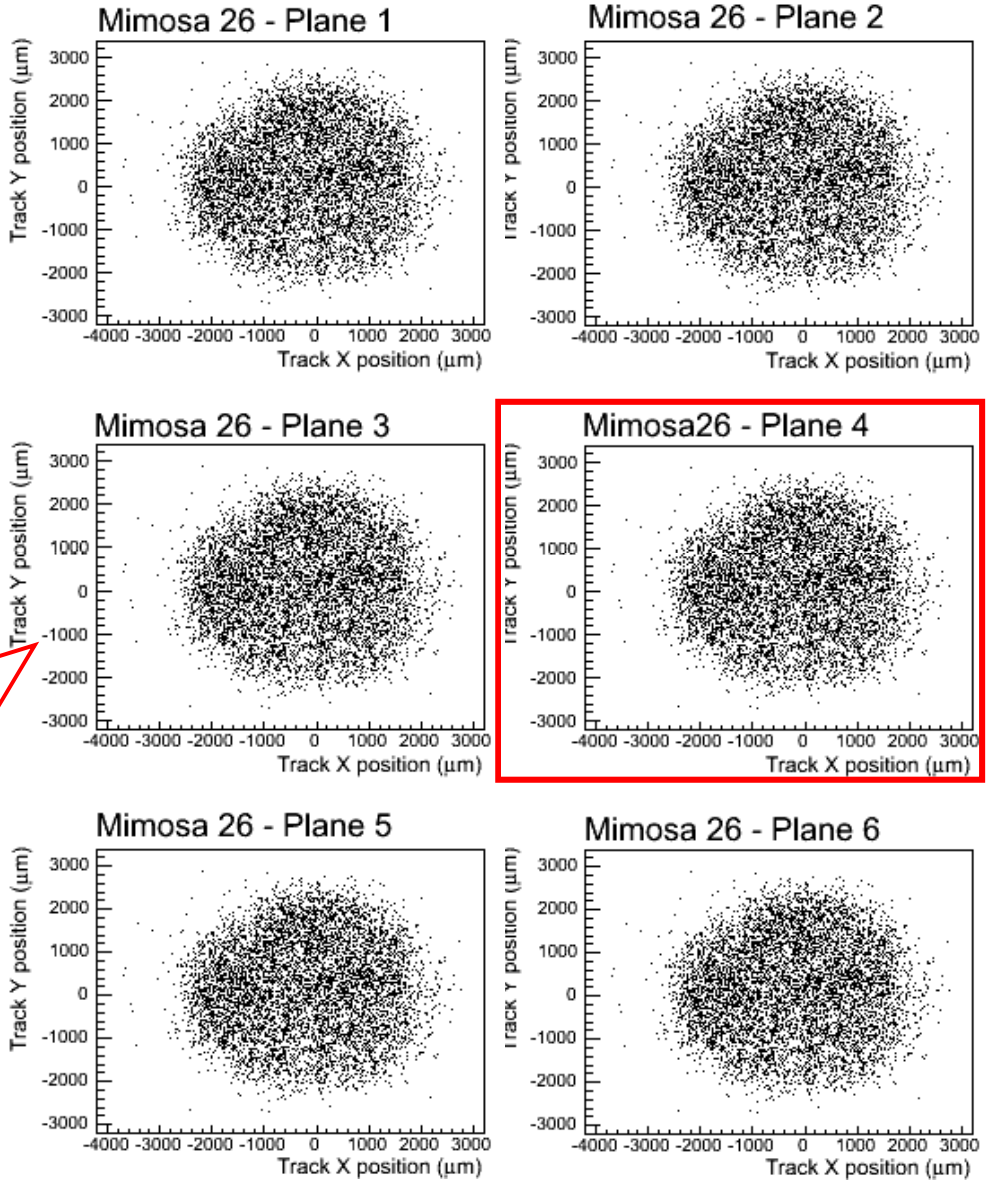
Discriminator Threshold	4 N	5 N	6 N	8 N	10 N	12 N
(N_{pix}> Threshold) / N_{Pix_total} (10^{-4})	< 4	~1.1	~0.45	0.07	0.014	0.003

  - *Varying the operation T from +20 °C to +40 °C ➔ essentially no change*

MIMOSA26: Beam Test at CERN SPS 120 GeV (pions)

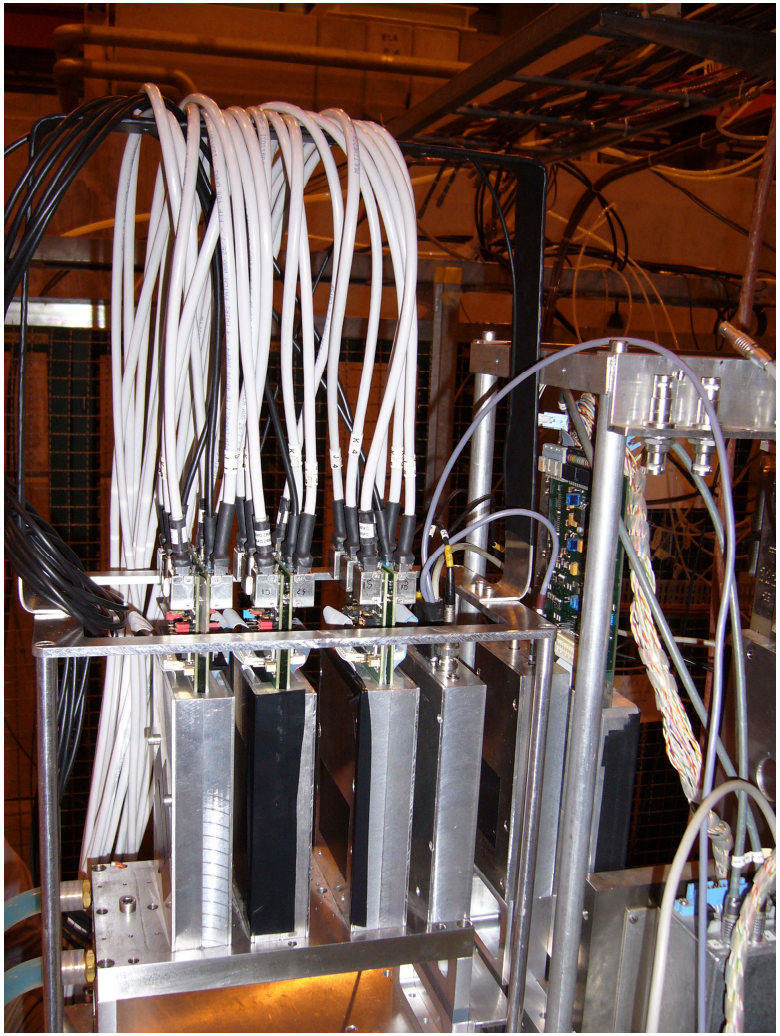
- ***Telescope made of 6 MIMOSA26 chips running at nominal speed***
  - *It tracks particles in beam with high efficiency (about 80% of the triggers lead to a good track quality).*
  - ➔ *This performance demonstrates that Mimosa26 sensor is appropriate for a beam telescope.*
  - *The detailed characterization is ongoing.*

- ✓ *Beam profile for 80 000 correlated tracks on the 5 reference planes*
- ✓ *Threshold at 8N*
- ✓ *Triggered by a scintillator of 7 x 7 mm²*

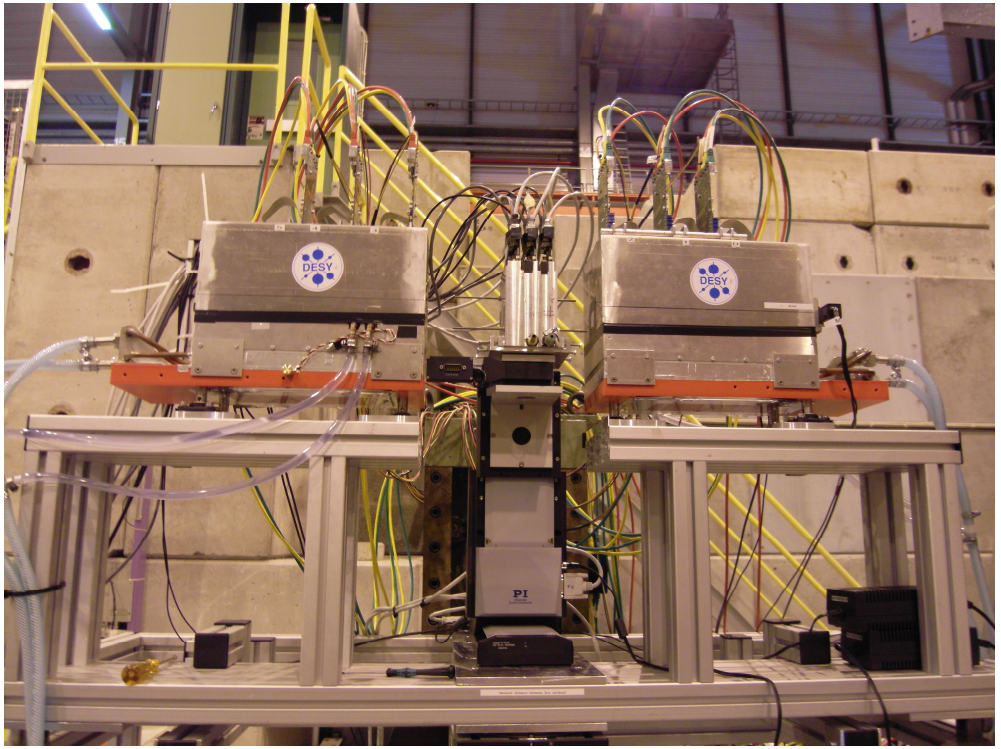


- ***Preliminary test results from the EUDET collaboration:***
  - *3 MIMOSA26 chips mounted as DUT in the EUDET BT demonstrator in July*
  - *BT tracks reconstructed in the 3 planes*
  - ➔ *Residues compatible with σ_{sp} ~ 3.5-4 µm*

MIMOSA26: Beam tests



6 MIMOSA26: 5 reference planes, 1 DUT



6 MIMOSA17 as reference planes,
3 MIMOSA26 (120 µm) as DUT

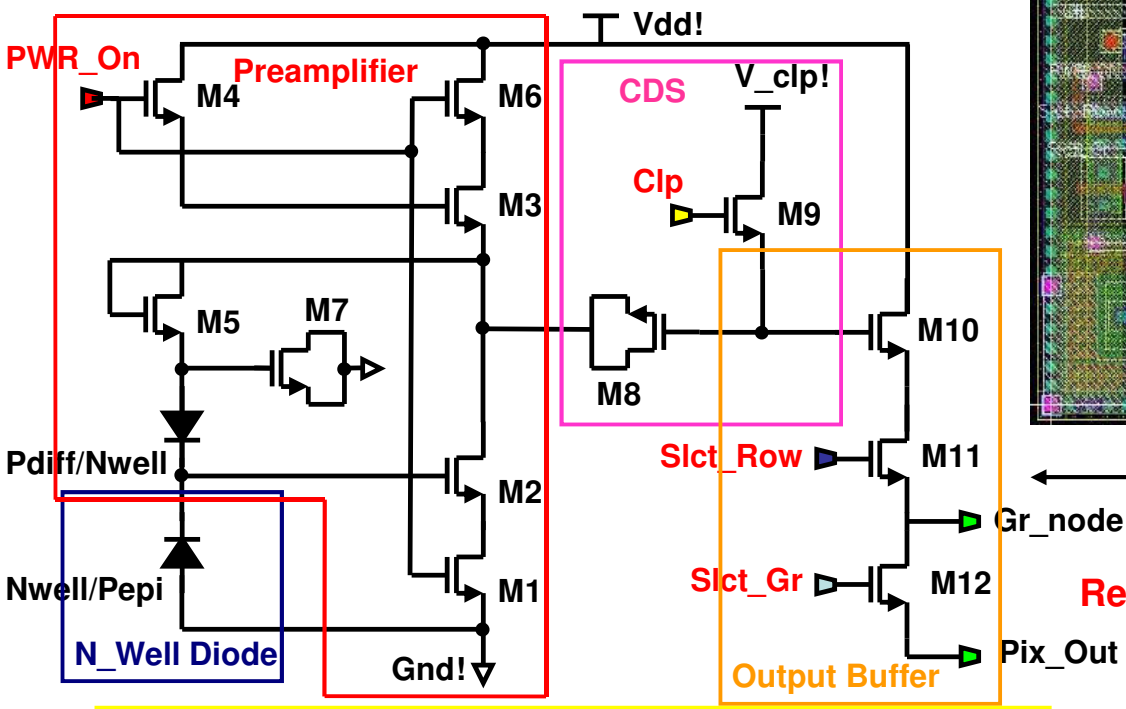
Summary + Perspectives

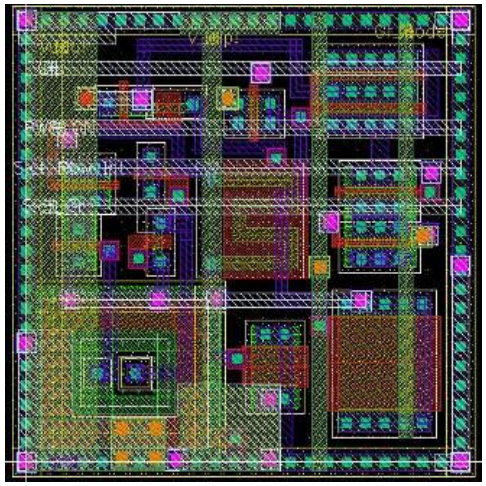
- ***The First reticule size MAPS with binary output and integrated zero suppression logic has been designed and fabricated***
  - *Small pitch pixel (18.4 µm), Large sensitive area (> 2 cm²)*
  - *High binary read-out speed : ~10 K frames/s*
  - ➔ ***2D MAPS have reached necessary prototyping maturity for real scale applications:***
  - *STAR vertex detector upgrade: MIMOSA26x1.7 (may also equip EUDET BT, ~50 µm)*
  - *Architecture will be extended to MVD-CBM (SIS-100) and is proposed for Vx det.-ILC*
- ***The emergence of fabrication processes with depleted epitaxy / substrate opens the door to :***
  - *Substantial improvements in read-out speed and non-ionising radiation tolerance*
    - *Non-ionising radiation tolerance up to 10^{14} N_{eq}/cm^2 is expected*
  - *"Large pitch" applications ➔ trackers (e.g. Super LHC)*
- ***Translation to 3D integration technology :***
  - *Resorb most limitations specific to 2D MAPS*
    - *T type & density, peripheral insensitive zone, combination of different CMOS processes*
  - *Offer an improved read-out speed : O(µs) !*
  - *Many difficulties to overcome (ex. heat, power)*
  - *R&D in progress ➔ 2009/10 important step for validation of this promising technology*

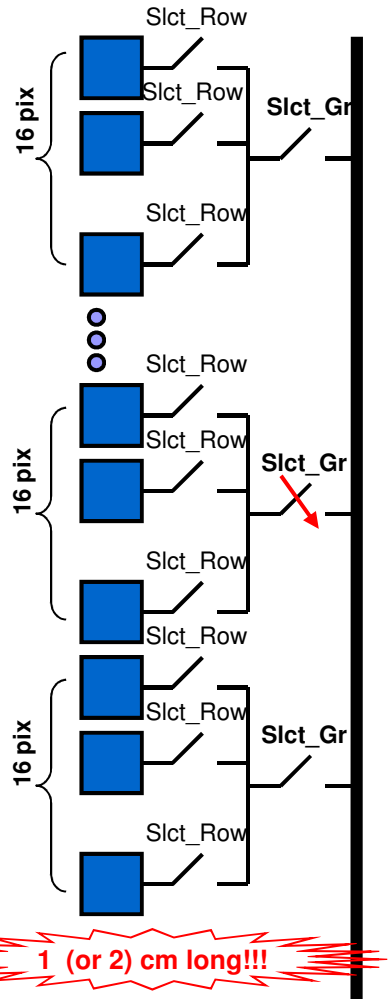
⇨ ***See talk of W. Dulinski on session B3***
⇨ ***See talk of Y. Fu on Poster session***

Readout Chain: Pixel

See Ref. A. Dorokhov et al., TWEPP-07 CERN-2007-007 proceeding pp. 423-427







Readout = 16 CK cycles

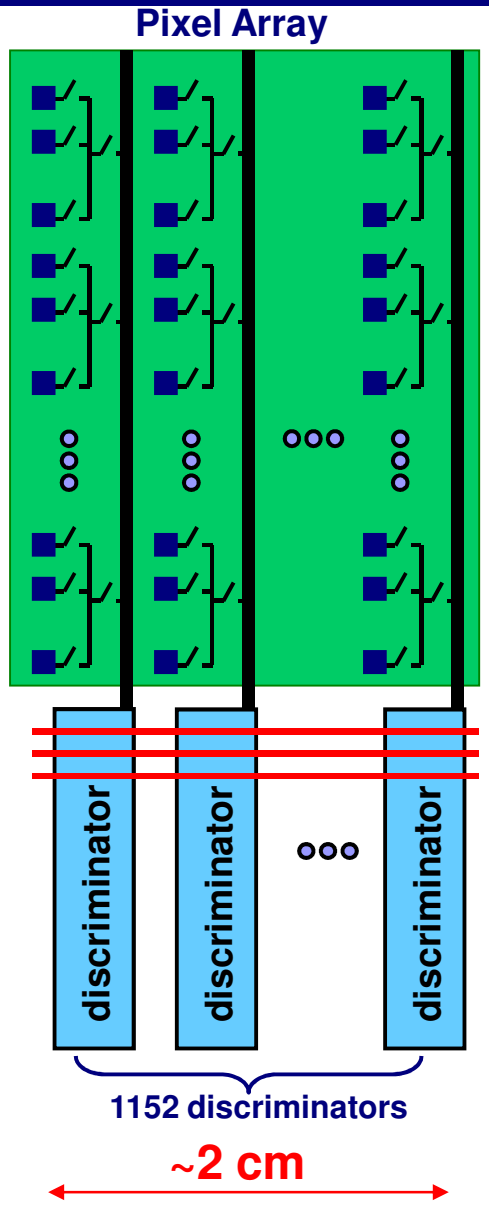
ONLY NMOS transistors can be used, since any additional N-well used to host PMOS transistors would compete for charge collection with the sensing N-well diode

1 (or 2) cm long!!!

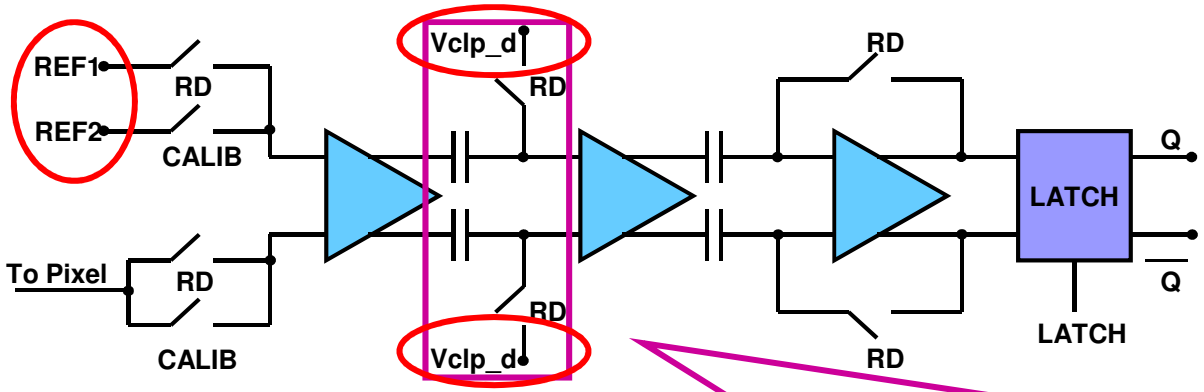
RD
CALIB
LATCH
Column –level discriminator

- *4 digital control signals per row: PWR_On, Slct_Row, Slct_Gr, Clp*
  - *Slct_Row (16CK), PWR_On (2x16CK), Slct_Gr (16x16CK): power activate signals*
  - *Clp: signal for CDS (3CK)*
- *Power consumption: ~200 µW/pixel*

Readout Chain: Pixel + discriminator



See Ref. Y. Degerli et al, IEEE, Trans. Nucl. Sci. vol.52, No. 6, pp. 3186-3193, Dec. 2005



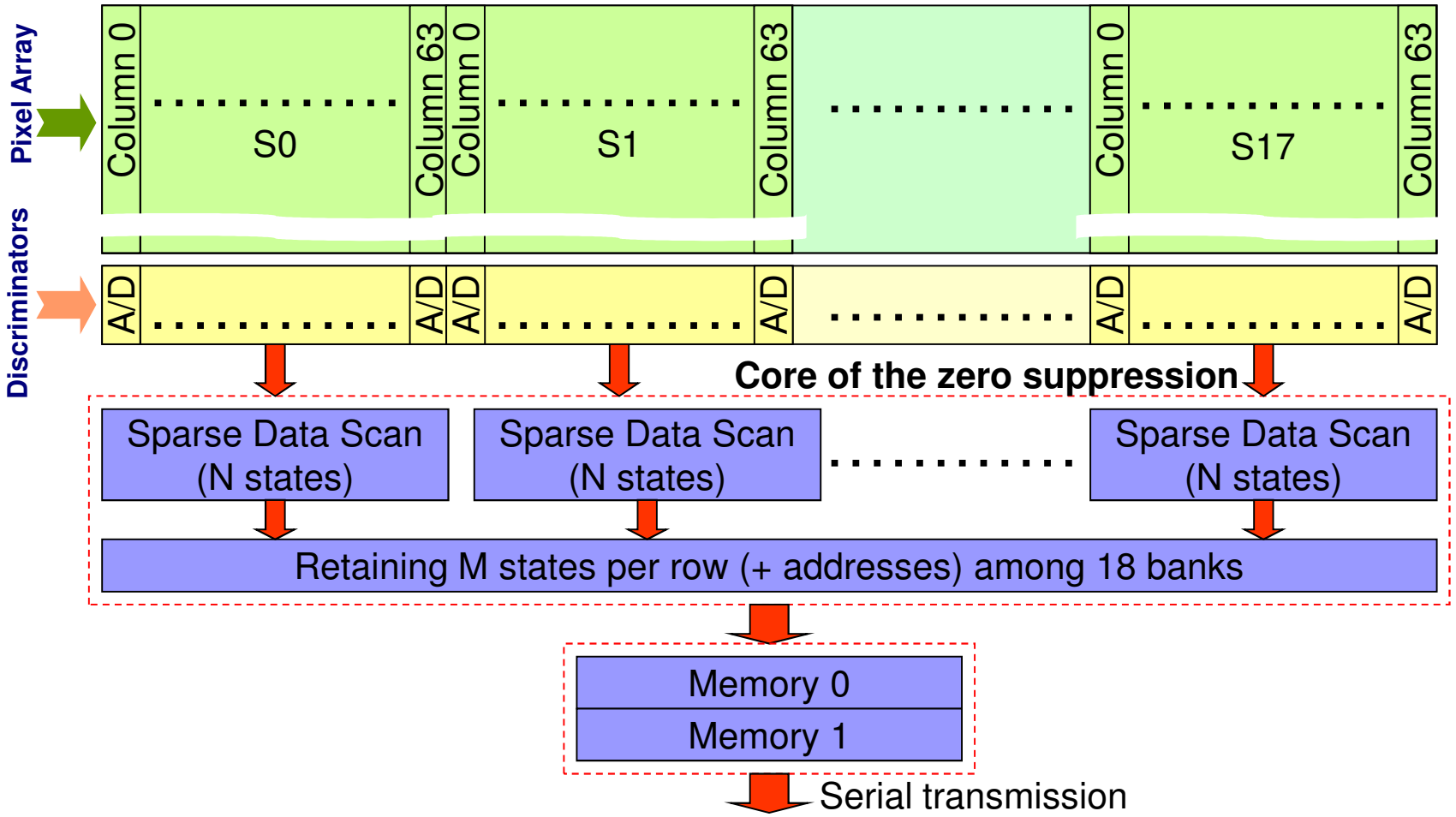
Column-level Double Sampling (DS)➔ reduce pixel to pixel dispersion (FPN)

- *Discriminator design considerations:*
  - *Small input signal ➔ Offset compensated amplifier stages*
  - *Pitch: 16.4 µm (pixel pitch: 18.4 µm)*
  - *A/D conversion time = row read out time (~160 - 200 ns)*
  - *1152 discriminators ➔ Low power consumption (~230 µW/discriminator)*
- *Reference voltages (threshold) & clamping voltage are analogue signals which have to apply to 1152 discriminators (~2 cm long line)*
  - *Have to consider RC distribution line + successive charge rejections*
  - *Even an ideal voltage source CANNOT provide stable references*
    - *Need stable signals during "RD" & "CALIB" periods*
    - *Ex. RD (3 CK ➔ ~ 30 ns)*
  - ➔ *1152 discriminators are divided into **4 groups, 4 bias DAC***
    - *compensate process dispersions of discriminators*

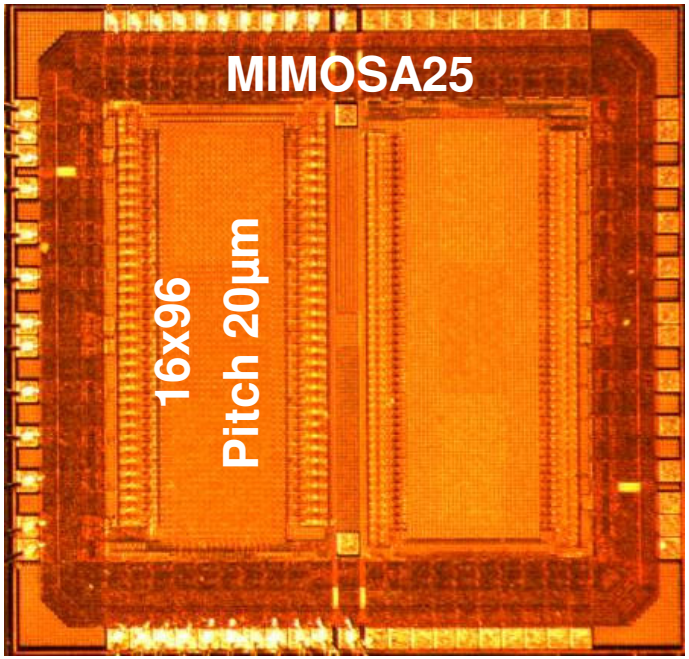
Readout path: zero suppression + memories

- *Connected to column-level discriminators outputs*
- *Zero suppression is based on row by row sparse data scan readout*

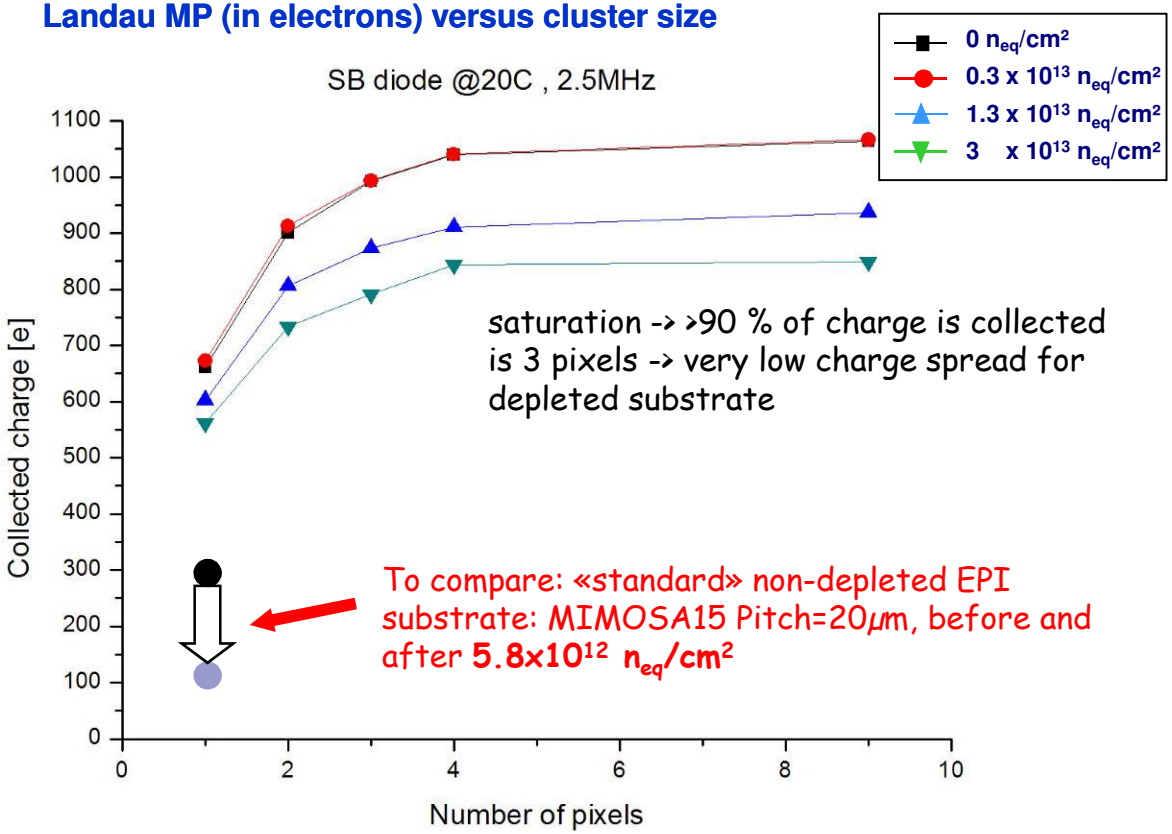
➔ *See poster: A. Himmi et al. "A Zero Suppression Micro-Circuit for Binary Readout CMOS Pixel Sensors"*



MIMOSA25 in a high resistivity epitaxial layer



Landau MP (in electrons) versus cluster size



- *20 µm pitch, + 20 °C, self-bias diode @ 4.5 V, 160 µs read-out time*
- *Fluence ~ (0.3 / 1.3 / 3·)10^{13} n_{eq}/cm^2*
- *Tolerance improved by > 1 order of mag.*
- *Need to confirm ε_{det} (uniformity !) with beam tests*

Using 3DIT to improve MAPS performances

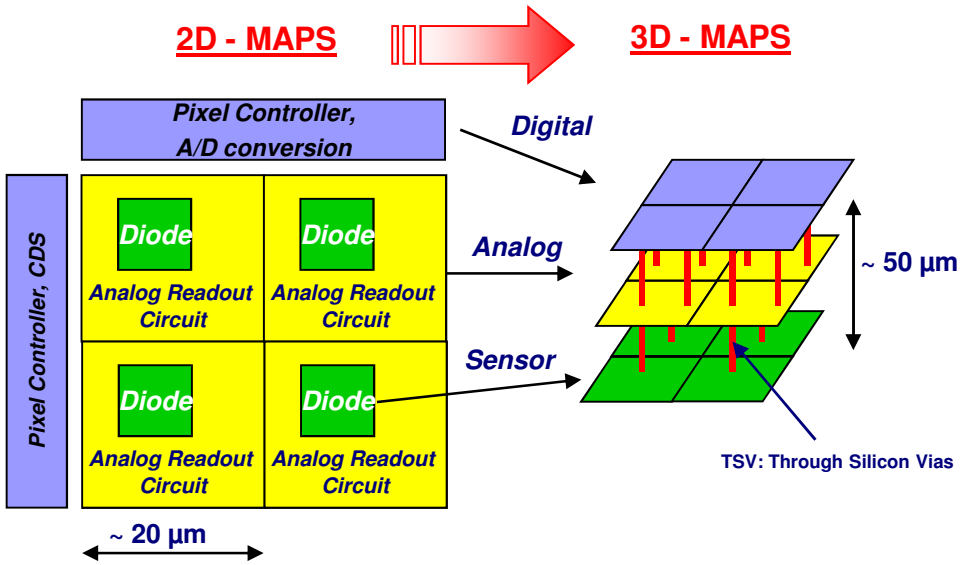
- ***3DIT are expected to be particularly beneficial for MAPS :***
  - *Combine different fabrication processes*
  - *Resorb most limitations specific to 2D MAPS*

- ***Split signal collection and processing functionalities, use best suited technology for each Tier :***
  - *Tier-1: charge collection system ➔ Epitaxy (depleted or not), deep N-well ? ➔ ultra thin layer ➔ X_0 ↓*
  - *Tier-2: analogue signal processing ➔ analogue, low I_{leak}, process (number of metal layers)*
  - *Tier-3: mixed and digital signal processing*
  - *Tier-4: data formatting (electro-optical conversion ?)*

  > *digital process (number of metal layers) feature size ➔ fast laser driver, etc.*

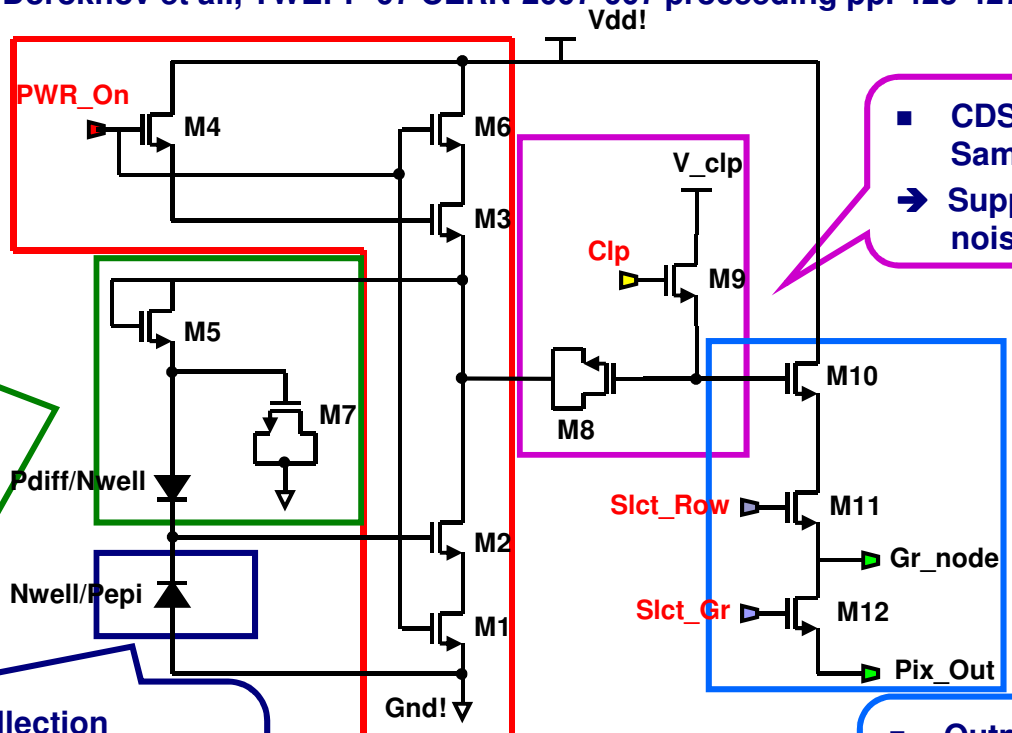
➔ **Run in Chartered - Tezzaron technology**

- *130 nm, 2-Tier run with "high"-res substrate (allows m.i.p. detection)*
  - *Tier A to tier B bond ➔ Cu-Cu bond*
- *3 D consortium: coordinated by FermiLab*
  - *FermiLab*
  - *INFN*
  - *IN2P3-IRFU*
  - *Univ. of Bonn*
  - *CMP*



Readout Path: Pixel

See Ref. A. Dorokhov et al., TWEPP-07 CERN-2007-007 proceeding pp. 423-427



- Negative feedback M5 & M7 low-pass filter
- ➔ Decrease the OP point variation due to process dispersion
- Self biased diode
- M5 Enclosed Layout Transistor
- ➔ Minimise leakage current

- CDS (Correlated Double Sampling): Clamping
- ➔ Suppress fixed pattern noise (FPN)

- Key element for charge collection
- ➔ Optimisation dimension & geometry
- Replace thick oxide surrounding Nwell diode ➔ thin oxide for tolerance to Ionising radiation

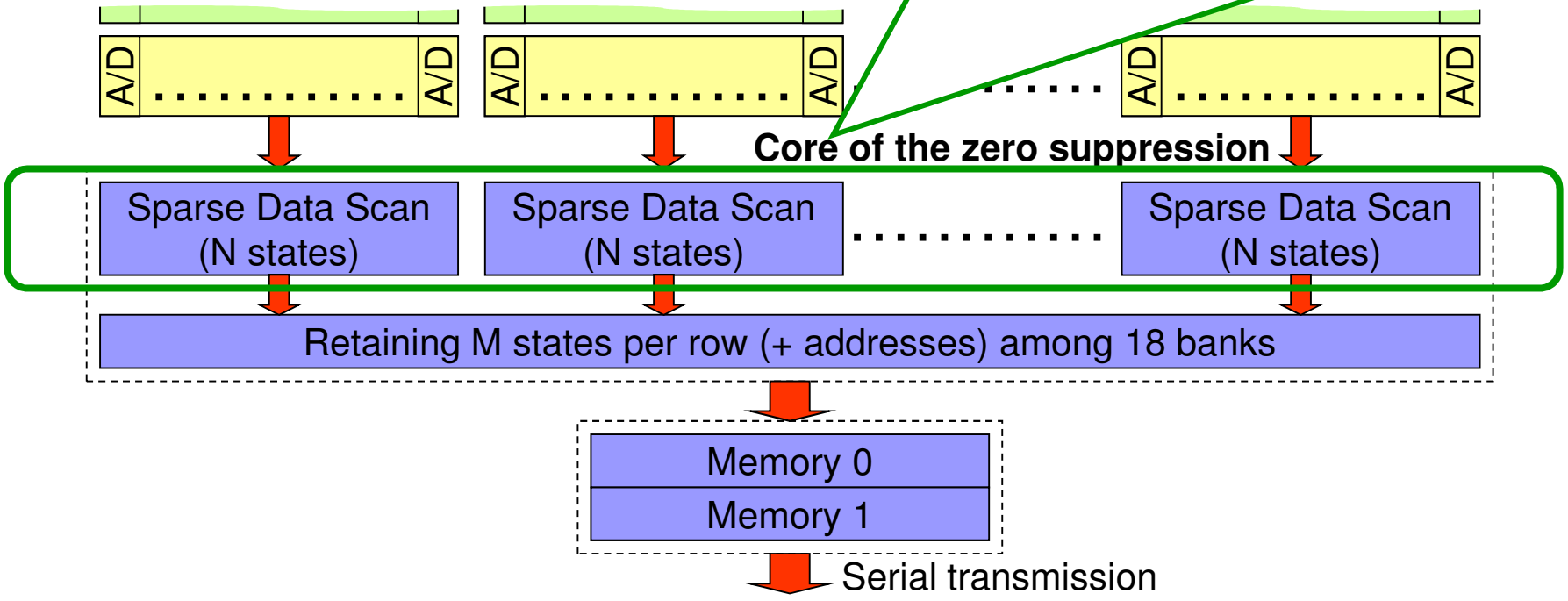
- Output stage: SF (M10)
- 1 column split into 36 groups
  - ➔ Reduce SW cap.

ONLY NMOS transistors can be used, since any additional N-well used to host PMOS transistors would compete for charge collection with the sensing N-well diode

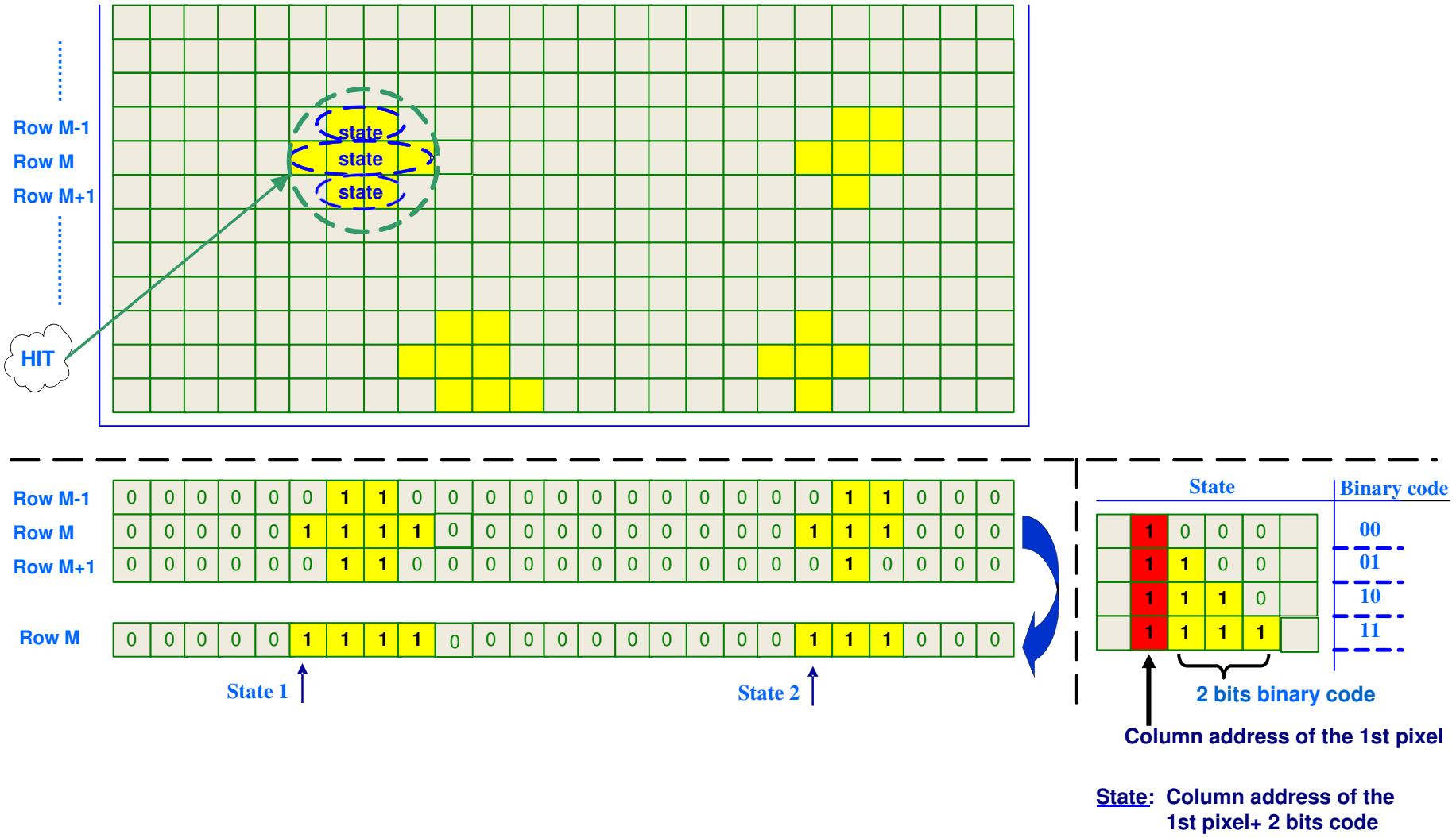
- Modified CS Amplifier: M2 input transistor , M3 & M4 load, M4 for biasing M3
  - AC Gain improved
  - DC Gain & operating point unchanged
- ➔ Resistant to process variation

Readout path: zero suppression + memories

- **1st step:**
  - 1152 columns terminations ➔18 banks // scan
  - Based on a sparse data scan algorithm to find hit pixels (discriminator output = "1")
    - Up to 4 contiguous pixel signals above V_{th} will be encoded in a 2 bits state word following by address of the 1st pixel
  - Find up to N states with column addresses per bank



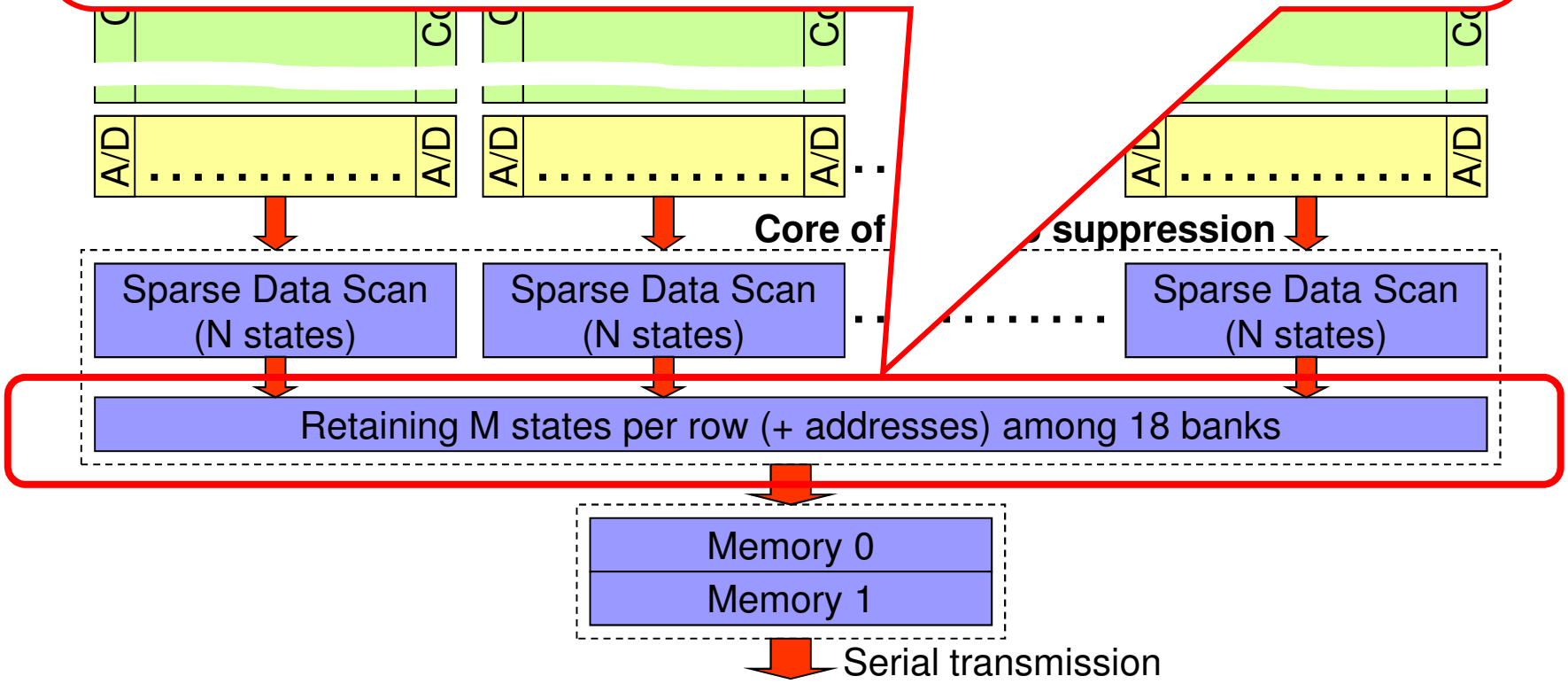
Readout path: zero suppression + memories



State: Column address of the 1st pixel+ 2 bits code

Readout path: zero suppression + memories

- **2nd step:**
  - Read out the outcomes of the 1st step in all banks and keep up to M states
  - Add row and bank addresses



Readout path: zero suppression + memories

N, M, Memory capacity and readout speed depend on hit density

➔ N = 6, M = 9, Memory ~ 40 Kbits, Read-out Freq.: 80, up to 160 MHz

- **3rd step:**
  - Store the outcomes of the 2nd step to a memory
  - The memory is made of 2 IP's buffers ➔ continuous read-out
    - 1 buffer stores current frame,
      1 buffer is read out previous frame
  - Serial transmission by LVDS pad