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About 10000 frames per second readout MAPS for the EUDET beam telescope

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Designed and manufactured in a commercial CMOS 0.35 µm Opto process for equipping the EUDET beam telescope, MIMOSA-26 is the first reticule size pixel sensor with digital output and integrated zero suppression. It features a matrix of pixels of 576 rows and 1152 columns covering an active area of ˜224 mm2. A single point resolution, better than 4 µm, is expected with a pixel pitch of 18.4 µm. Its architecture allows a fast readout frequency of ˜10 k frames/s. The workshop contribution will present, in details, the chip design, test and its major characterisation outcome.

Summary

A high resolution beam telescope, based on CMOS Monolithic Active Pixel Sensors (MAPS), is being developed within the EUDET collaboration a coordinated EU (FP 6) detector R&D program for the future International Linear Collider (ILC). The IPHC and IRFU team is involved in this Joint Research Activity (JRA) to develop a fast readout MAPS, called MIMOSA-26, for equipping the telescope. The latter will consist of 2 arms of 2x3 MAPS measurement planes, providing an extrapolated resolution better than 2 µm on the surface of the device under test.

The MIMOSA-26 architecture is based on the successful design of the two separate prototyping lines, completed with the MIMOSA-22 and SUZE-01 chips, respectively. The first line addresses the upstream part of the signal detection, analogue processing and analogue to digital conversion, while the second is dedicated to data sparsification and formatting. Combining the architectures of these two prototype circuits, MIMOSA-26 features a pixel matrix of 1152 columns and 576 rows with a pixel pitch of 18.4 µm. Each pixel hosts an N-well/P-epi charge collection diode, a preamplifier and a correlated double sampling (CDS) functionality minimizing the low frequency noise. The pixel array is read out in rolling shutter mode sweeping the array row by row. At the bottom of the pixel array, a stage of 1152 offset compensated discriminators, each one connected to a column, performs the analogue to digital conversion. The digital data are then treated by a zero suppression circuitry integrated on the same chip in order to restrict the chip output to useful information. The compressed data of a frame are buffered alternatively in 2 SRAM allowing a continuous readout. They are then sent out during the acquisition of the next frame via one or two 100 M bits/s LVDS transmitters. The on-chip programmable biases, the voltage references and the selection of the test modes are set via a JTAG controller.

The MIMOSA-26 architecture is the outcome of a ten years long R&D activity. It is expected to be the cornerstone of the design of various CMOS pixel sensors foreseen to equip vertex detectors of several subatomic physics experiments, such as the STAR Heavy Flavour Tracker (HFT) upgrade or the CBM Micro Vertex Detector (MVD). It is also proposed for the ILC vertex detector.

MIMOSA-26 returned from foundry in February 2009. Extensive tests are going on in the laboratory; those preliminary results indicate that the sensor is likely to meet the EUDET telescope specifications. A temporal noise of 0.64 mV and a Fixed Pattern Noise (FPN) of 0.29 mV have been observed, for one quarter of the pixel array with its associated discriminators. These values are fully compatible with those obtained with MIMOSA-22. The remaining three quarters of the matrix exhibit similar performances, showing a good uniformity of the whole 576 x 1152 pixels associated to the 1152 discriminators.

Details of the MIMOSA-26 chip design and preliminary characterisation results will be presented. Possible upgrades and extensions to improve the device performances will be discussed.

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