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The First Vertically Integrated MPW Run for HEP

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In 2008 a consortium of 15 international institutions was formed to pursue the development of 3D integrated circuits at a commercial foundry. The first MPW run from the consortium was submitted to Tezzaron. Wafers were fabricated at Chartered Semiconductor in the 130 nm process. These wafers were then assembled by Tezzaron into vertically integrated circuits. More than fifteen designs were submitted. Designs include custom analog and digital circuits for particle detection in ATLAS, CMS, ILC and other experiments. Issues related to the submission of the MPW run and initial results will be presented.

Summary

Interest in 3D integrated circuits for HEP has grown steadily since talks at Perugia and Ringberg in 2006. Early 3D work utilized the MIT Lincoln Lab SOI process. Based on that early work a group of international institutions has come together to explore and develop 3D integrated circuit concepts for HEP.

One of the first truly commercial processes for 3D integrated circuits is offered by Tezzaron Semiconductor. Tezzaron has been in the business of offering 3D integrated circuits for commercial customers for a number of years. Although their main business is in 3D stacked memories, they have also produced 3D chips for imaging, FPGAs, and microprocessors. Recently Tezzaron has agreed to host MPW runs for HEP and a separate DARPA funded program. The MPW runs allow a large number of customers to explore 3D circuits using a commercial foundry at a reasonable cost.

In 2008, a consortium of 15 institutions was formed with members from France, Italy, Germany, Poland, and the United States. The consortium placed a purchase order with Tezzaron to produce vertically integrated circuits using the Chartered 130 nm low power process. The circuits have two tiers of electronics fabricated in a via first process using a single set of masks. The two tiers are bonded together using copper to copper bonding. More than fifteen circuit designs and dedicated test circuits were submitted in ten major sub reticules. Two of the designs are for ATLAS pixel upgrades that would separate analog and digital electronics on to two different tiers, allowing for higher circuit density and separate substrates for analog and digital circuits. Another design explores a new trigger concept for the CMS upgrade that uses two closely spaced sensor layers, an interposer, and separate tiers of a 3D circuit for each sensor layer. Other designs explore pixel designs for the ILC, and various MAPS designs. There are numerous test structures and circuits for evaluating the 130 nm process for radiation tolerance and viability for cryogenic operation.

The designs were completed in a relatively short period of time in part due to the sharing of designs and code developed by various members of the consortium. Thus in addition to the cost savings for chip fabrication afforded to each member by means of the MPW run, significant manpower saving was also realized. Initial test results from some of the circuits will be presented. Future MPW runs are planned. Although it is still early, both CMP and MOSIS have shown interest in our Tezzaron/Chartered MPW runs which could have significant long term benefits for HEP.

1) R. Yarema, Fermilab Initiatives in 3D Integrated Circuits and SOI Design for HEP, ILC Vertex Workshop, Ringberg Castle, Tegernsee, Germany, May 29-31, 2006

Primary author: Mr YAREMA, Ray (FNAL)

Presenter: Mr YAREMA, Ray (FNAL)

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