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A Radiation Tolerant 4.8 Gb/s Serializer for the Giga-Bit Transceiver

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This paper describes the data serializer of the GigaBit Transceiver (GBT) which has been under development for the LHC upgrade (SLHC). The circuit operates at 4.8 Gb/s and is implemented in a commercial 130 nm CMOS technology. The serializer occupies an area of 0.6 mm² and its power consumption is 300 mW. The paper focuses on the techniques used to achieve radiation tolerance and on the simulation method used to estimate the sensitivity to SETs.

Summary

The GBT project aims at designing a radiation tolerant optical transceiver operating at 4.8 Gb/s within the framework of the luminosity upgrade of the LHC machine and the experiments. The GBT will replace the three communication links currently in use, namely the timing, trigger and control system (TTC), the data acquisition system (DAQ) and the slow control system (SC), therefore providing a single solution for all the communication needs at the LHC.

The GBT chip set will include a radiation tolerant serializer (SER) which converts 120-bit-wide, 40 Mb/s parallel data into 4.8 Gb/s serial stream. Operating from a single 1.5 V supply with a power consumption of 300 mW and occupying an area of 0.6 mm², the circuit accepts CMOS-level data and control signals. The SER outputs a pseudo-differential signal with a worst-case simulated pattern-dependent jitter of less than 6 ps at 4.8 Gb/s.

The SER architecture is based on dividing the 120-bit frame into 3 equal sized framelets stored in separate shift-registers with a conversion rate of 40 Mb/s and multiplexing these shift registers to the output at one third of the full speed. This architecture minimizes the number of components operating at full speed.

A fully integrated programmable charge-pump phase-locked loop (CP-PLL) synthesizes an internal 4.8 GHz bit clock from the 40 MHz LHC reference. Due to strong dependency of the SER output jitter on the CP-PLL behavior, the values of the loop filter resistor and the charge-pump current are controlled by D/As having 2 and 4-bit resolution, ranging from 1.5 KOhm to 6.0 KOhm and from 1 μA to 100 μA, respectively.

The CP-PLL is designed to be tolerant to single event transients (SET) via employing custom-designed devices for higher performance and triple-well structures for better isolation. Triple modular redundancy (TMR) is as well used in the feed-back divider of the CP-PLL for mitigating the single event upsets (SEU). The design performance of interest along all the processing corners is limited to the temperature range of [-20 C°, 100 C°] and the power supply variation of pm 10%.

A GBT prototype has been designed in a commercially available 130 nm CMOS technology as a flip-chip. By the time of this writing, it is in the process of being submitted to the foundry for fabrication.

Full text focuses on the functional architecture of the SER, the techniques applied to achieve radiation tolerance and the simulation method used for estimating the circuit sensitivity to SETs.

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