Reduction techniques of the back gate effect in the SOI Pixel Detector

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for the SOI Pixel collaboration
http://rd.kek.jp/project/soi/

SOI Pixel Collaboration

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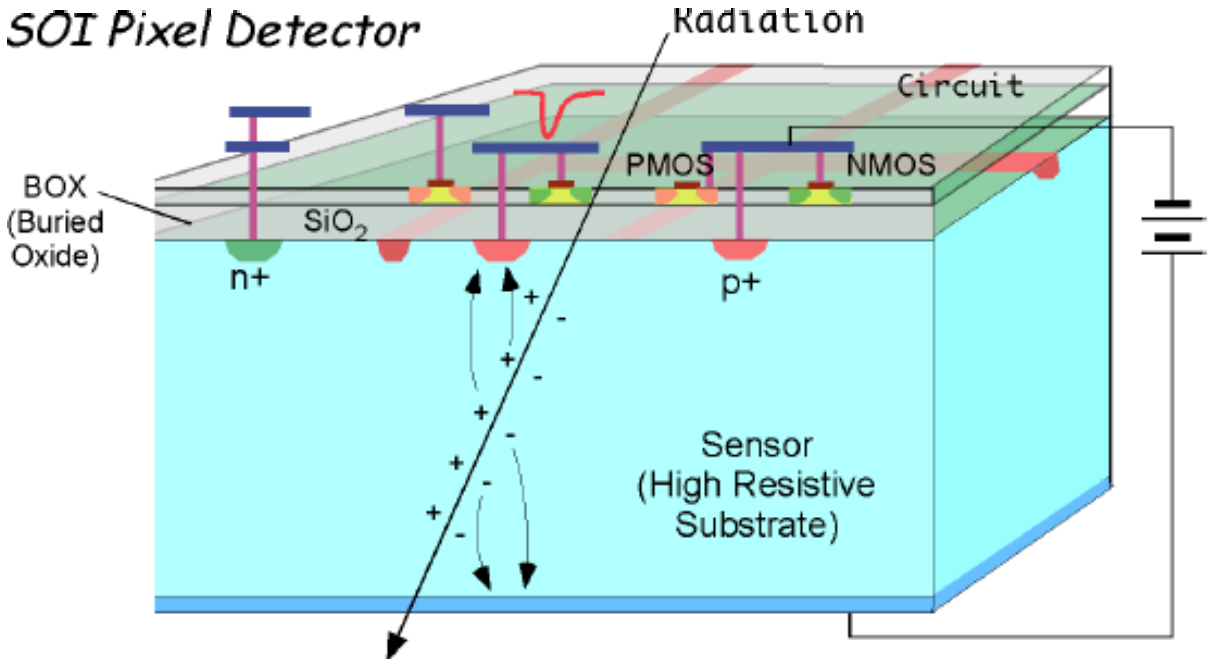
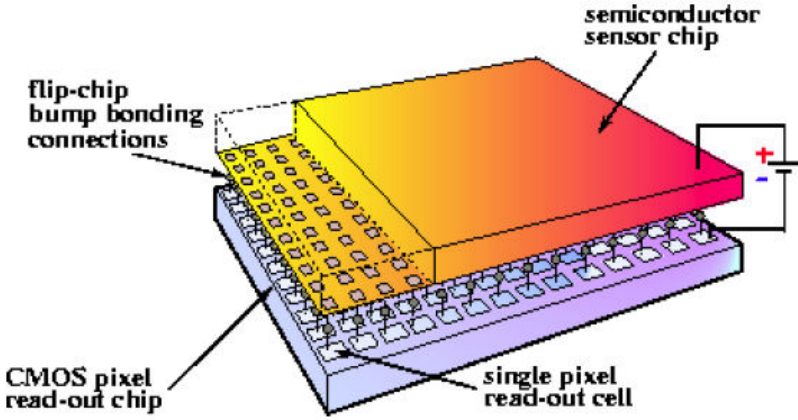
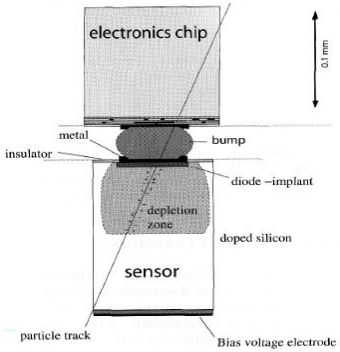
Outline

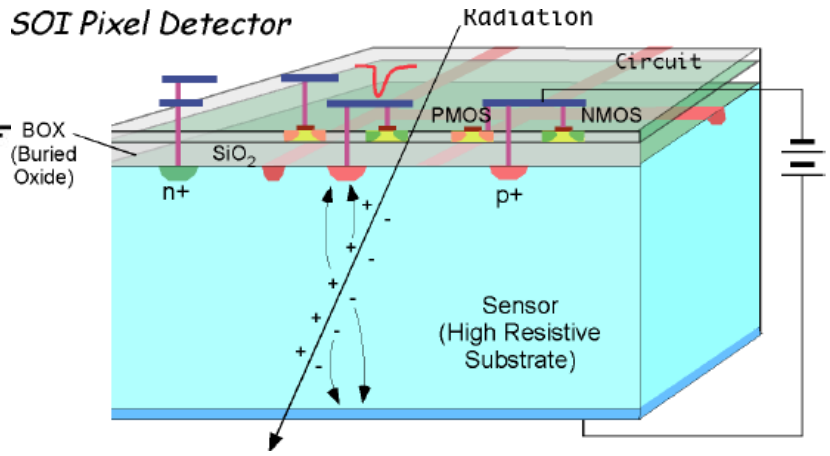
1. SOI technology and SOI pixel detector
2. Pixel Test Results
3. On going R&Ds
4. Summary



Hybrid Pixel v.s. SOI pixel





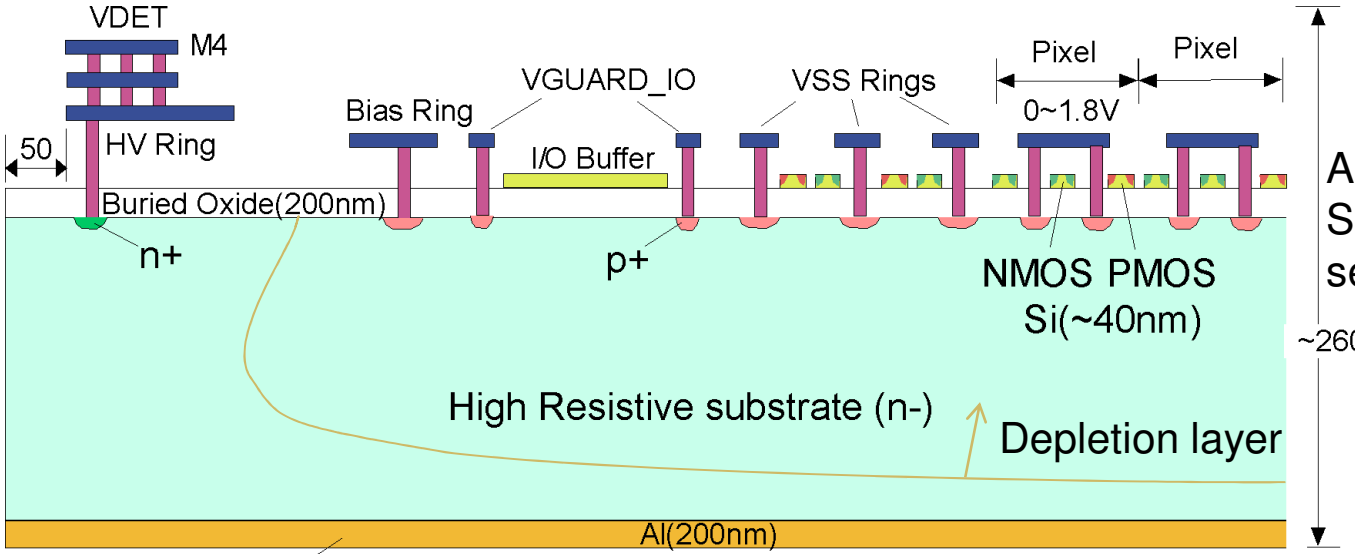


- Hybrid Pixel (conventional pixel detector)
  - Fabricate Sensor and Readout chip individually.
  - Make contacts by bump bonding for each pixel.
  - Granuarity is limited (~50um) from bump-bonding fabrication .
  - Speed and Gain reduction by parasitic capacitance.
  - It becomes thick detector by bump-bonding structure.

- SOI Pixel
  - Bonded wafer: High Resistivity (Sensor) and Low Resistivity (CMOS).
  - Truly Monolithic Detector
    - High Density, Low material, Thin device
  - No mechanical bonding.
    - High yield, Low cost.
  - Fully depleted sensor with small capacitance of the sense node.
    - ~10fF, High gain, Low noise
  - Based on Industrial standard technology
    - Cost benefit and scalability.
  - No Latch-up, Radiation hardness, Low power.
  - Low to High temperature operation (4K-300C).
  - …

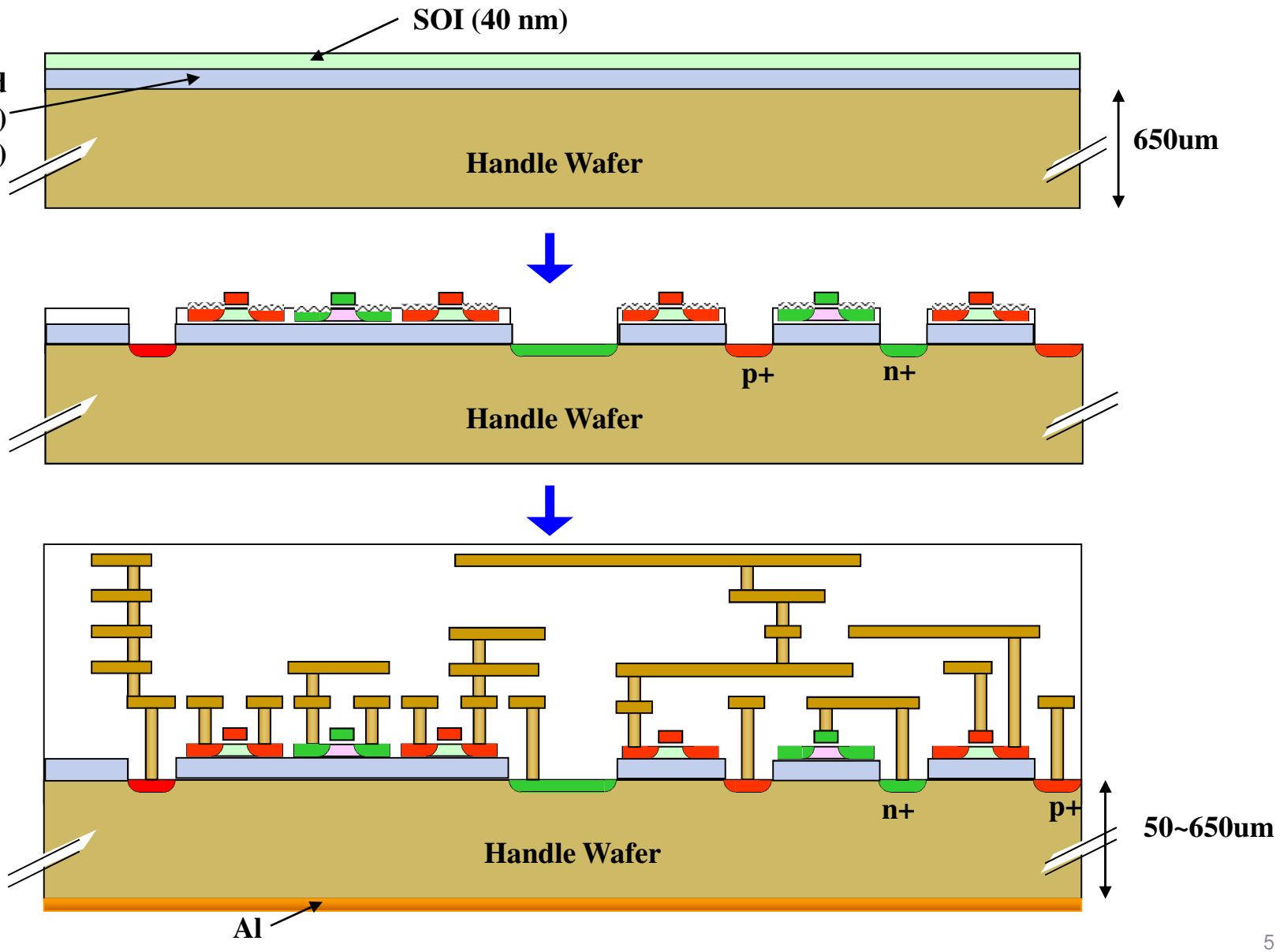
Oki 0.2μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS (OKI) 1 Poly, 4 Metal layers, MIM Capacitor, DMOS option Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、700 Ω-cm (*n-type)*, 650 μm thick
Backside	Thinned to 260 μm, and sputtered with Al (200 nm).

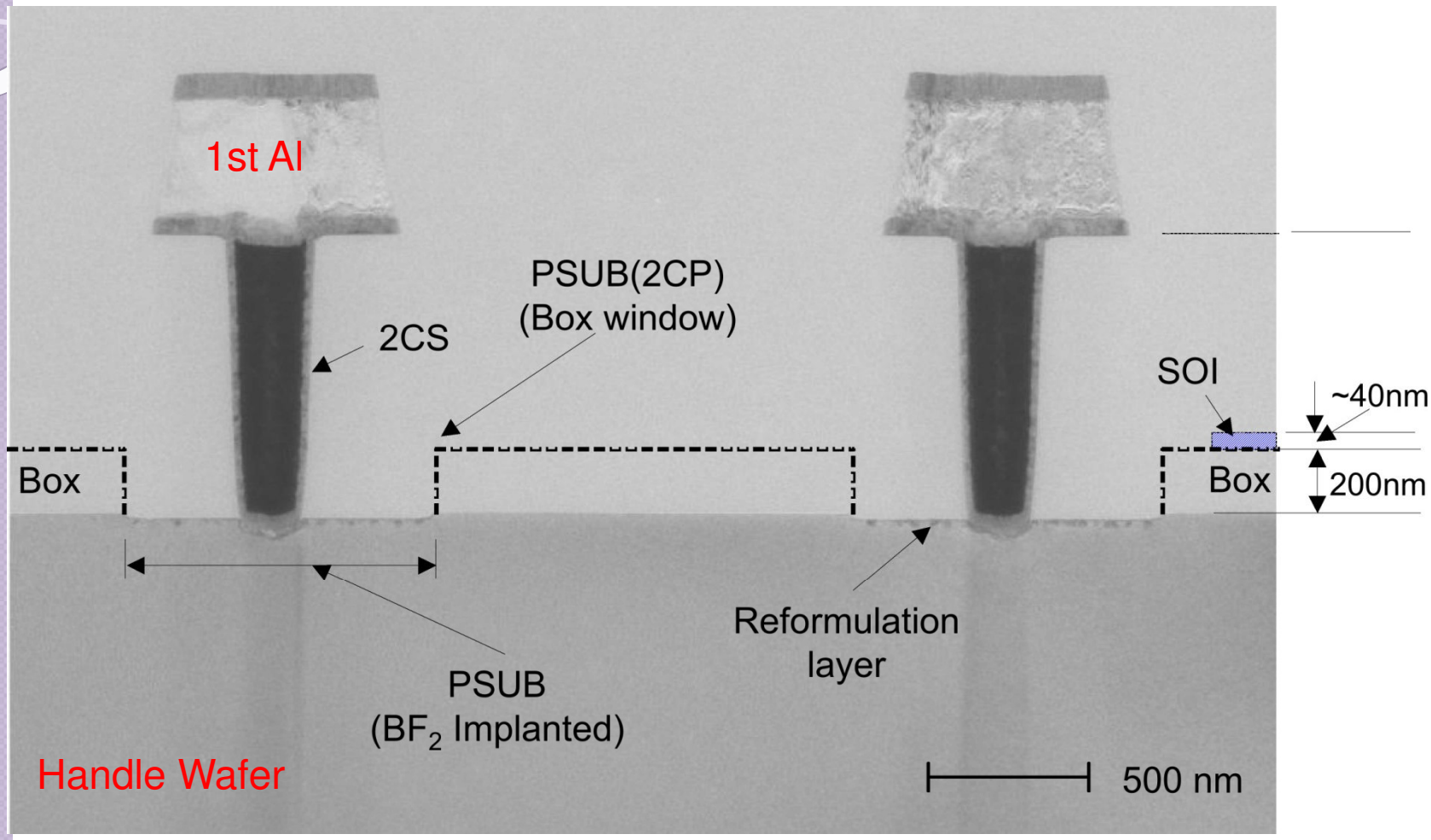


An example of a SOI Pixel cross section

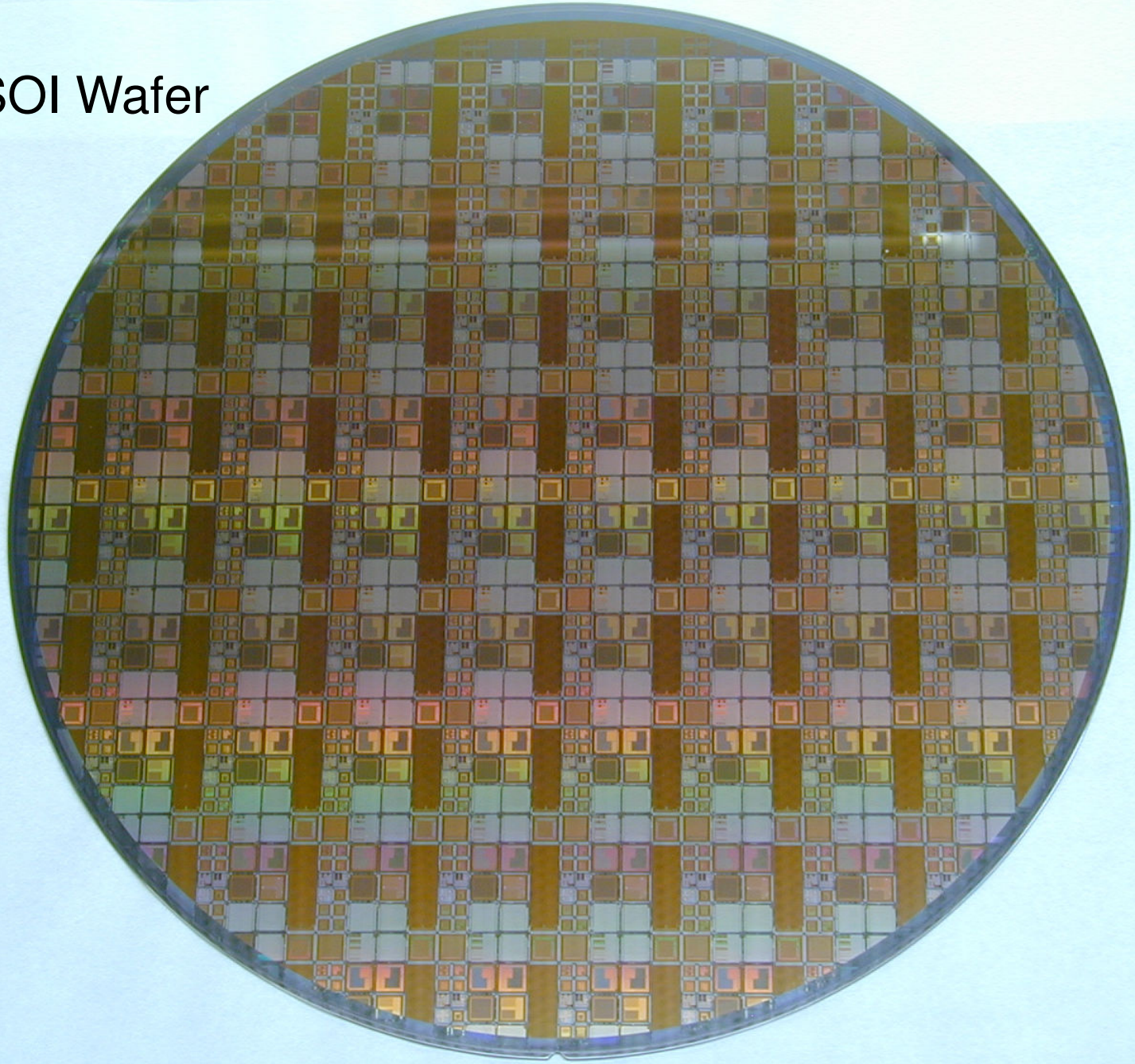
SOI Pixel process flow



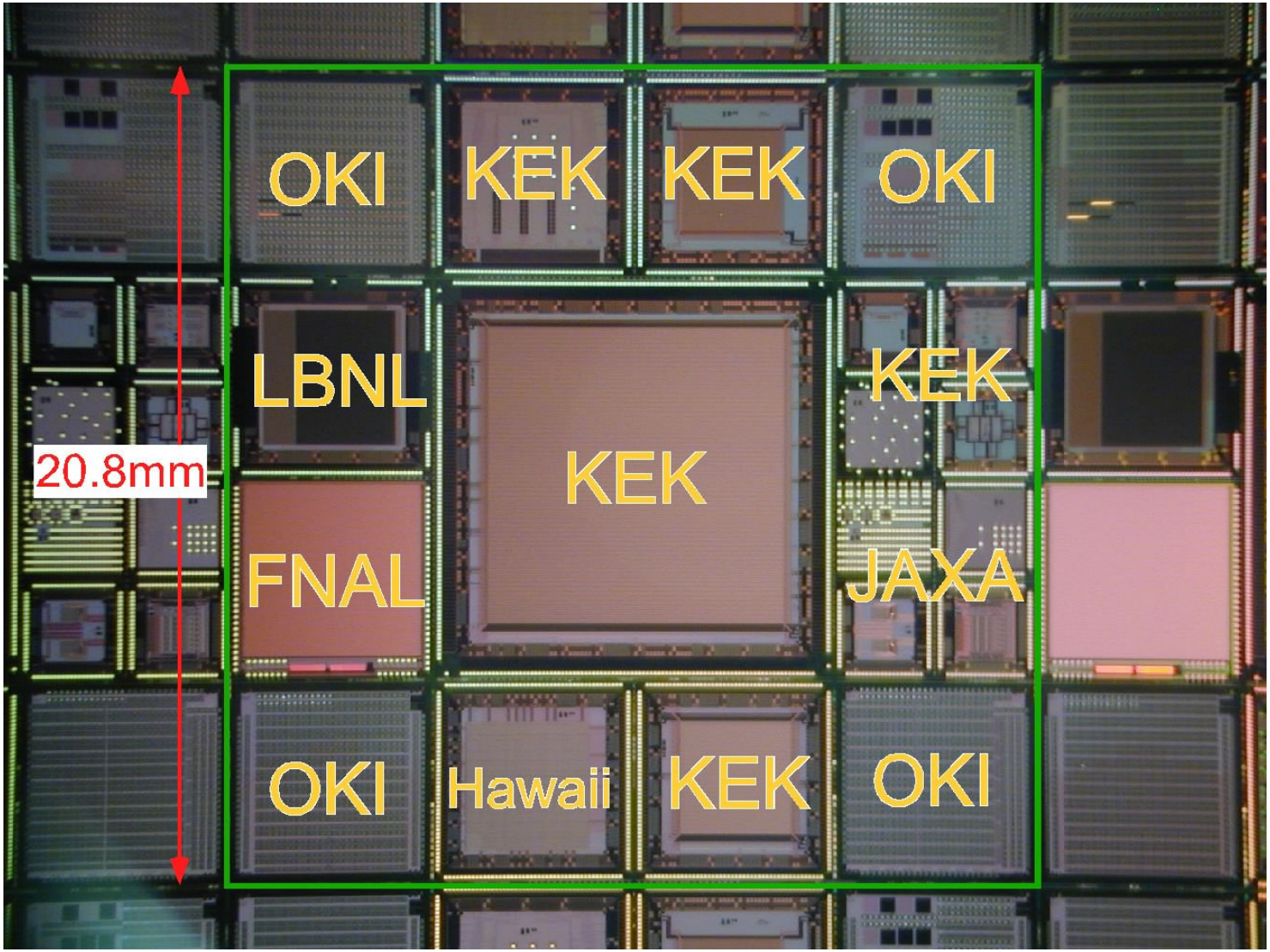
Metal contact & p+ implant



8inch SOI Wafer



KEK SOI Multi Project Wafer (MPW) run



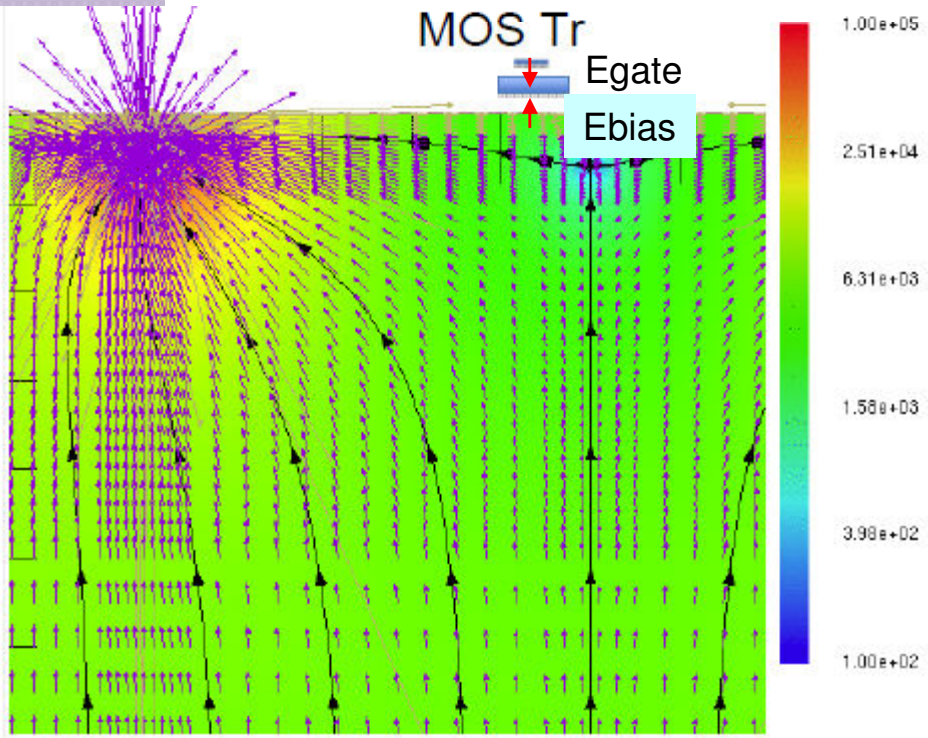
- 3 MPW runs are scheduled in 2009 FY.
- We welcome your Designs.

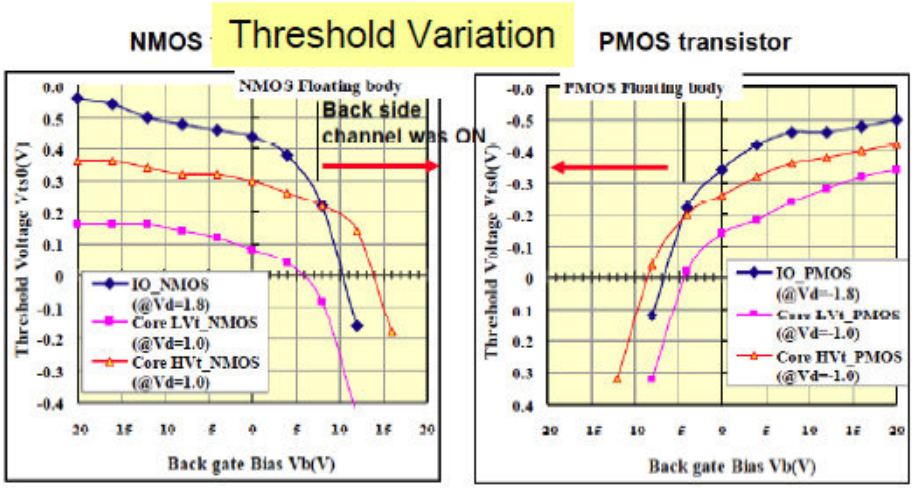
http://rd.kek.jp/project/soi/MPWrun/

Back gate effect on SOI pixel

- Transistors locate very close (=200nm) to the Sensor where high voltage applied.
- Substrate (Sensor) Voltage acts as Back Gate in a MOS transistor, and change its threshold voltage.

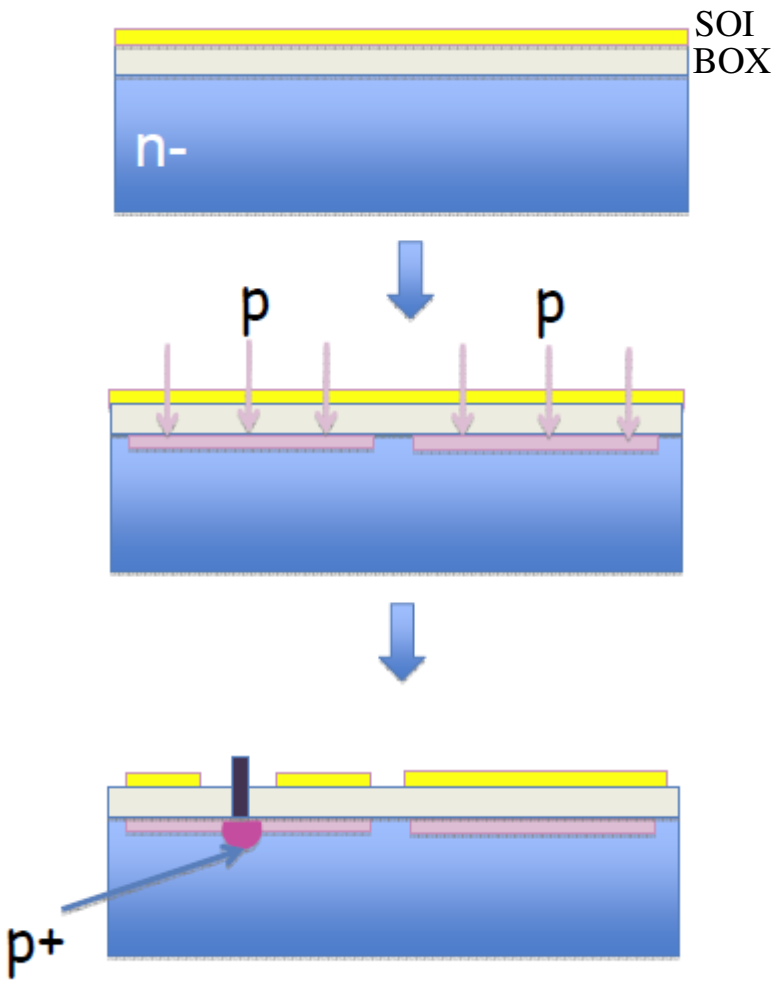
- Unless we solve this dilemma, we cannot operate this detector with fully depleted condition.





Buried p-well technology

- In order to shield the transistors from electrical field from the Sensor,
- Implant p-Well through SOI and BOX layer. (buried p-Well)

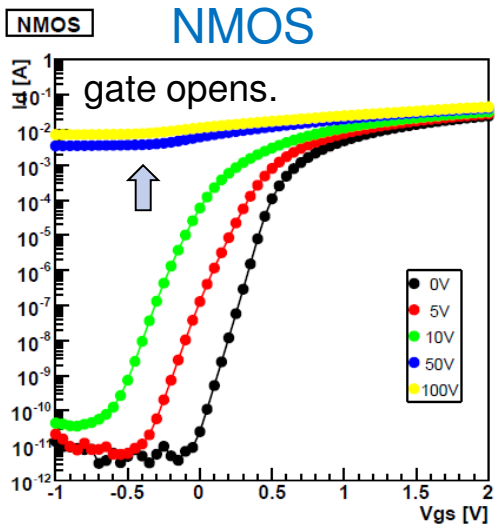


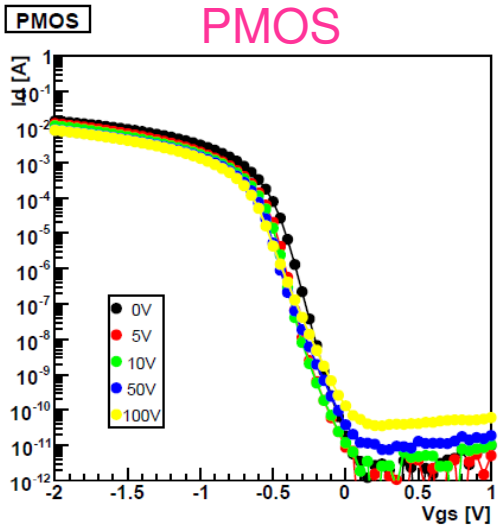
- Benefits:
  - Suppress back gate effects.
  - Reduce electric field around p+ sensor.
  - Less electric field in BOX to improve radiation hardness.

Essential and breakthrough technology to overcome the back gete effect.

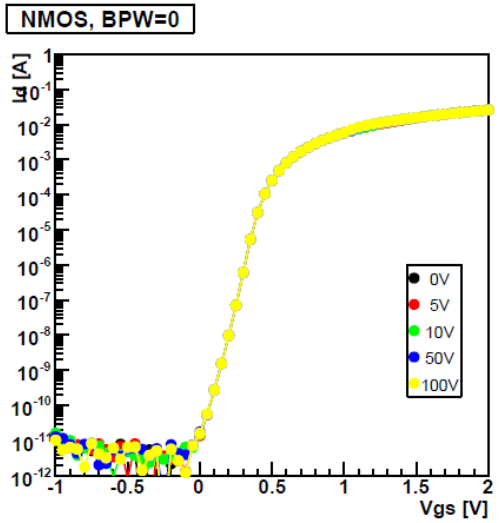
I_d-V_{gs} curve under bias voltage applied

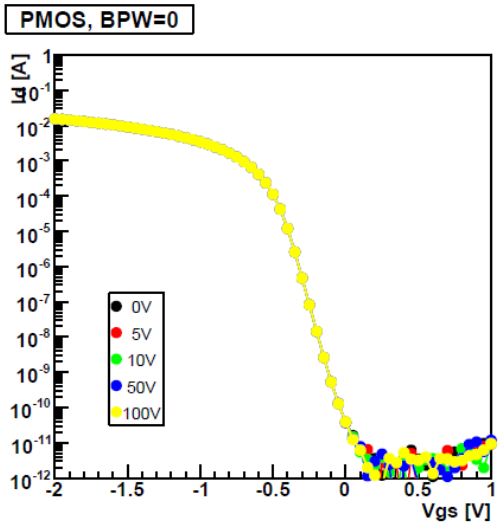
w/o BPW





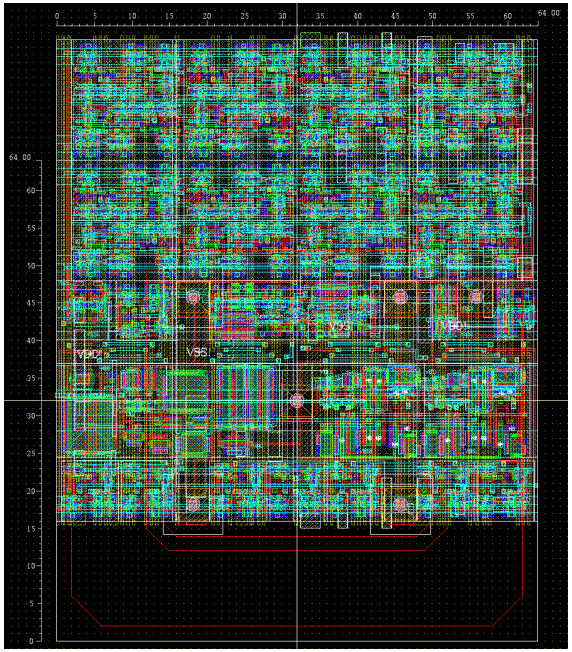
w/ BPW =0V





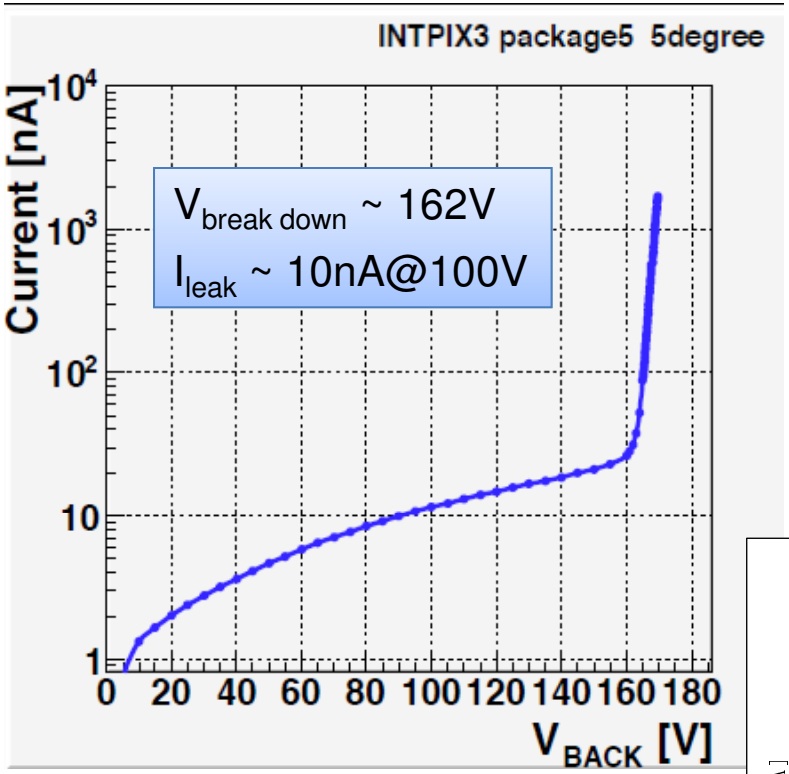
•Back gate effect is effectively suppressed by BPW even at 100V bias voltage.

Pixel test Results

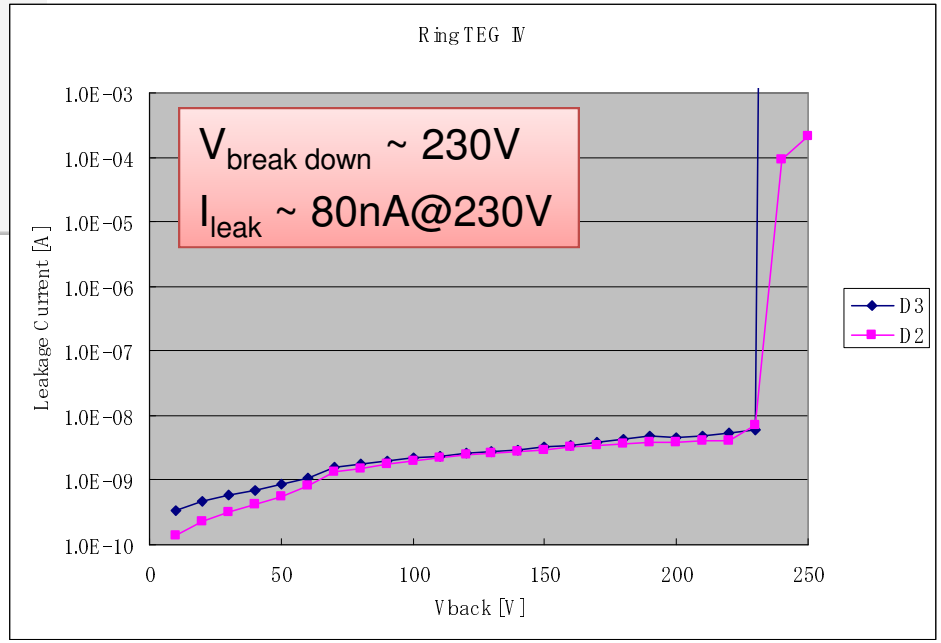


CNTPIX3 pixel

Breakdown voltage & leak current

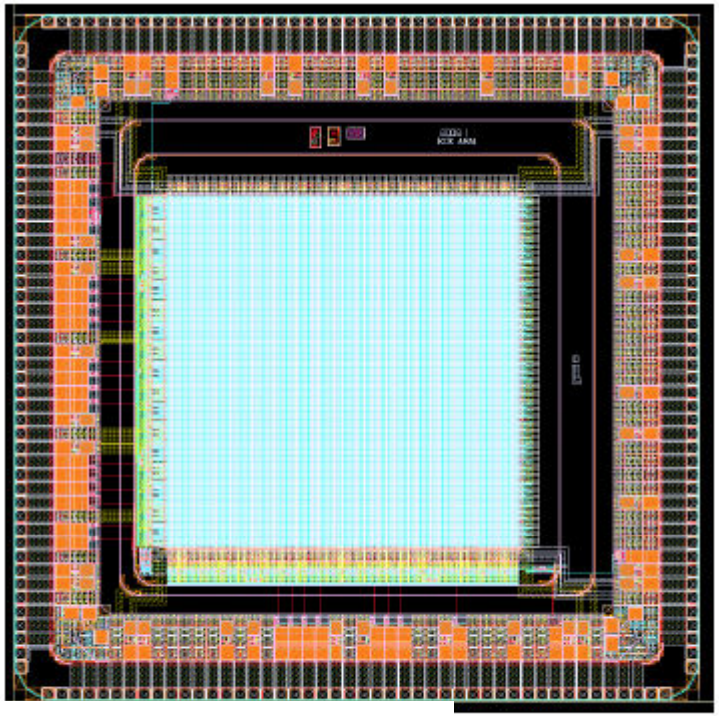


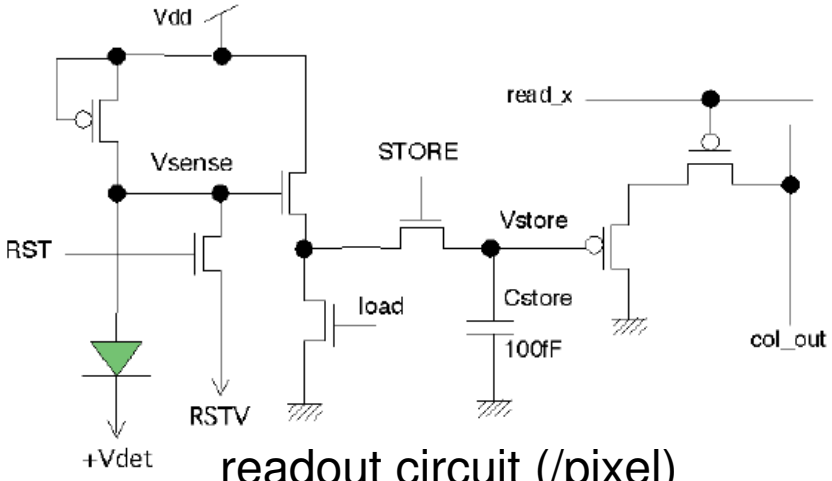
2.5mmx2.5mm chip (INTPIX3)



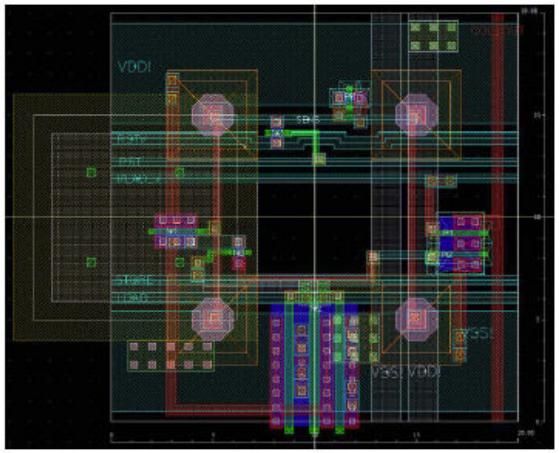
TEG

Integration type Pixel (INTPIX)





readout circuit (/pixel)

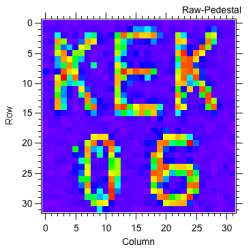


20μm x 20μm pixel

SOI pixel Laser Images

2006

0.64 mm



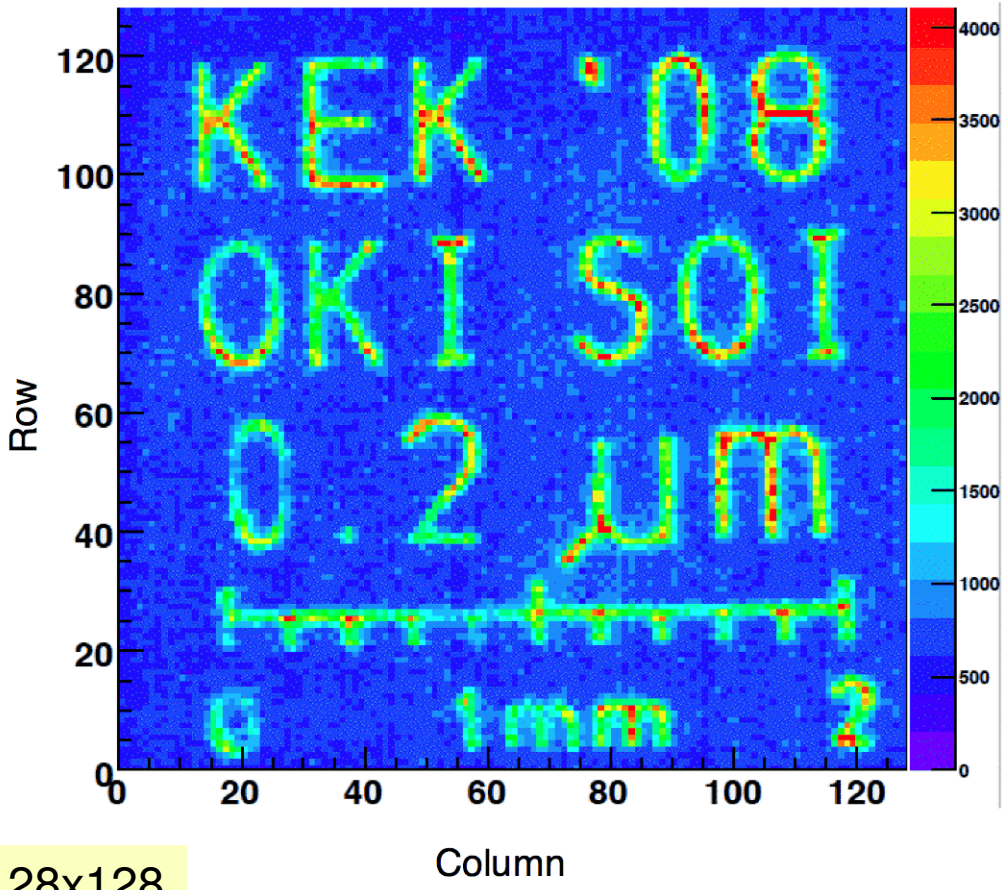
32x32

with Plastic mask

INTPIX2

2008

2.56 mm

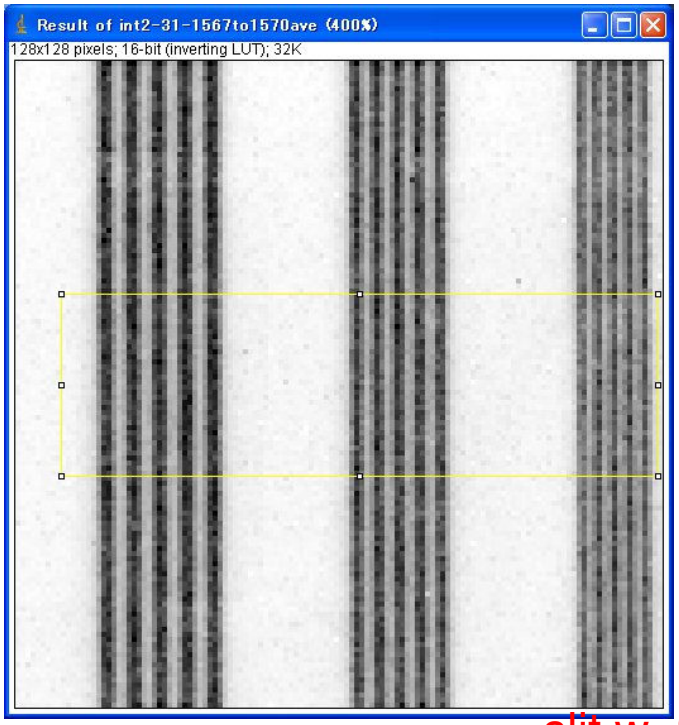


128x128

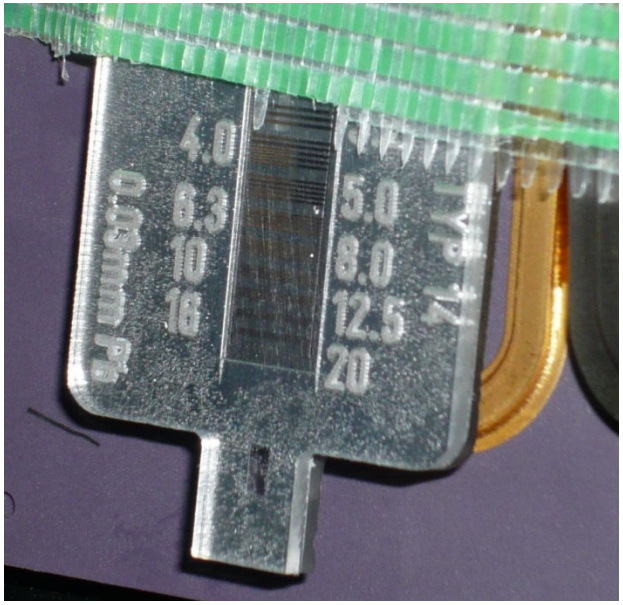
X-ray Irradiation test

INTPIX2
(pixel size=20μmx20μm)

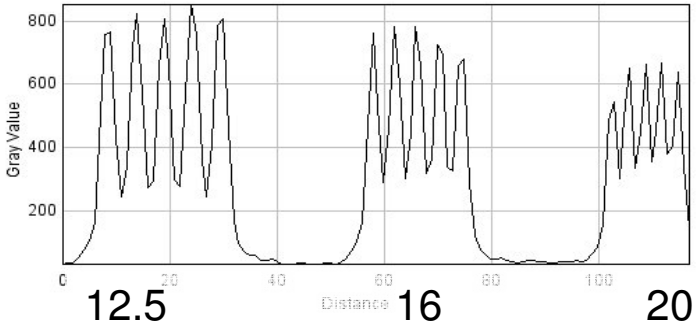
- X-ray generator: Rigaku FR-D
- Target: Cu (Cu Kα ~8keV)
- Power: 30-35 kV, 10-30mA
- Intensity: ~10^4 photons/pixel/sec @30kV, 10mA



slit w=25μm



X-ray Test Chart

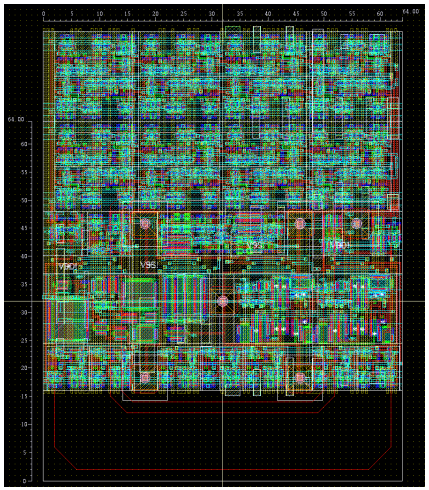


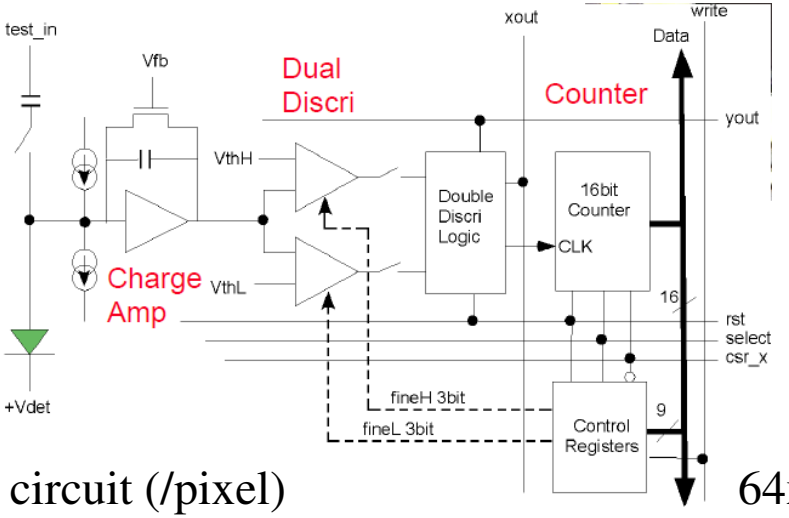
12.5 16 20
[lp/mm]

25 μm Slit is well separated.

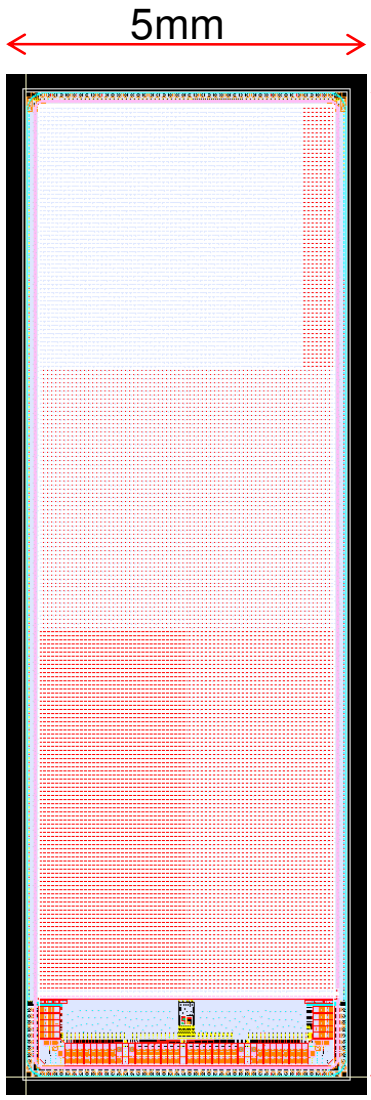
Counting type Pixel (CNTPIX)

- Discriminated signal is counted by a16-bit counter.
- Energy window can be set in each pixel.





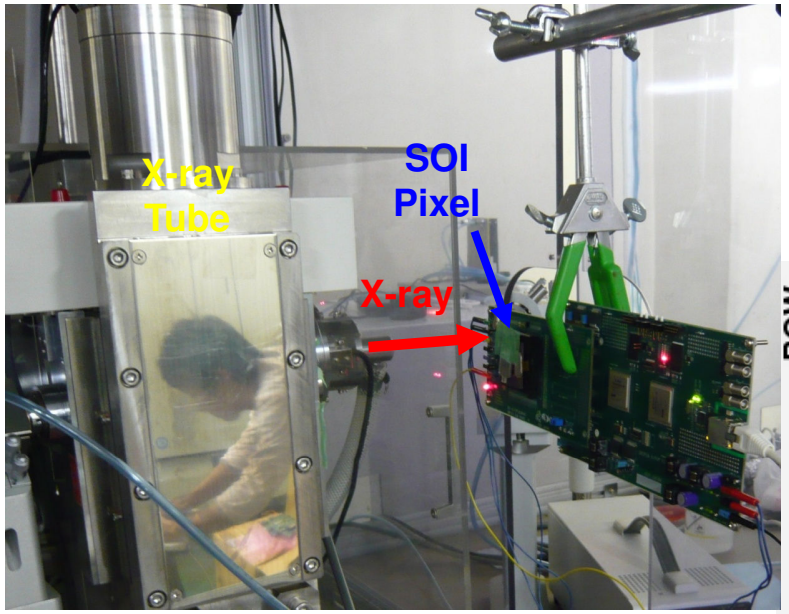
Readout circuit (/pixel)



CNTPIX3
(row:218 x column:72)

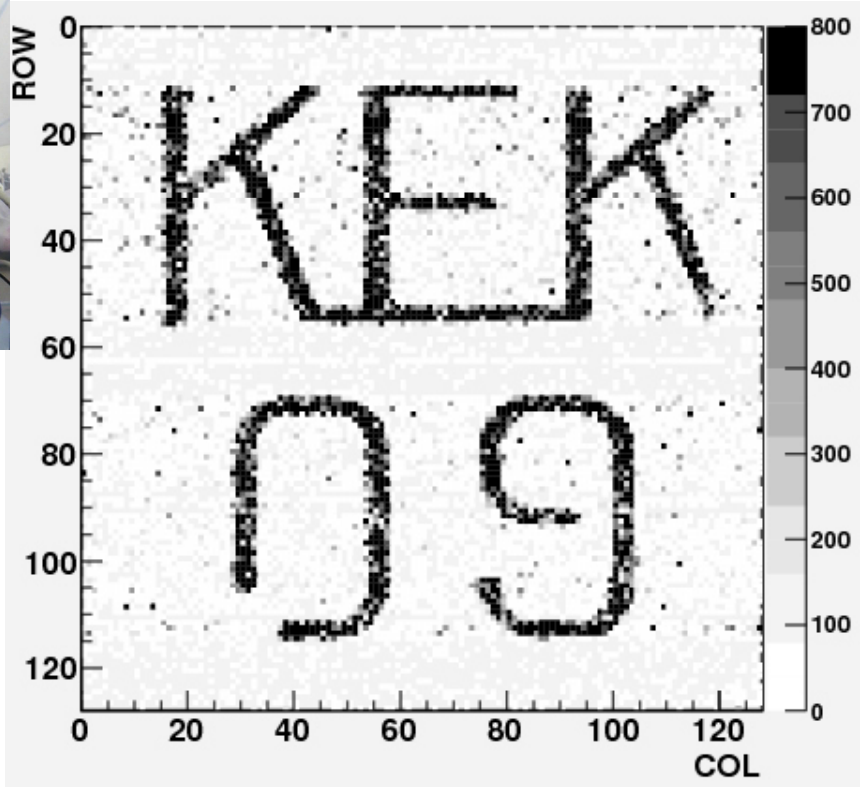
64x64 μm^2

SOI pixel Laser Image (CNTPIX)



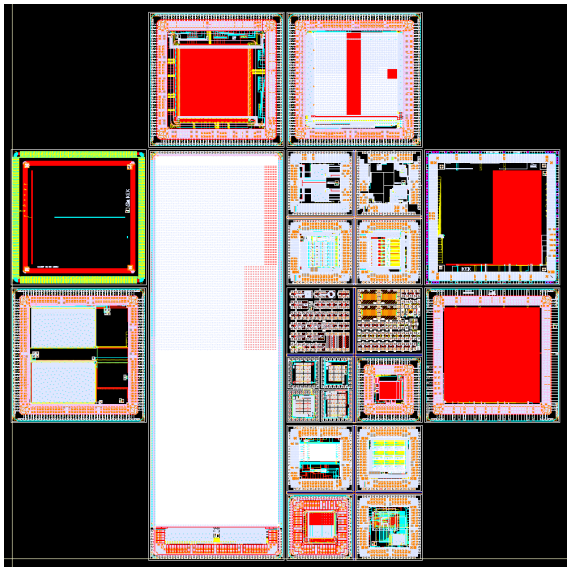
40kV-40mA
Substracted by background count
Integration time 64ms / vth 350mV
Vback=15V

•Image taken by X-ray irradiation

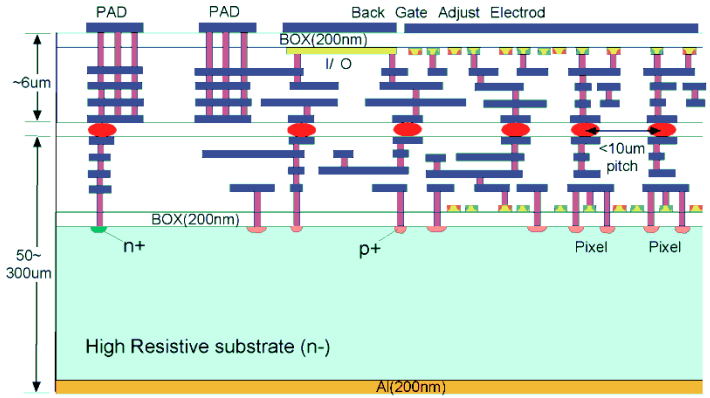


Counter works well

On going R&Ds

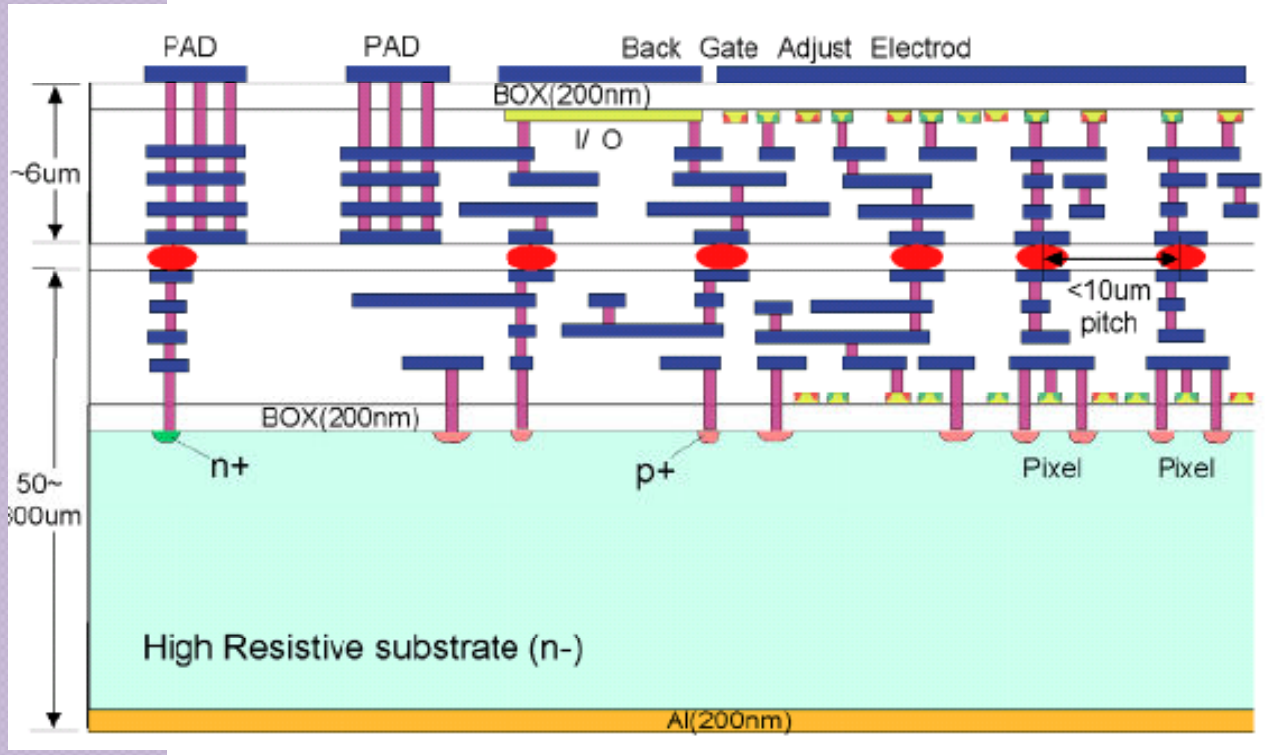


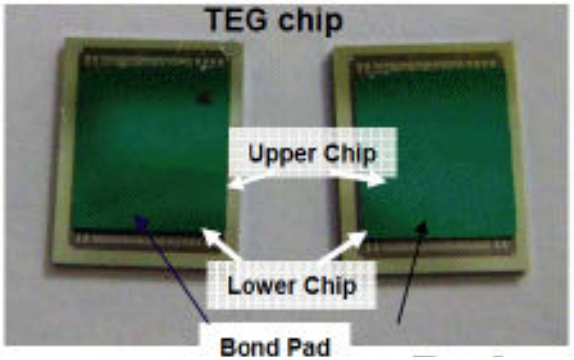
- Process improvement:
  - High radiation tolerance, high resistively wafer, deeper depletion layer, wafer thining,…
- Larger sensitive area; stitching,…
- 3D integration

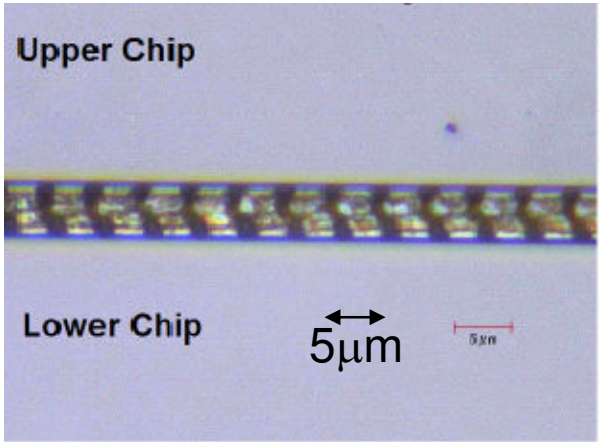


3D Integration with ZyCube μ-bump

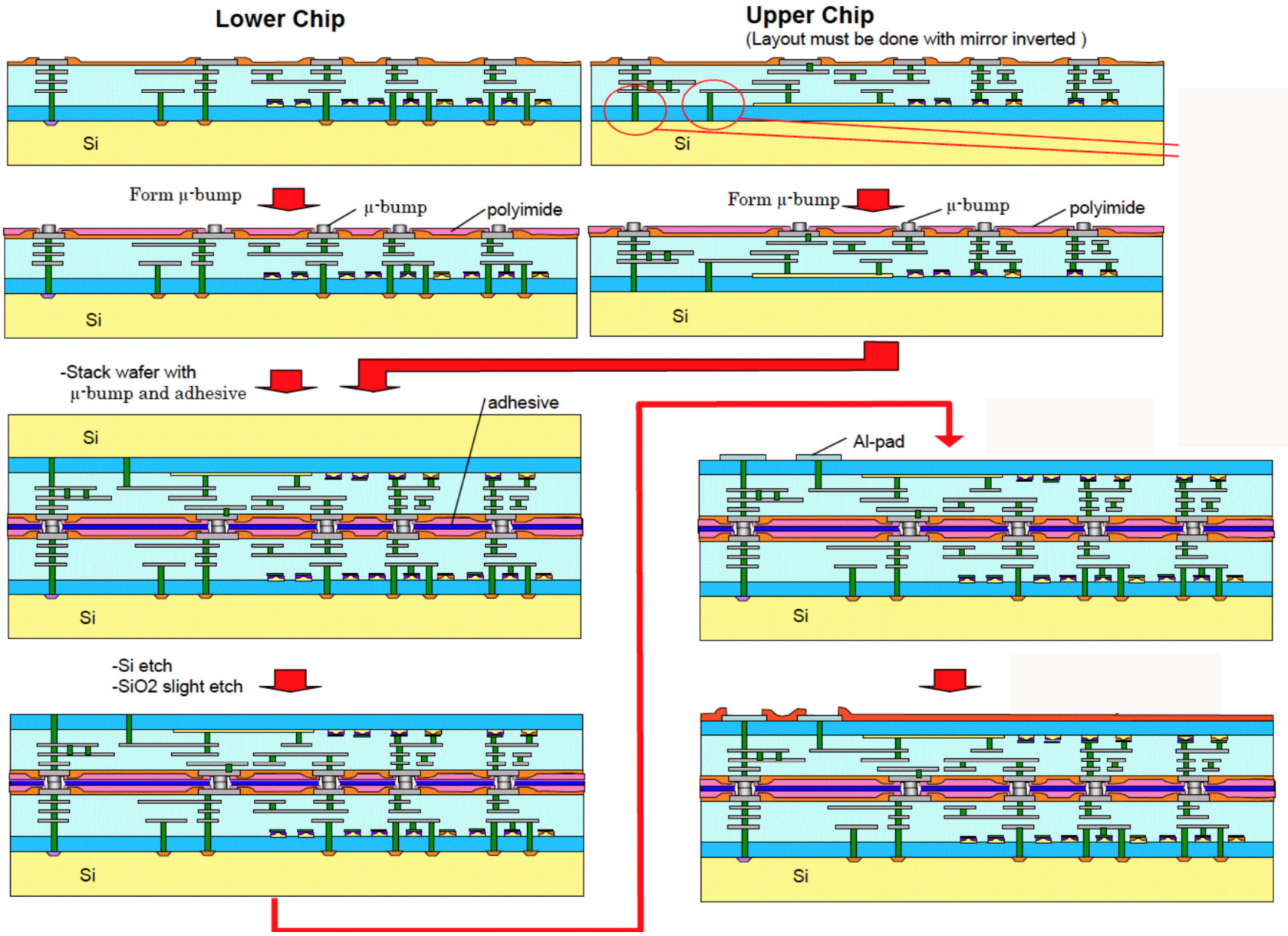
- Use ZyCube Co. Ltd.(Japan) μ-bump bonding (~5μm pitch) technology.
- This enables
  - Dead-Area Free Large pixel detector.
  - ADC integration,…







(1) Stack Process Flow (after finishing wafer process)



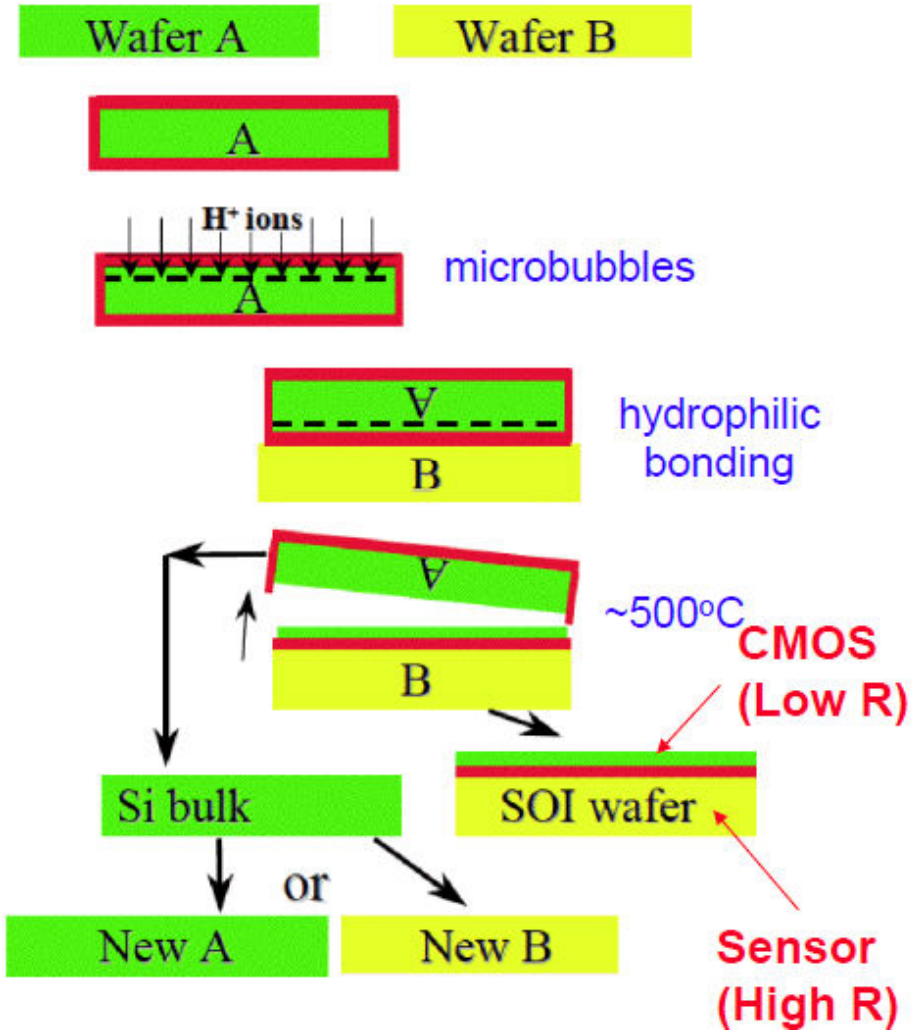
Summary

- The SOI Pixel detector is a unique and attractive monolithic pixel detector. It features such as high speed, low material budget, high resolution,…
- As SOI pixel detector uses commercial mass production process, it has cost benefits and scalability. (Moore's Law)
- We have overcome the back gate effect (electrical field of bias voltage changes transistor's threshold voltage) by Buried p-well (BPW) implantation. Now SOI pixel detector becomes practical detector.
- We have confirmed good sensitivity of the SOI pixel detector to Light, X-rays and charged particles. They functioned well as expected.
- We have done 4 MPW runs. Each run includes 15~25 designs from many institutes.
- In this FY2009, we are scheduling 3 MPW runs.
- Improving SOI process with Oki Semiconductor Co. Ltd. to improve the performance, and trying 3D integration with ZyCube Co. Ltd.
- we would like to contribute to future particle-physics experiments such as SHLC upgrade, ILC or Super B factory

Backup

UNIBOND™ Process (1995, France LETI) -> SOITEC

1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
7. Split-off wafer A is recycled, becoming the new wafer A or B



PD-SOI v.s. FD-SOI

PD-SOI (Partially Depleted)

◆Thick SOI thickness (T_{SOI})
~100-200nm

◆Depletion layer < T_{SOI}

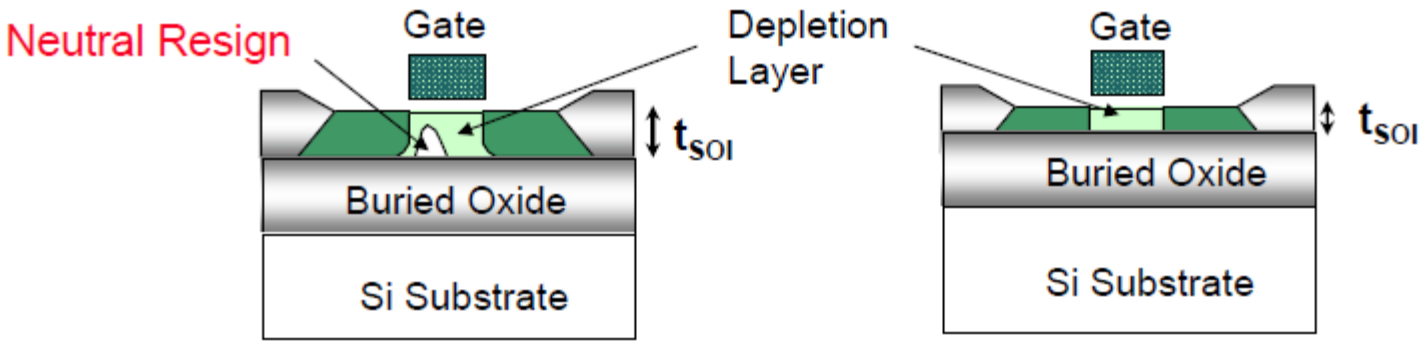
◇Large floating body effect
◇High drive Current by kink effect
→ High speed application

FD-SOI (Fully Depleted)

◆Thin SOI thickness (T_{SOI})
< 50nm

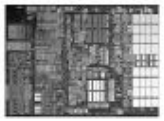
◆ Depletion layer > T_{SOI}

◇Less floating body effect
◇Steep subthreshold slopes
→ Low power application



FD-SOI has advantage in performance under very low voltage operation.

PD-SOI v.s. FD-SOI (2)



◆ PD-SOI (Partially Depleted)
High-speed microprocessors
- IBM: PowerPC , mainframe CPU's, Wii(Nintendo), Xbox
- Free scale: PowerPC
- AMD: Athlon processors
- Sony (with IBM and Toshiba) : Cell, PS3

◆FD-SOI (Fully Depleted)
Low-power application
- Oki: solar cell watch, long-wave RF decoder

Technology Node option beyond 32nm, Next 3D Tr.
- Intel, many major companies

http://www.casio.co.jp

At present, only Oki has an experience of mass production of FD-SOI

CNTPIX3

- 4 kinds of Pixel Block 216 x 72 (15,552) pixels
- 5.0 x 15.4 mm^2 chip size
- 64 x 64 um^2 pixel size
- Enable Tiling