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Low Power SoC Design

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The design of Systems-on-Chip (SoC) in very deep submicron technologies becomes a very complex task that has to bridge very high level system description to low level consideration due to technology defaults and variations. This talk will describe some of these low level main issues, such as dynamic and static power consumption, temperature, technology variations, interconnect, DFM, reliability and yield, and their impact on high-level design, such as the design of multi-Vdd, fault-tolerant, redundant or adaptive chip architectures. Low power SoC designed by CSEM will be presented for applications in three domains: wireless sensor networks, vision sensors and mobile TV.

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