(Low-Power)
Analog Design
in Scaled Technologies

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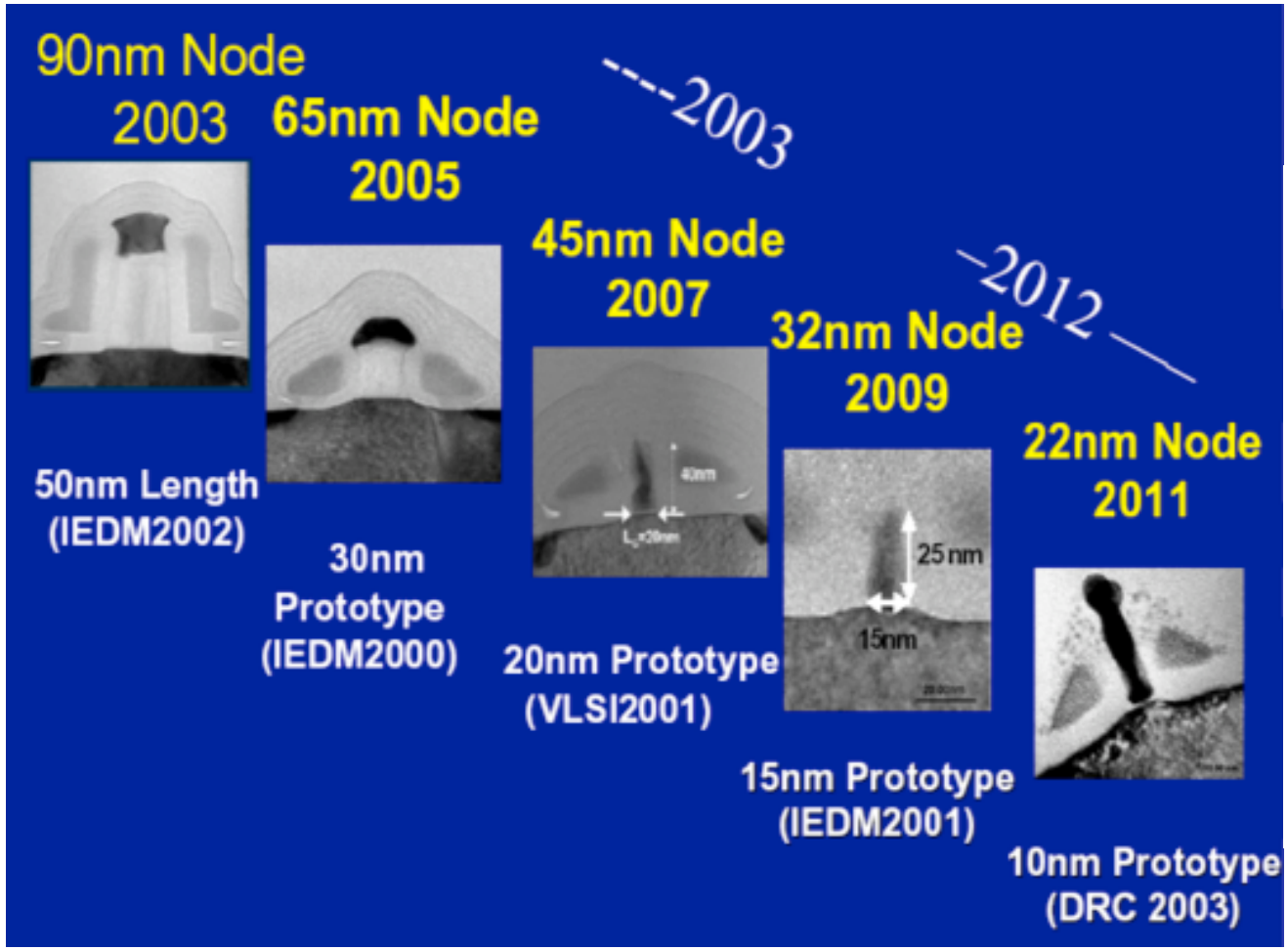
Analog Design in ScalTech

Outline

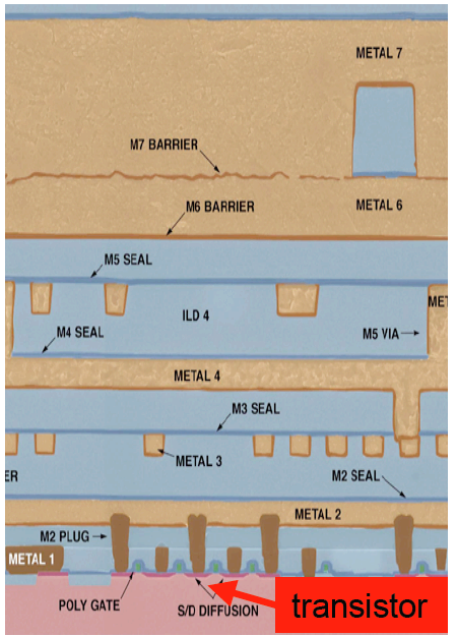
- CMOS technology scaling trends
  - Power reduction
  - $\{V_{DD}-V_{TH}\}$ reduction
  - Gain reduction
  - V_{TH} variation
- **ScalTech** Analog design
  - **ScalTech** at transistor level
    - Transistor in subthreshold
  - **ScalTech** at circuit level
    - Analog switch
    - Opamp design
    - Basic bandgap design
  - **ScalTech** at system level
    - Analog filter
    - ADC

CMOS Technology scaling

Minimum gate size reduction



Metal 7
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1



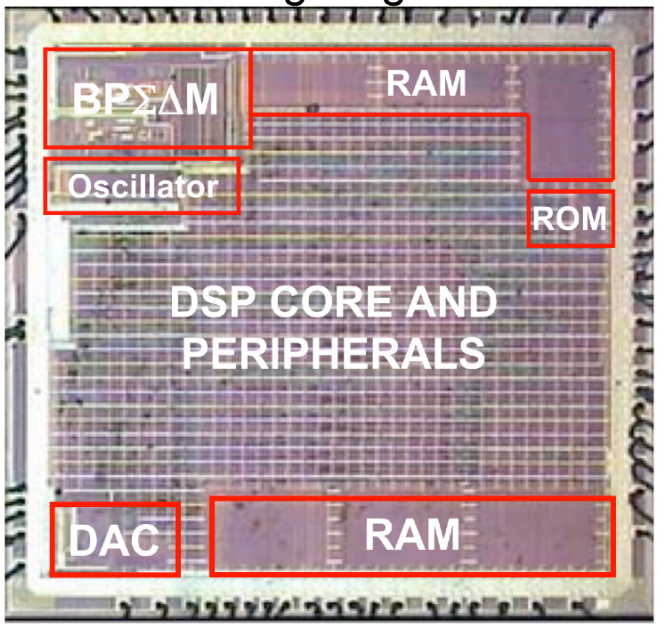
Silicon wafer

ScalTech ➔ LV & LP

- For CMOS SoC's
  - the larger digital part forces the use of the ScalTech
    - ➔ increased number of digital function for the same die area
    - reduced digital part power consumption
  - Example: FM receiver (JSSC2004)

BiCMOS Fully Analog Solution

CMOS Analog&Digital Solution



ScalTech ➔ LV & LP

Low-Voltage vs. Low-Power

- In **digital circuits**, reducing V_{DD} ➔ power reduction:

$$P_{dig} \approx f \cdot C \cdot V_{DD}^2$$

- In **analog circuits**, with ***thermal noise limitation***
- Maximum output swing: ..... SW = $[V_{DD} - 2 \cdot V_{sat}]$
- The analog power consumption ..... $P_{an} = \beta \cdot I \cdot V_{DD}$ ..... $I = P_{an}/(\beta \cdot V_{DD})$
- The thermal noise is *kT/C*-limited & ≈1/I: ..... $N = \alpha/I$

$$DR = \frac{[V_{DD} - 2 \cdot V_{sat}]^2}{\alpha / I} = [V_{DD} - 2 \cdot V_{sat}]^2 \frac{P_{an}}{\alpha \cdot \beta \cdot V_{DD}}$$

- For a given DR

$$P_{an} = \frac{DR \cdot \alpha \cdot \beta \cdot V_{DD}}{[V_{DD} - 2 \cdot V_{sat}]^2} \propto \frac{DR}{V_{DD}}$$

  - ➔ P_{an} increases for V_{DD} decreasing

CMOS Technology scaling

Parameter of the digital NFET in IBM CMOS *

Node	Nm	250	180	130	90	65	⇓
L_{GATE}	Nm	180	130	92	63	43	
t_{OX}(inv.)	Nm	6.2	4.45	3.12	2.2	1.8	⇓
Peak g_m	µS/µm	335	500	720	1060	1400	⇑
g_{ds}**	µS/µm	22	40	65	100	230	⇑⇑
g_m/g_{ds}	-	15.2	12.5	11.1	10.6	6.1	⇓
V_{DD}	V	2.5	1.8	1.5	1.2	1	⇓⇓
V_{TH}	V	0.44	0.43	0.34	0.36	0.24	⇓
f_T	GHz	35	53	94	140	210*	⇑⇑

1

2

3

- The above trends affects:
  - Analog block **functionality**
  - Analog block **performance**

- * projected
- ** at peak g_m

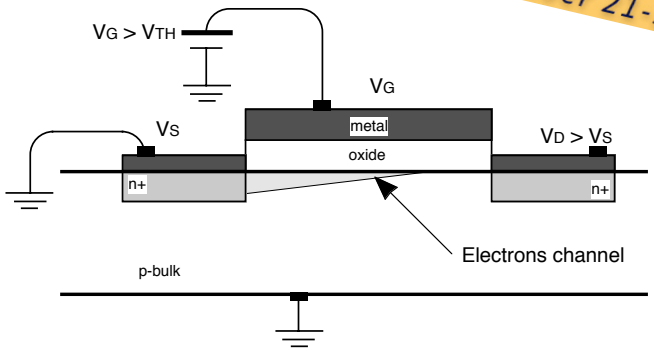
* Pekarik@CICC2004

CMOS Technology scaling

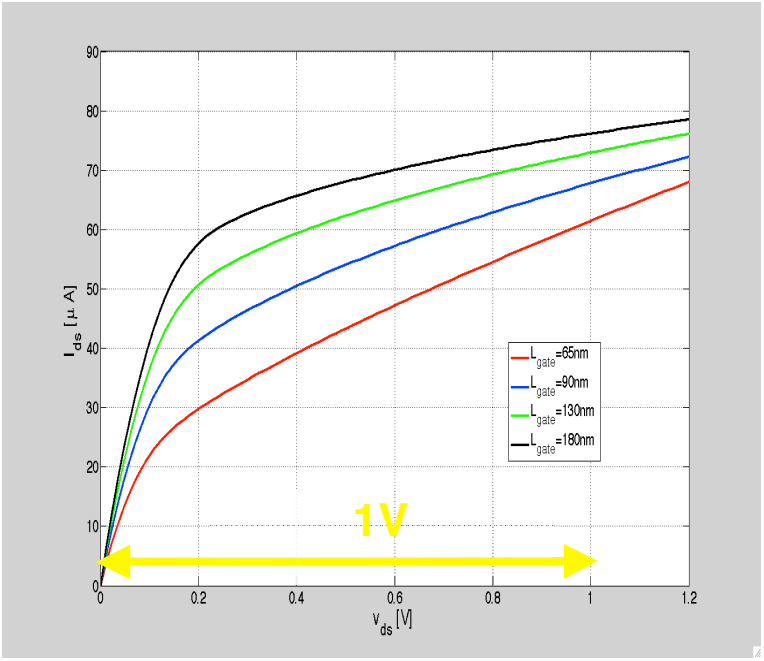
MOS in Saturation region

$$I_D = \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2$$

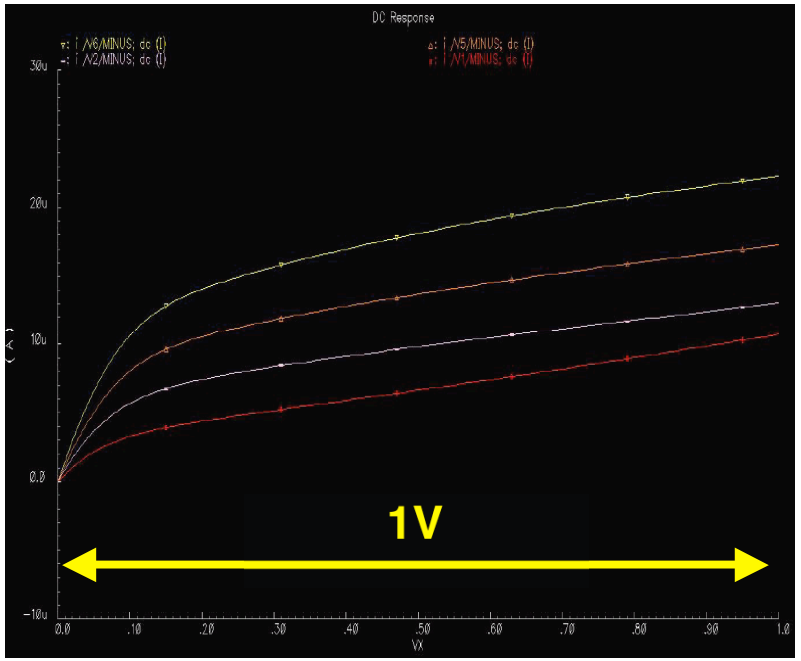
- $V_{GS} > V_{TH}$
  - V_{DD} is decreasing slower than V_{TH}
    - V_{GS} is approaching V_{DD}
- Output impedance is decreasing



65nm

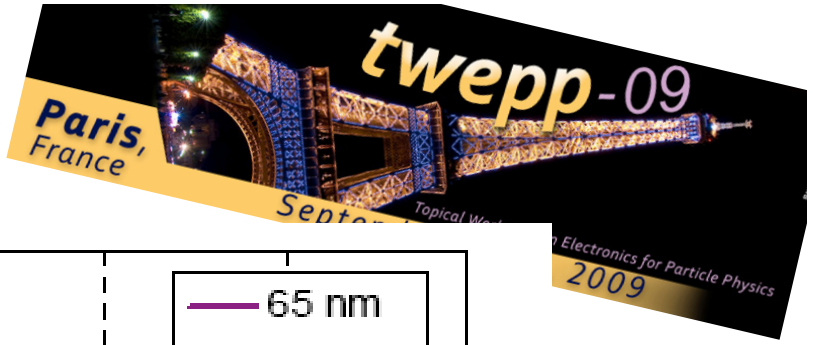


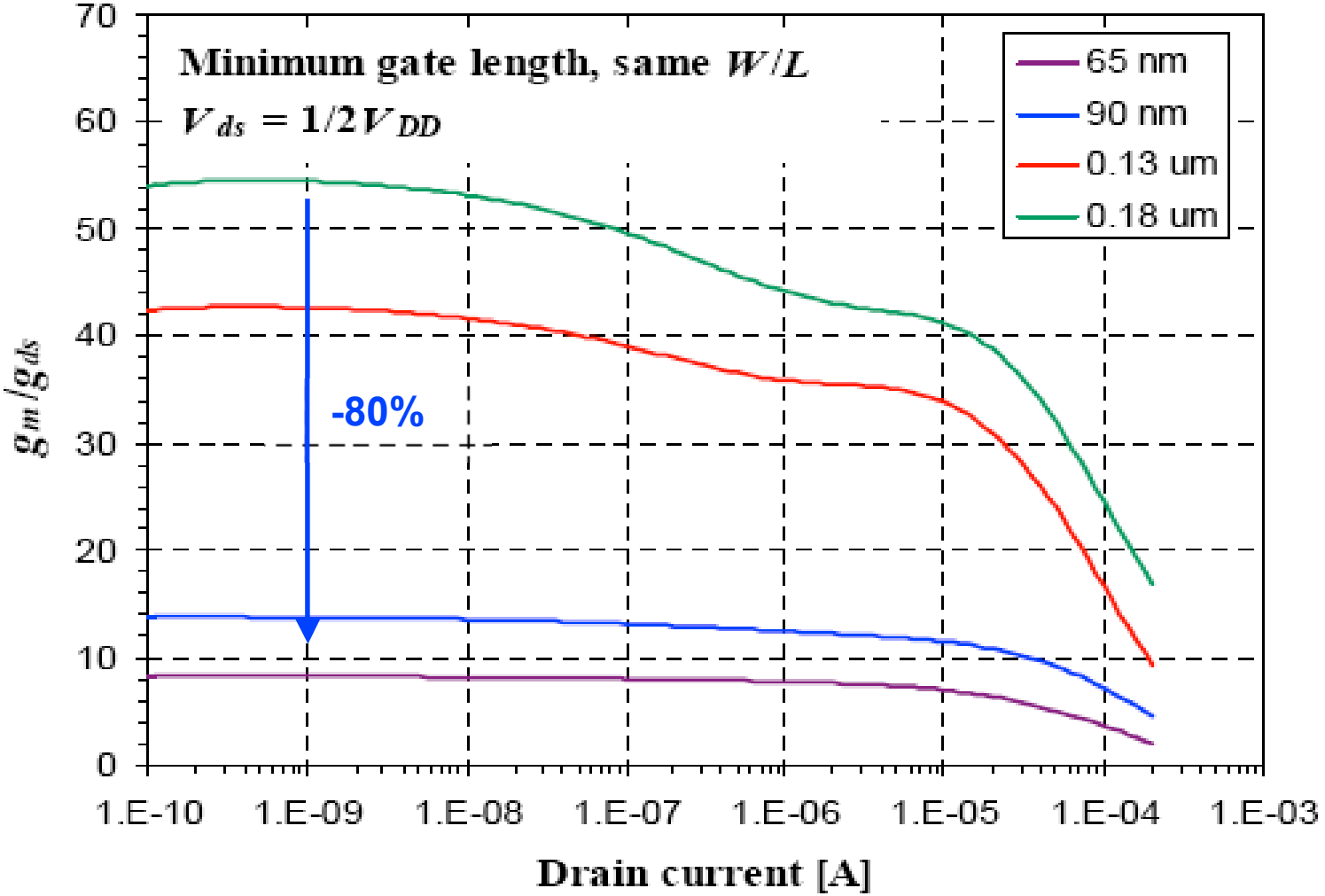
45nm



CMOS Technology Scaling

Intrinsic gain reduction *





* Trond Ytterdal "Analog Circuit Design in Nanoscale CMOS Technologies", 2006

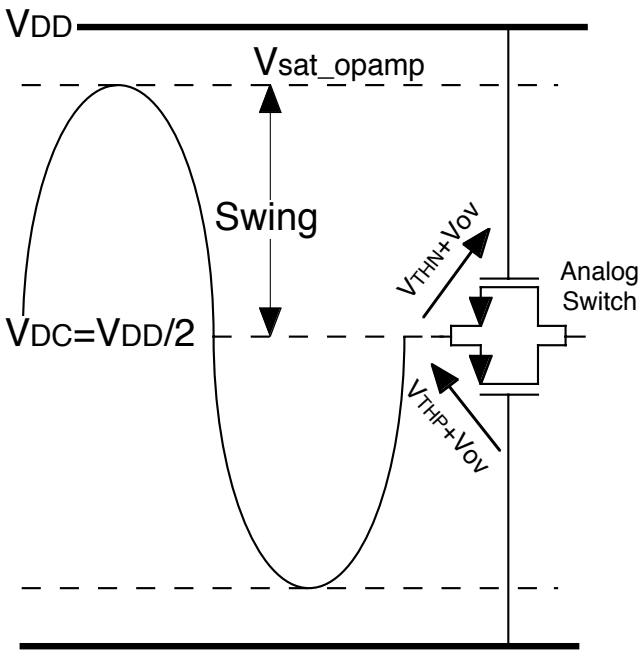
CMOS Technology scaling

$\{V_{DD} - V_{TH}\}$ Reduction: Switch functionality

- The passgate operation
  - ➔ V_{DDmin_STD}
- Problems at $V_{DD}/2$

$$V_{DDmin\_STD} > V_{THN}(V_{DD}/2) + V_{ov} + V_{THP}(V_{DD}/2) + V_{ov}$$

$$V_{DDmin\_STD} > 2 \cdot V_{TH} + 2 \cdot V_{ov}$$



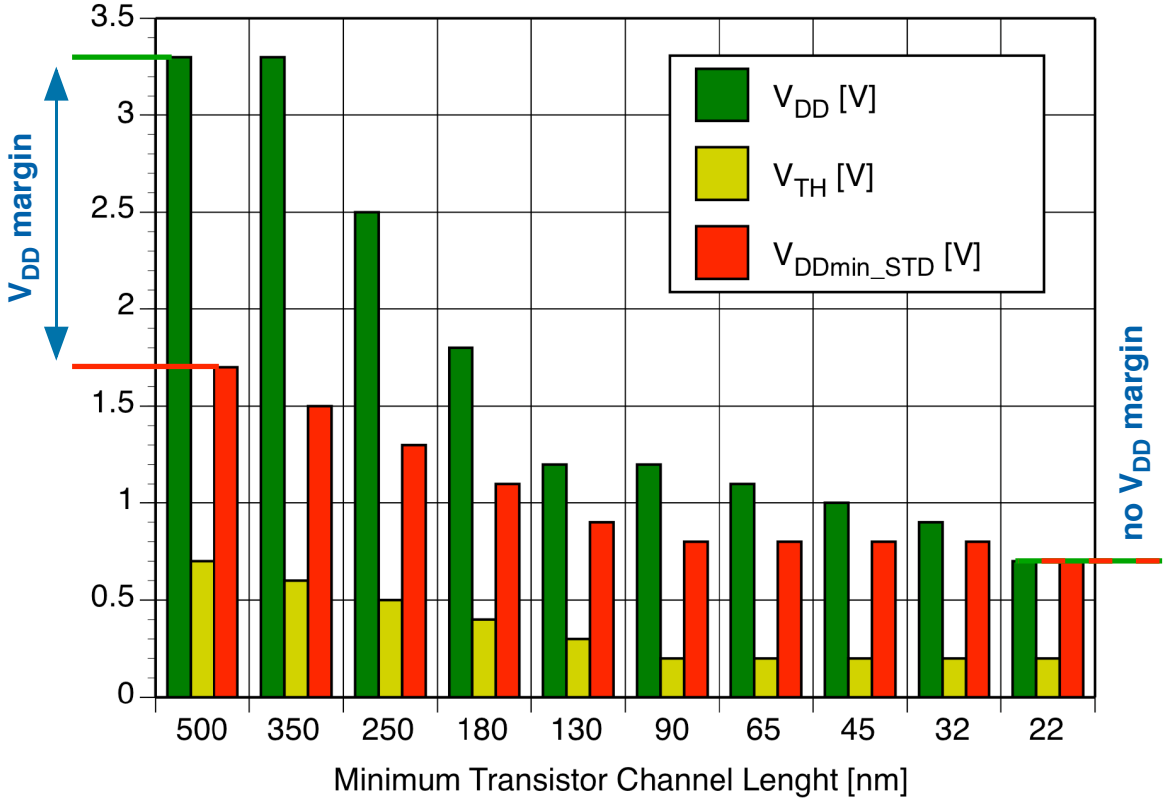
  - ➔ V_{DDmin_STD} is technology dependent

CMOS Technology scaling

$\{V_{DD} - V_{TH}\}$ Reduction: Switch functionality

$$V_{DDmin\_STD} > 2 \cdot V_{TH} + 2 \cdot V_{ov}$$

- The reduced distance $\{V_{DD} - V_{TH}\}$ has impact on analog blocks
  - ➔ Lower overdrive ($V_{GS} - V_{TH}$)
  - ➔ Lower linearity
    - ➔ **Performance loss**
  - ➔ Lower linearity
    - ➔ **Critical Functionality**
    - Analog switch will be possible until 22nm node



CMOS Technology scaling

V_{TH} deviations

- In **ScalTech** V_{TH} strongly changes
  - Statistical variation
    - Technology & Temperature spread
      - Design
    - Mismatch
      - Design & Layout
  - Systematic variation
    - Short & Narrow channel effects (W&L effects)
      - ➔ Design
    - Shallow Trench Insulator (STI) effects
      - ➔ Layout

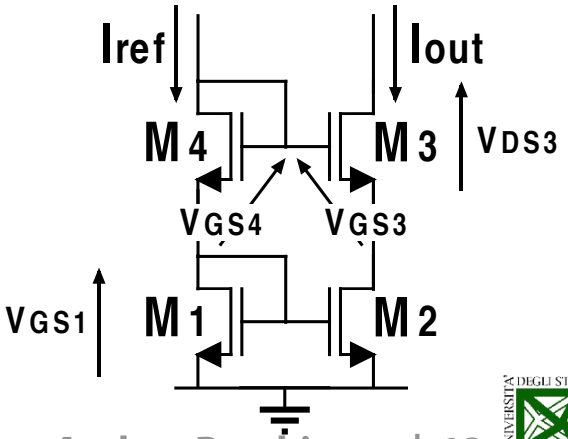
CMOS Technology scaling

MOS in Saturation region

- Technological Parameter Variation
  - 65nm CMOS Technology
  - W = 650nm L=65nm
  - V_{GS}=730mV; V_{DS}=1.2V

	Nominal			*Fast*			*Slow*		
	-40°C	*27°C*	*120°C*	*-40°C*	*27°C*	*120°C*	*-40°C*	*27°C*	*120°C*
V_{TH} *[mV]*	*584*	*547*	*496*	*510*	*475*	*425*	*646*	*606*	*552*
g_{ds} *[µA/V]*	*34.4*	*34.1*	*34.1*	*50.9*	*49.2*	*47.4*	*19.6*	*21.0*	*22.5*
g_m *[µA/V]*	*548*	*486*	*432*	*667*	*583*	*505*	*392*	*370*	*348*
g_m/g_{ds}	*15.9*	*14.3*	*12.7*	*13.1*	*11.8*	*10.6*	*20*	*17.6*	*15.5*

- A cascode current mirror requires for the two cascode diodes
  - ➔ $(2 \cdot V_{GS}) > (2 \cdot V_{TH}) \geq (1.2V)$ in the worst case
    - ➔ No cascode current mirror in a safe design



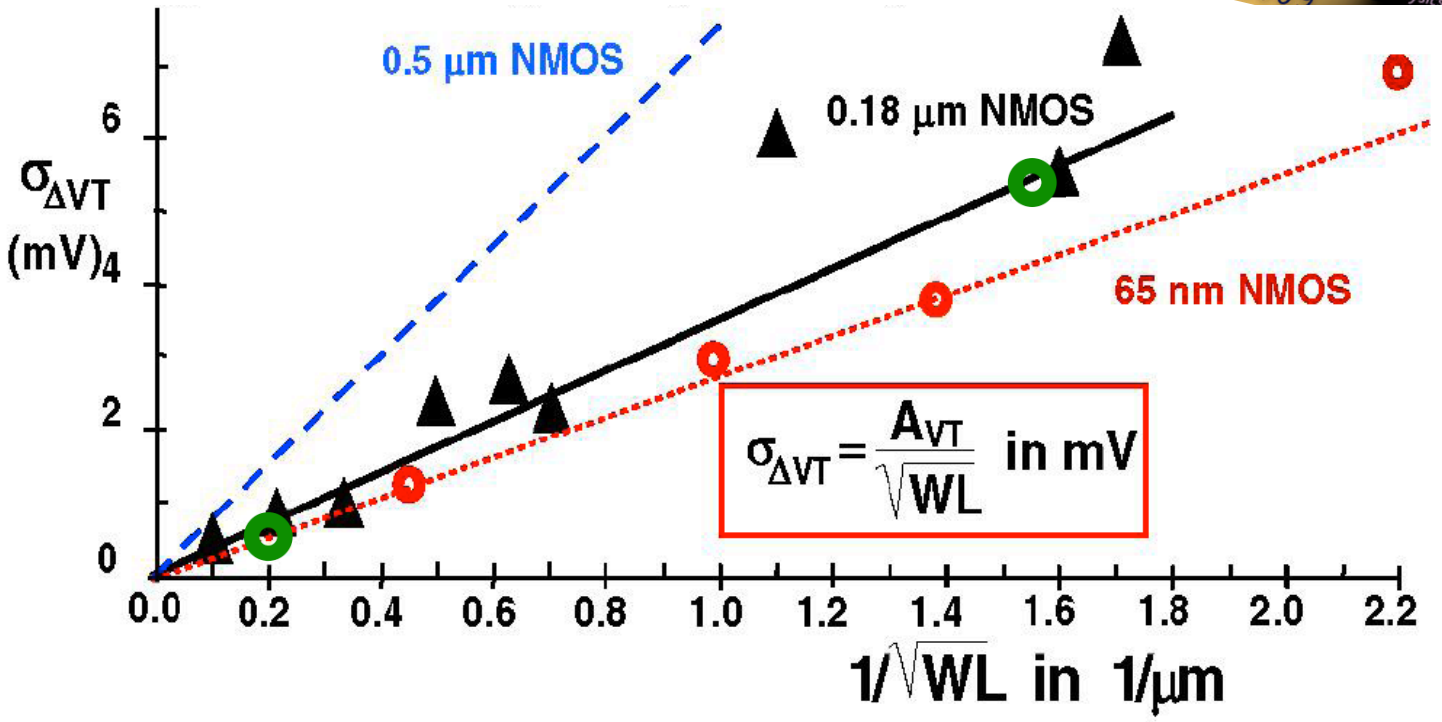
CMOS Technology scaling

V_{TH} Mismatch

$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{W \cdot L}}$$

$$A_{VT} = \gamma \cdot T_{ox}$$

- "1mV·µm x nm T_{ox}"
- **For a given (W·L)**
  - ➔ **ScalTech** give better matching



- **For a given (W/L)**

$$(W \cdot L)_{180nm} \approx 0.13 \cdot (W \cdot L)_{65nm} \quad \rightarrow \quad \frac{1}{\left(\sqrt{W \cdot L}\right)_{180nm}} = \frac{7.6}{\left(\sqrt{W \cdot L}\right)_{65nm}}$$

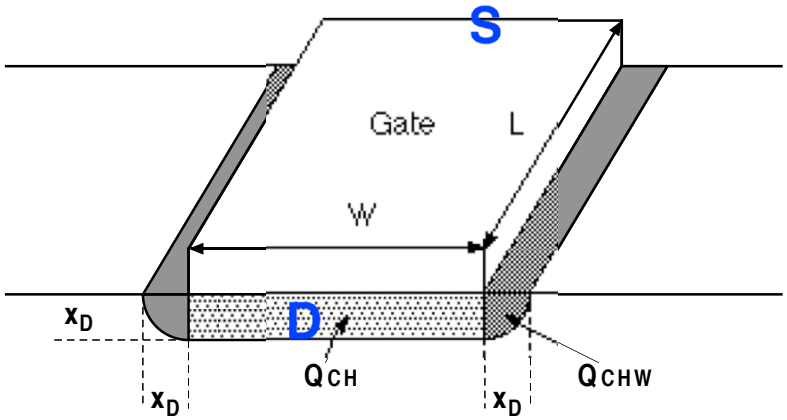
  - ➔ **ScalTech** give better matching

- **ScalTech *matched-limited*** circuits (ADC) requires lower power

CMOS Technology scaling

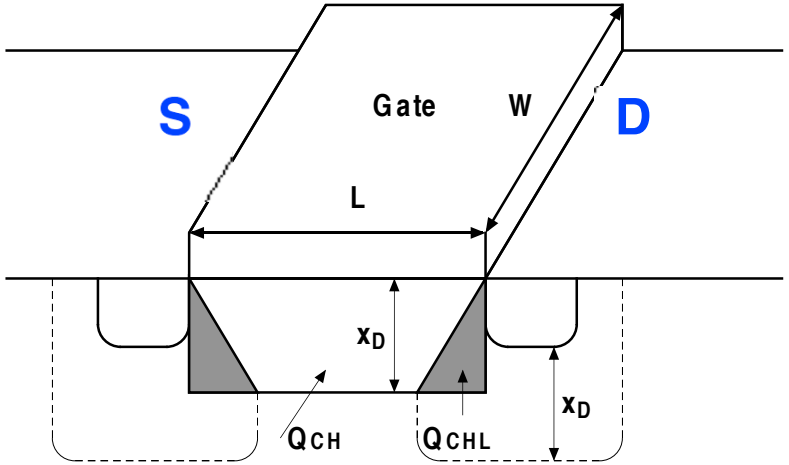
V_{TH} Variation – Narrow & Short Channel Effects

- The depletion layer is not limited to the charge in the area under the gate (Q_{CH})



- For **large W**, Q_{CHW} is negligible
- For **narrow W**, Q_{CHW} becomes important !!!
  - ➔ V_{TH} increases

- The depletion layer under the gate includes all the charge from S to D
- At S&D, part of the charge (Q_{CHL}) is not directly controlled by G but it depends on S&D



- For **short L**, Q_{CHL} has not to be included in the calculation of V_T
  - ➔ V_{TH} reduces

CMOS Technology scaling

V_{TH} Variation - Velocity saturation

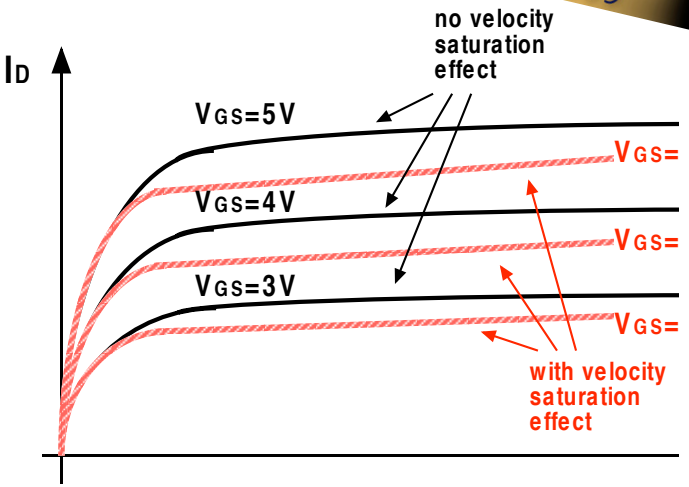
- For **low** electric field (ε)
  - the velocity increases proportionally

$$\mu_o = \frac{v_{sat}}{\varepsilon_{crit}}$$

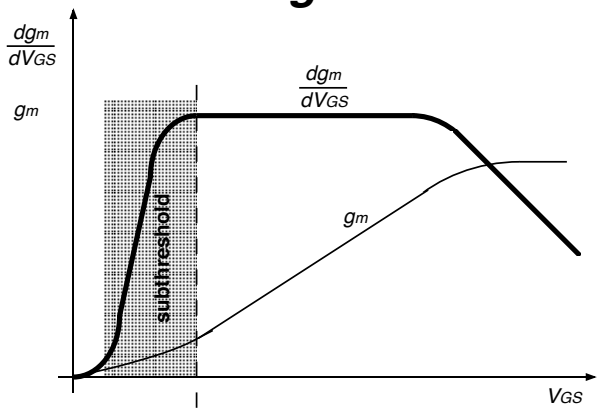
- For **large** electric field (i.e. **Small L**)
  - the velocity saturates to v_{sat} ($\approx 10^5$ m/s)

$$I_D = W \cdot Q_m \cdot v_{sat} = W \cdot C_{ox} \cdot (V_{GS} - V_{TH}) \cdot v_{sat}$$

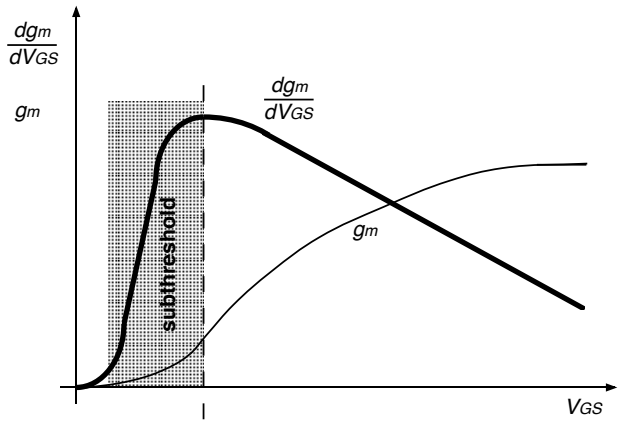
$$g_m = \frac{\partial I_D}{\partial (V_{GS} - V_{TH})} \cong W \cdot C_{ox} \cdot v_{sat}$$



Large L



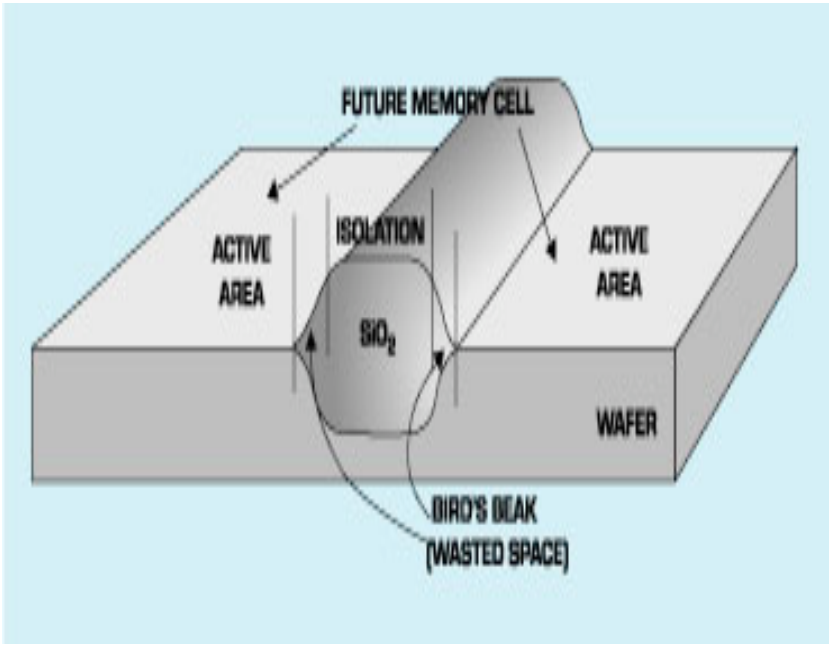
Small L



CMOS Technology scaling

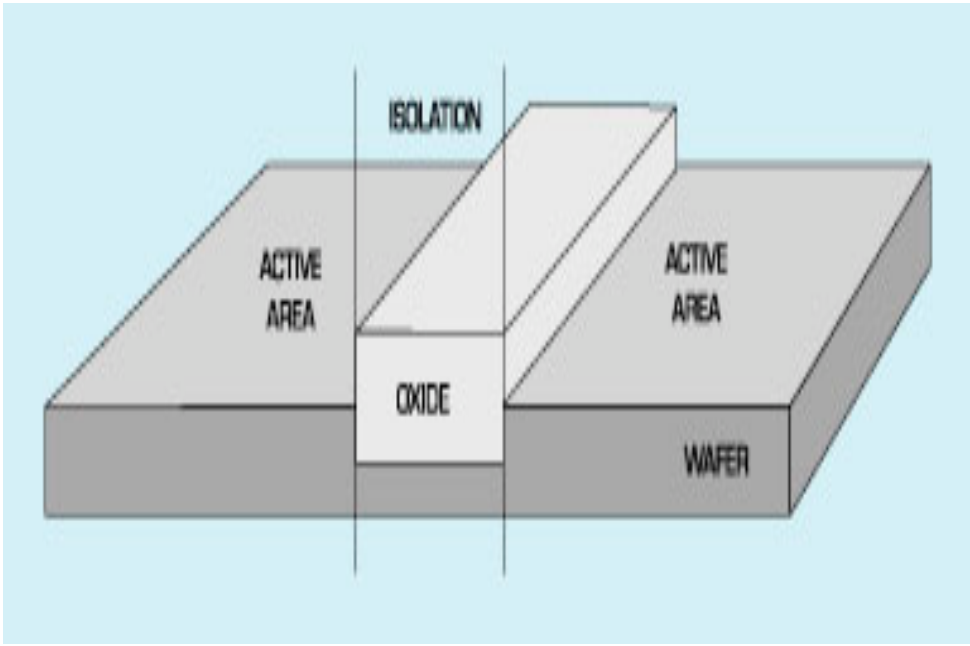
Shallow Trench Isolation (STI)

- STI electronically isolates microstructures in semiconductors devices
  - STI is smaller than LOCOS ➔ STI replaces LOCOS
    - ➔ structure density can be maximized



Isolation using LOCOS process

The "bird's beak" regions are wasted space



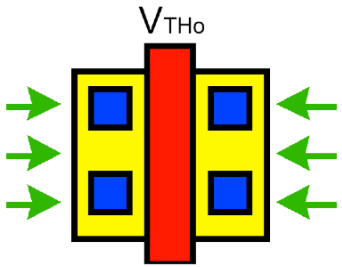
Isolation using STI process

The raised oxide profile will subsequently be nearly flattened by CMP

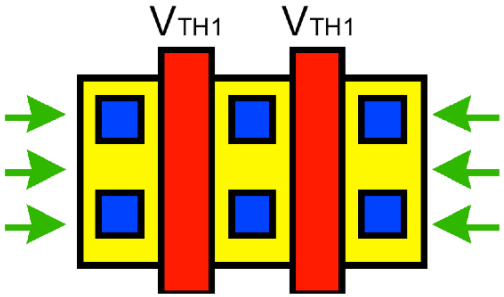
CMOS Technology scaling

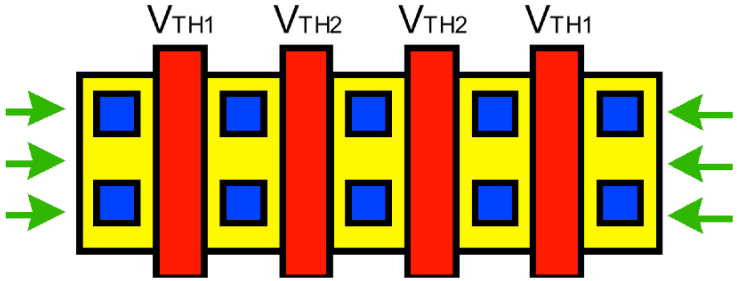
Shallow Trench Isolation (STI) - Simulation issues

- Technology models are extracted from the unitary transistor
- Both sides are affected by STI



- Stacked transistors may have different V_{TH}





- "Internal" devices do not see STI and are ***well matched*** (same V_{TH2})
  - Good for current mirrors (current steering DAC)
- BUT they are not modeled (post-layout in some Design Kits)
  - ➔ For matched devices (current mirror, etc..) use external dummy (shield) devices
    - Matched but Unknown V_{TH} before layout

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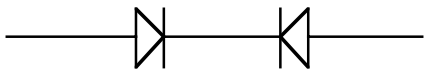
CMOS Technology scaling

MOS in Subthreshold

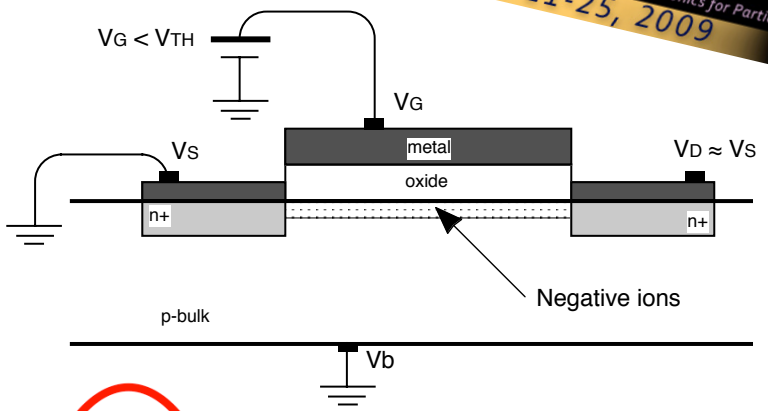
$V_{GS} \approx\!< V_{TH}$

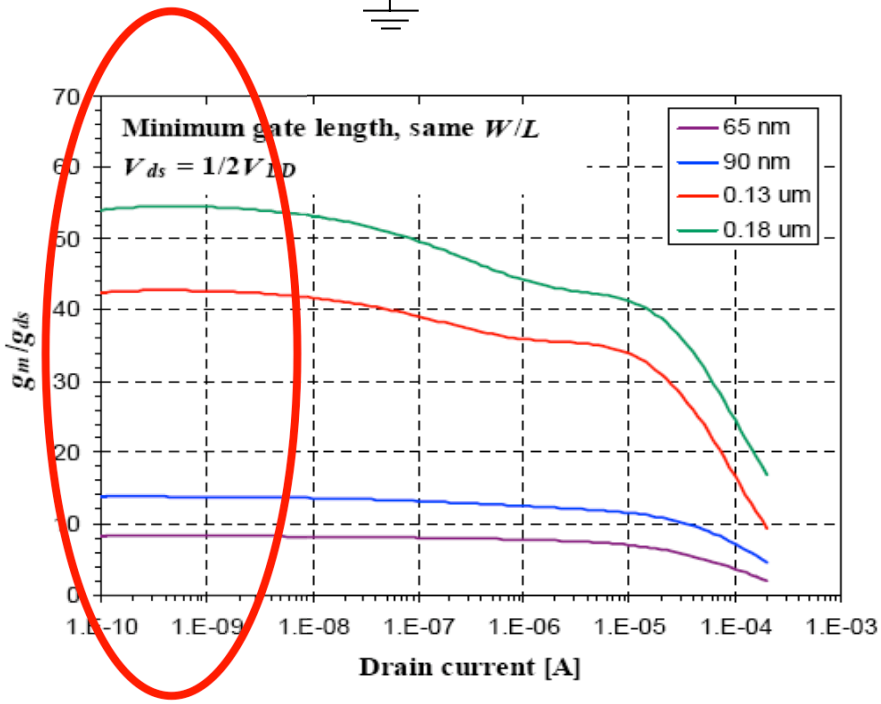
- The structure is equivalent to



$$I_D = I_{Do} \cdot e^{q \cdot V_{GS} / n \cdot k \cdot T} \cdot e^{-q \cdot V_{BS} / n \cdot k \cdot T} \cdot \left[1 - e^{-q \cdot V_{BS} / k \cdot T}\right]$$

  - ☺ Minimum V_{OV}
  - ☺ Small gate capacitance
  - ☺ Large g_m/I_D ratio
  - ☺ Large voltage gain
    - ☹ Large drain current mismatch
      - ➔ (input offset)
    - ☹ Large output noise current for a given I_D
    - ☹ Low speed, $f_T \cong \dfrac{\mu \cdot V_T}{2 \cdot \pi \cdot L^2}$





CMOS Technology scaling

MOS in Subthreshold

- Diode connected transistor
  - I_D = 60µA & L = 200nm

W [µm]	V_{TH} [mV]	V_{GS} [mV]	g_m [mA/V]	g_{ds} [µA/V]	r_{ds} [kΩ]	A_o
5	506	556	0,75	27,1	36,9	27,68
10	506	509	0,896	32,5	30,8	27,57
30	506	446	1,12	40,8	24,5	27,45
50	506	421	1,21	44,2	22,6	27,38
70	506	406	1,27	46,2	21,6	27,49
90	506	395	1,31	47,6	21,0	27,52
120	506	382	1,35	49	20,4	27,55
150	506	373	1,39	50	20,0	27,80

- For a given current
  - Larger is V_{GS} (closer to V_{TH}) ➔ ➔ Smaller is W
    - Lower is g_m
    - Larger is g_{ds}
      - The gain is constant
  - ➔ For input stage a large device with low V_{GS} is OK ==> Large g_m
  - ➔ For output stage a small device with large V_{GS} is OK ==> Low g_{ds}

CMOS Technology scaling

V_{TH} Mismatch: Strong Inv. Vs. Weak Inv. *

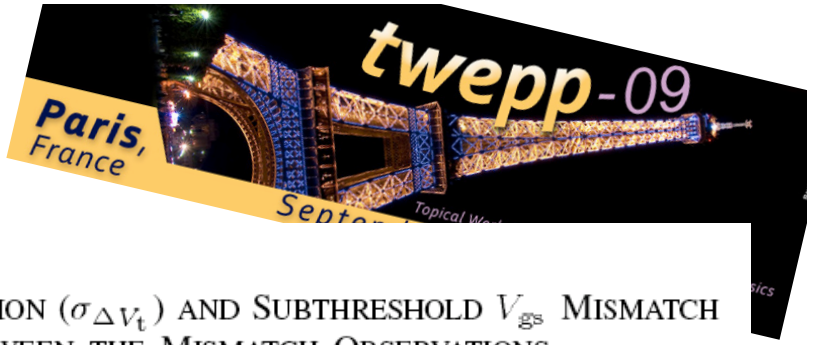


TABLE II
THRESHOLD VOLTAGE MISMATCH STANDARD DEVIATIONS IN STRONG INVERSION ($\sigma_{\Delta V_t}$) AND SUBTHRESHOLD V_{gs} MISMATCH ($\sigma_{\Delta V_{gs}}$ at $I_d = 10$ pA/(W/L)) AND THE CORRELATIONS BETWEEN THE MISMATCH OBSERVATIONS FOR A RANGE OF TRANSISTOR DIMENSIONS

drawn_W (μm)	drawn_L (μm)	$\sigma_{\Delta Vt}$ (strong inversion) (mV)	$\sigma_{\Delta Vgs}$@[Id=10pA/(W/L)] (mV)	Correlation factor R^2
10	4	0.7	2.1	0.07
2	10	1.1	3.0	0.05
10	1	1.7	4.5	0.03
0.4	10	2.5	5.1	0.24
2	1	5.4	10	
0.32	4	4.0	6.6	
2	0.2	12	27	
0.4	1	8.9	12	
0.4	0.24	23	38	
0.32	0.2	27	44	

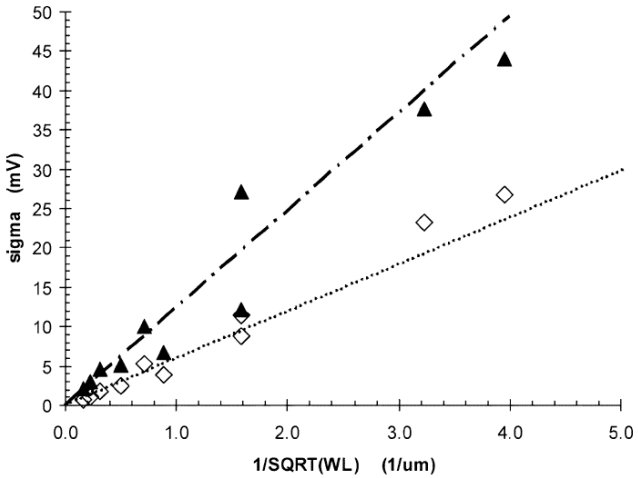


Fig. 12. Mismatch area scaling graph. Diamonds: strong inversion (linear region) V_t mismatch. Triangles: subthreshold V_{gs} mismatch (at 10 pA/square). The 6 mVμm and 12.5 mVμm lines are estimates for the corresponding area scaling factors for the strong and weak inversion mismatch standard deviations, respectively.

* Pineda de Gyvez, Tuinhout, "Threshold Voltage Mismatch and Intra-Die LeakageCurrent in Digital CMOS Circuits", IEEE JSSC Jan. 2004

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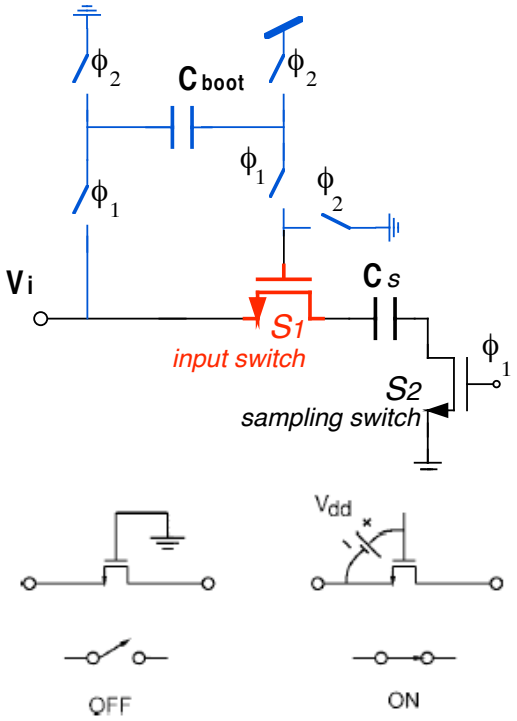
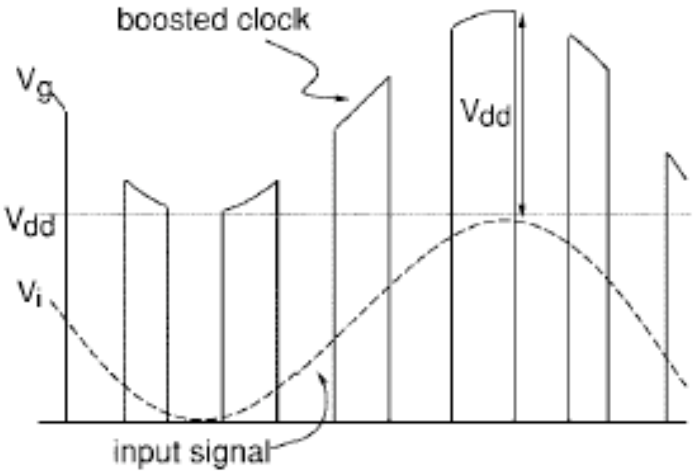
ScalTech Analog Switch

Bootstrap switch

- A charge pump enable switch operation
  - The switch operates with a fixed $V_{OV}=V_{DD}$
    - ➔ the R_{on} is constant for all the swing
  - The gate voltage can go higher than the supply



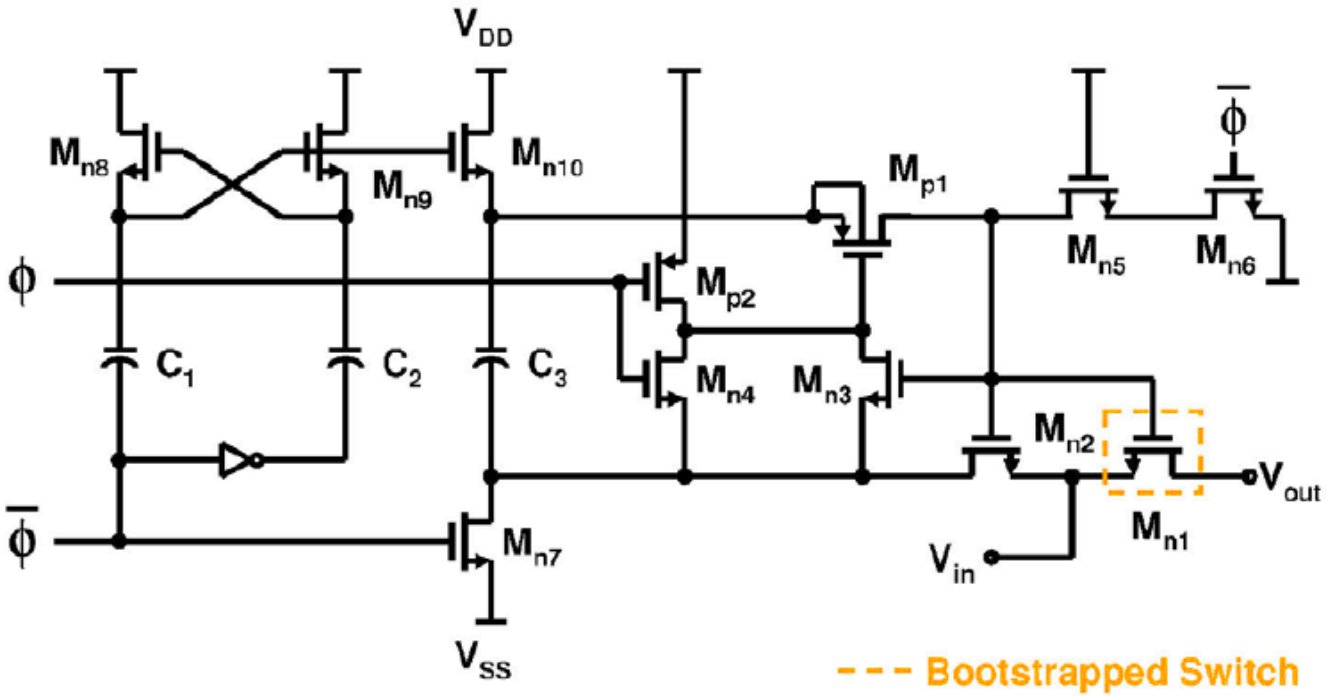


OFF: Grounded gate ensures OFF state
ON: V_{GS} fived to V_{DD} ensures ON state without overdriving gate

ScalTech Analog Switches

On-chip clock multiplication *

- Boosted switch complexity



- Additional load for the previous stage
- A charge-pump for each switch increases area, power consumption and noise injection

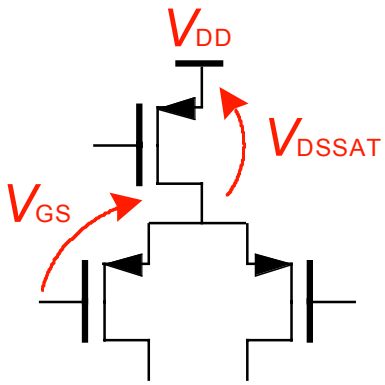
* A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipelined Analogto-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 34, pp. 599-606, May1999.

ScalTech Opamp

General issue

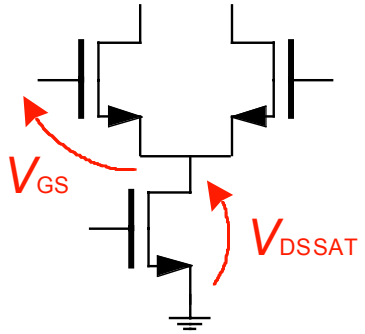
- It is key to get the maximum output swing available
  - => Rail-to-Rail output swing is mandatory

$$V_{out\_DC} = V_{DD}/2$$



- For supply minimization & optimum switch operation
  V_{in_DC} close to ground or V_{DD}

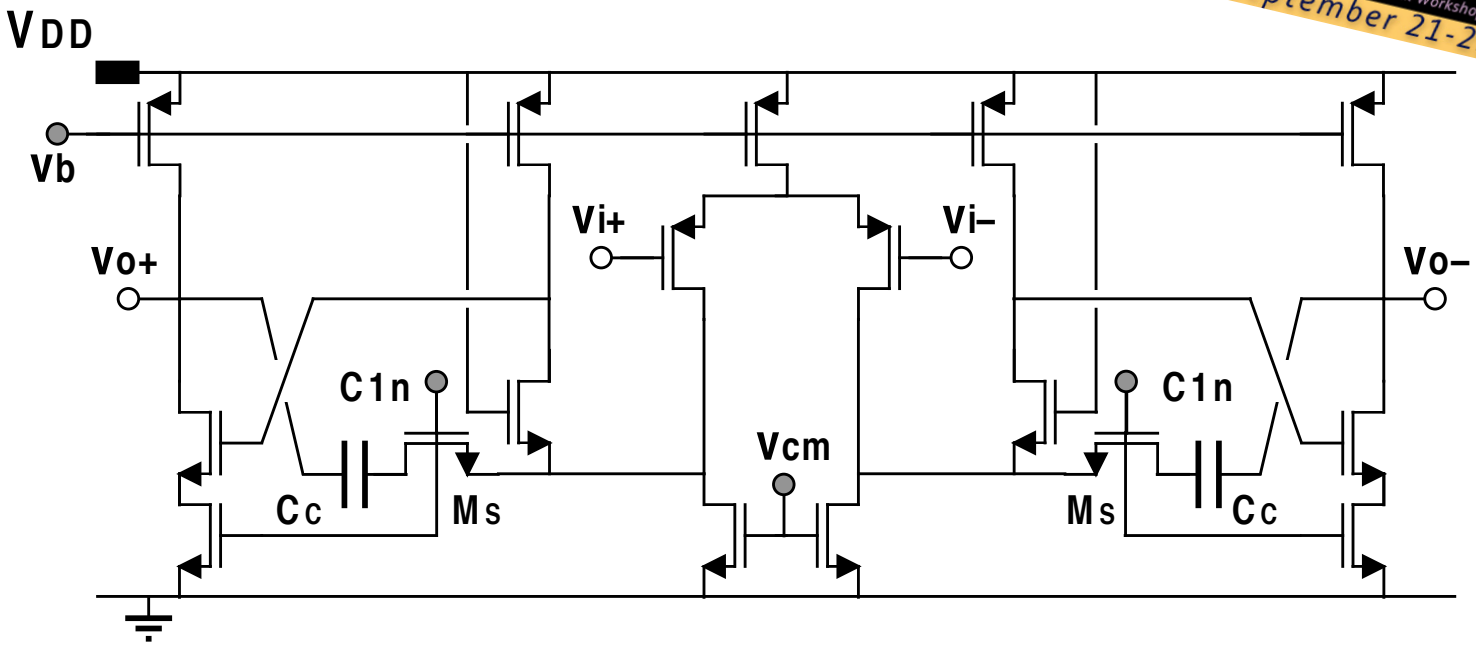
- It is not possible to stack many devices between rails
  - ➔ no cascode



- To get sufficient gain multistage structures are used
  - ➔ for stability reason, bandwidth is limited

ScalTech LV Opamp

Two-stage Miller-compensated Structure *



- Optimum bias for V_{in_DC}=0

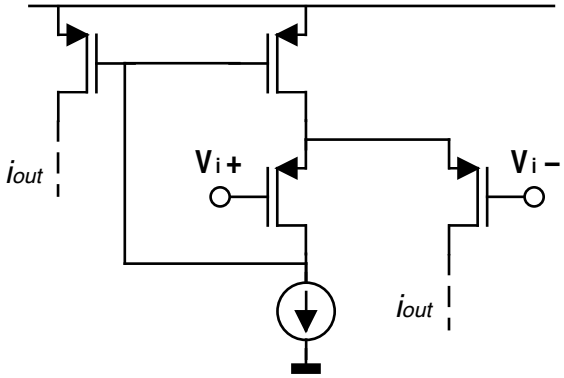
$$V_{DDmin} = V_{TH} + 2 \cdot V_{ov}$$

- A low-voltage CMFB is needed
- Low Gain = $(g_m \cdot r_o)^2 \approx$ 40dB - 45dB

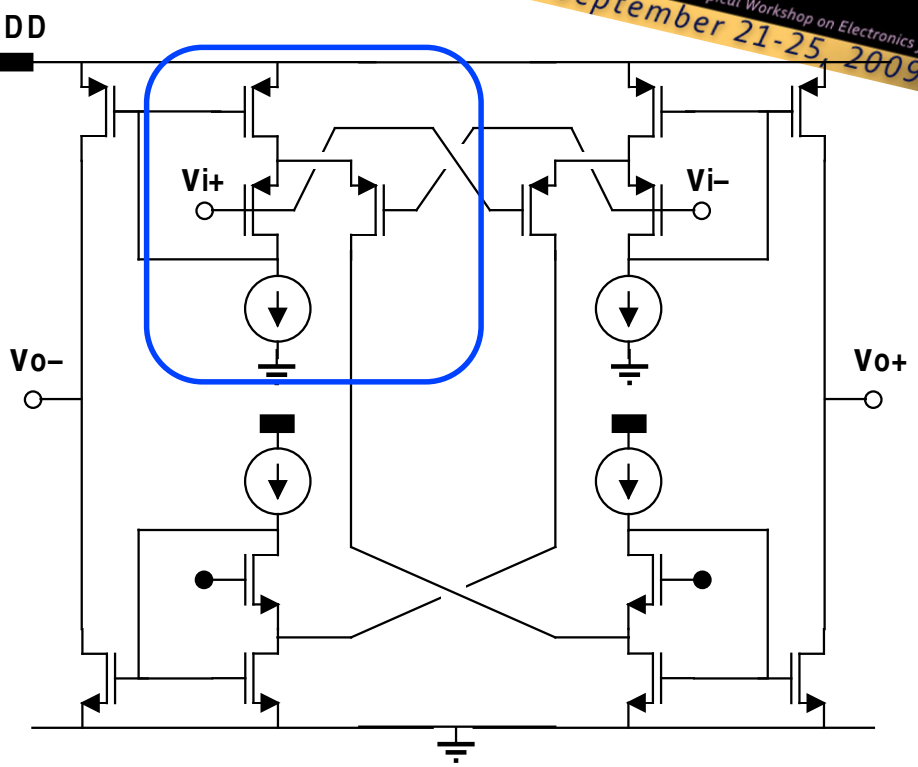
* R. Castello, F. Montecchi, F. Rezzi, and A. Baschirotto, "Low-voltage analog filter", IEEE Transaction on Circuits and Systems - II - Nov. 1995 - pp. 827-840

ScalTech LV Opamp

Class-AB input pair *



Input differential pair



complete AB opamp

$V_{DDmin} = V_{TH} + 2 \cdot V_{ov}$

- Low Gain = $(g_m \cdot r_o) \approx$ 20dB - 25dB

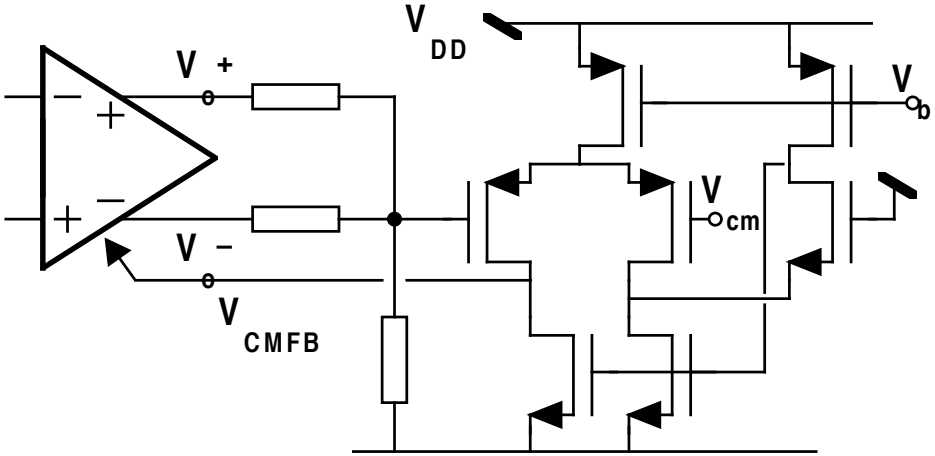
* V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, W. Sansen, "A 900mV 40μW Switched Opamp $\Delta\Sigma$ Modulator with 77dB Dynamic Range", ISSCC '98

ScalTech Opamp

Common-Mode Feedback

- The CMFB inputs are connected to the opamp output nodes @ ≈ $V_{DD}/2$
  - For LV, $V_{DD}/2 < V_{TH}$

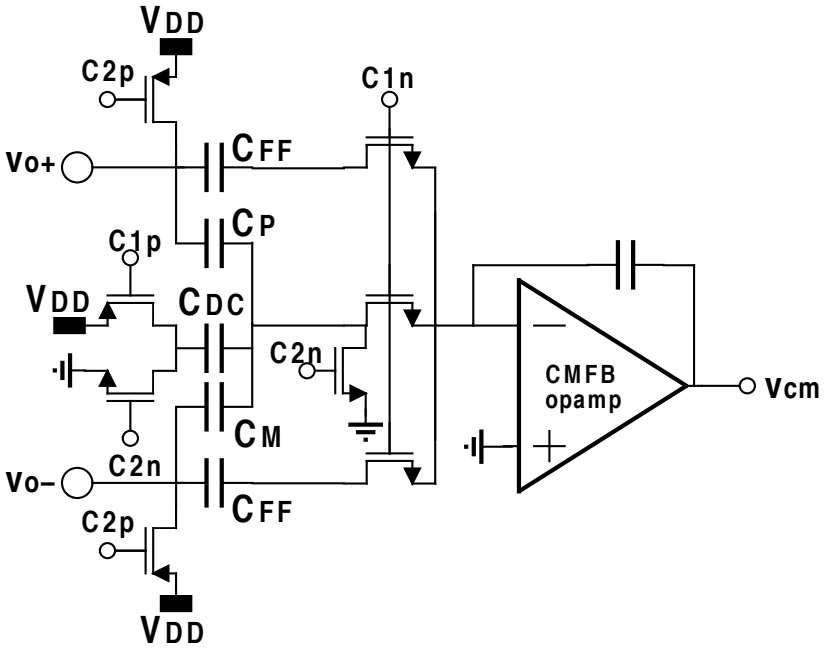
- Passive level shift



- CM input of CMFB opamp is close to GND
- Lower CMFB G_{LOOP}

$$V_{DDmin} = V_{TH} + 3 \cdot V_{OV}$$

- Switched-Opamp CMFB circuit



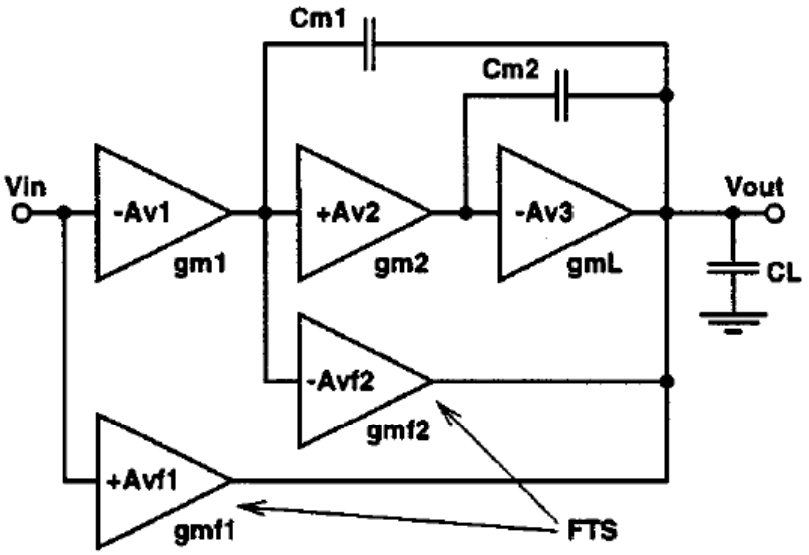
- CM input of CMFB opamp is set to GND
- Charge domain level shifter (C_{CM})
- All switches connected to V_{DD} or GND

$$V_{DDmin} = V_{TH} + 2 \cdot V_{OV}$$

ScalTech Opamp

Higher-gain structures

- CMOS gain-per-stage is dropping with technology scaling
- LV design disables cascode
  - ➔ Multistage structure are needed
    - Compensation scheme are becoming crucial
      - Feedback (Miller cap)
      - Feedforward (g_m)



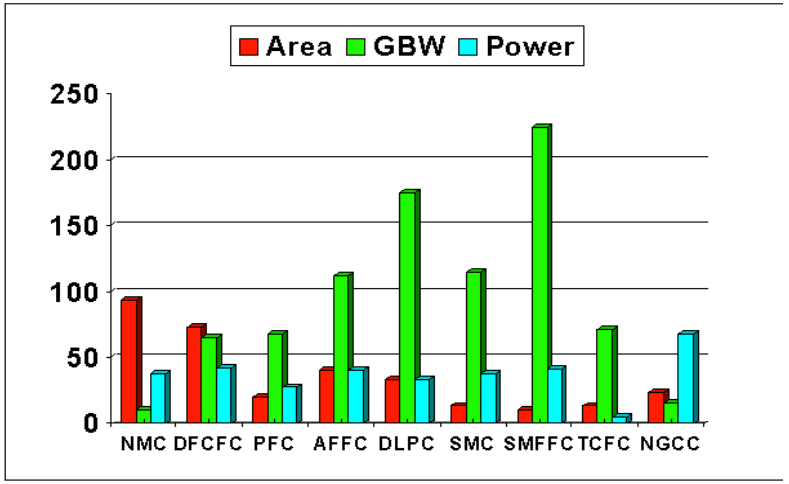
- FD structures are mandatory for achieving a sufficient DR
  - LV CMFB is critical
  - Feedforward paths are not seen by the CMFB !!!

ScalTech Opamp

Possible structures

- Multistage opamp topology
  - Nested Miller Compensation (NMC)
  - Damping-Factor-Control Frequency Compensation (DFCFC)
  - Positive Feedback Compensation (PFC)
  - Active Feedback Frequency Compensation (AFFC)
  - Single Miller capacitor Compensation (SMC)
  - Single Miller capacitor FeedForward Compensation (SMFFC)
  - Transconductance with Capacitance Feedback Compensation (TCFC)
  - Nested Gm-C Compensation (NGCC)
  - Dual-Loop Parallel Compensation (DLPC)

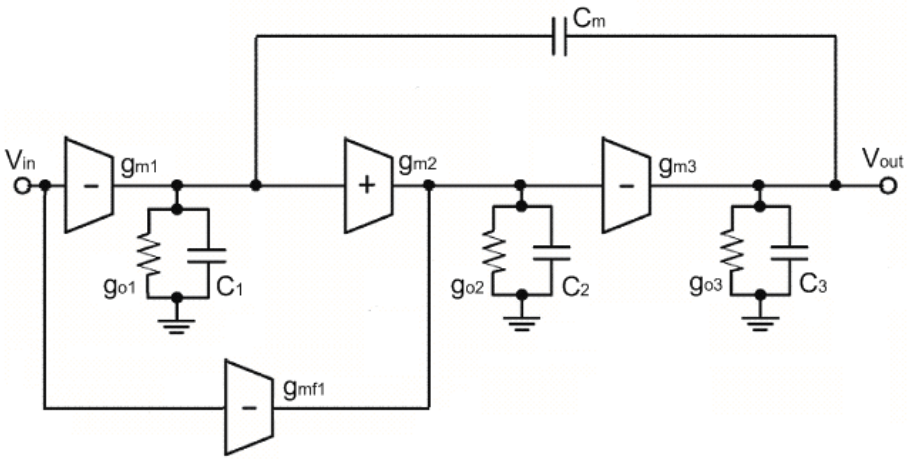
- To be compared in terms of:
  - AC Performance (Gain, bandwidth, phase margin)
  - Load driving capability
  - Power consumption
  - Area
    - Compensation cap is not scaling with technology

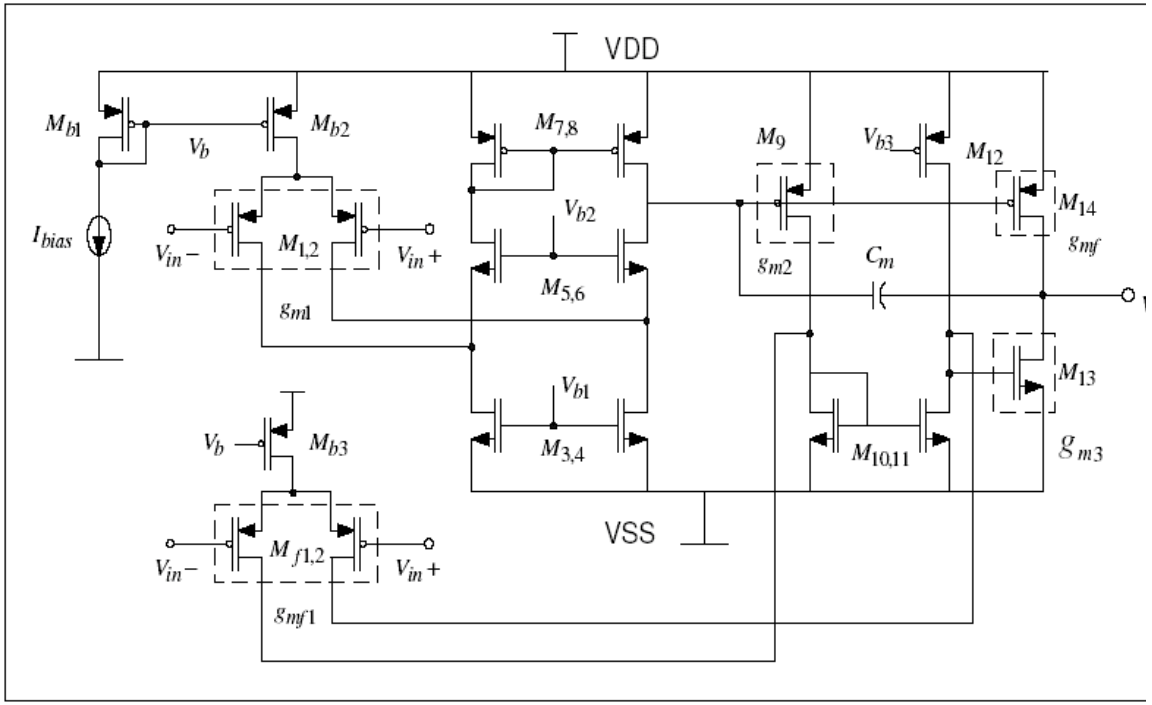


ScalTech Opamp

3-stage-opamp

- Feedforward path for compesation *



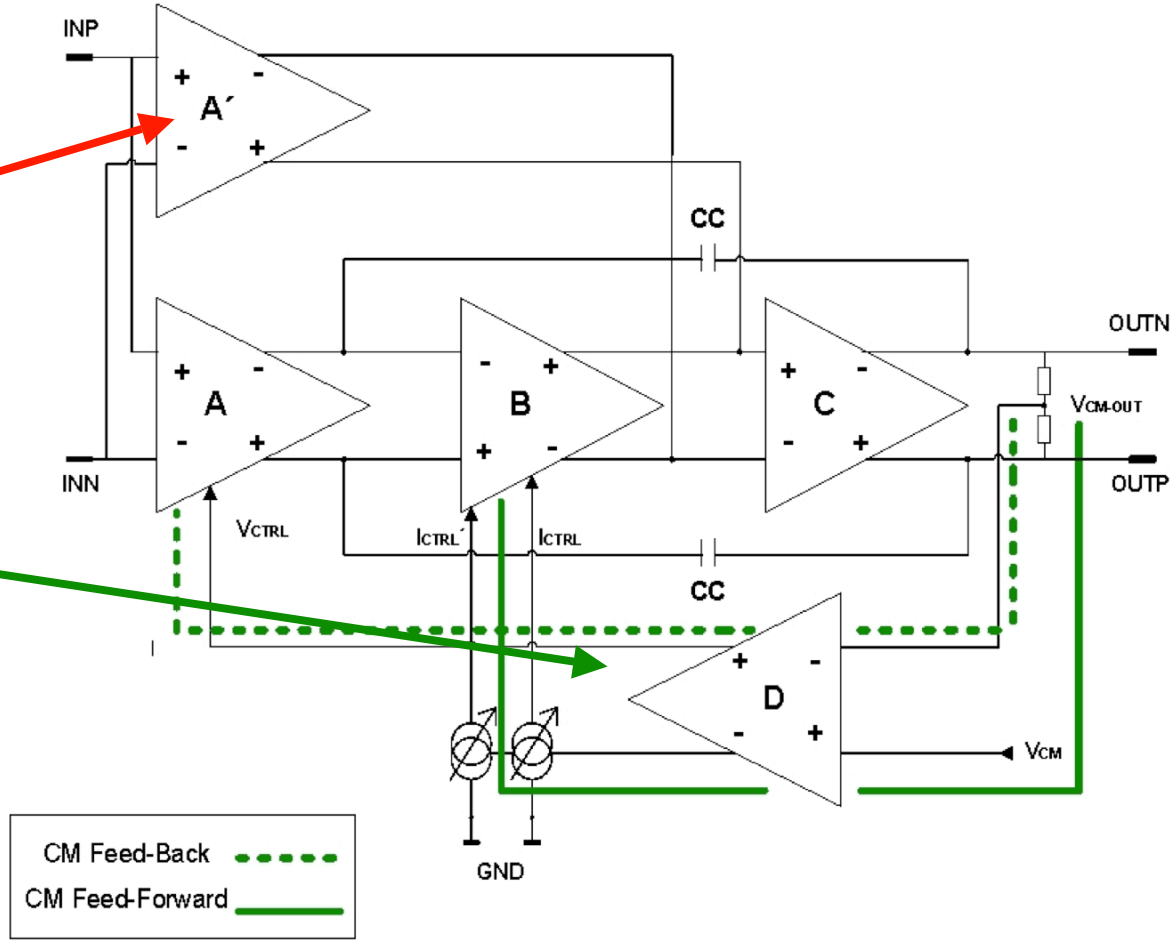


* I. Di Sancarlo, ESSCIRC 2008

ScalTech Opamp Design

Multistage Common-Mode Feedback Circuit

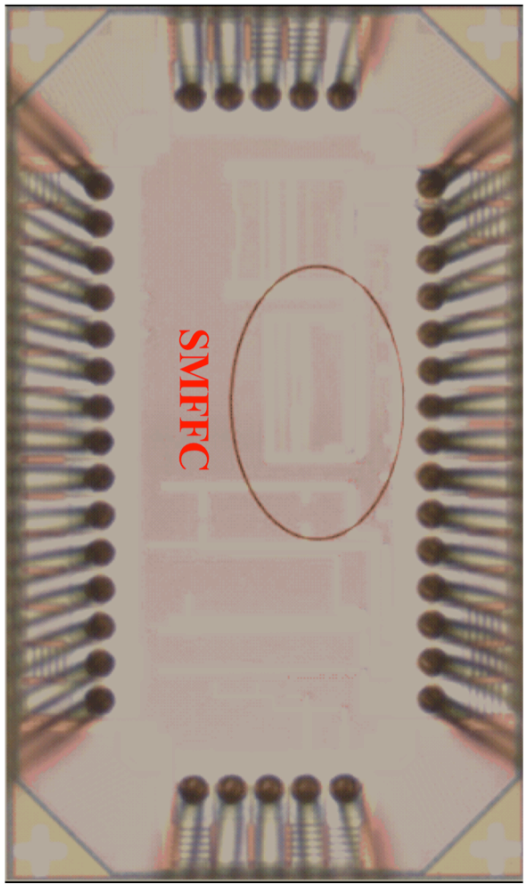
- The diff-mode feedforward paths are not valid for the CMFB
  - ➔ A feed-forward path is added in the CMFB



ScalTech Opamp Design

3-stage SMFFC opamp prototype

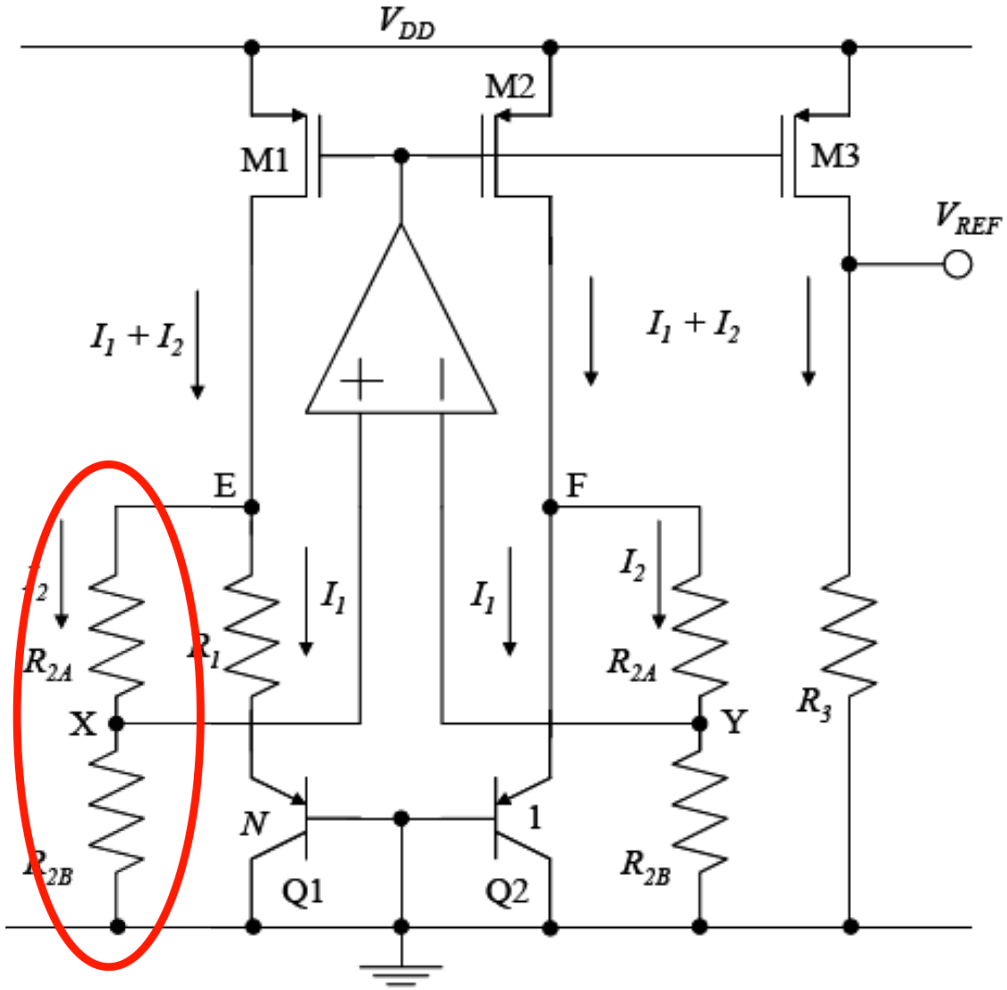
- Experimental results



Parameter	***Performance***
Technology CMOS	65nm
Differential Gain/UGB	84dB / 200MHz
Common Mode Gain/UGB	85dB / 136MHz
PSRR@1MHz	60dB
CMRR@1MHz	38dB
HD3@5MHz	-82dBc
Output Noise@1MHz	27nV/√Hz
Power Consumption	10mW

Bandgap Reference Voltage

Sub-1V operation is possible *



* K.N. Leung and P.K.T. Mok, "A Sub-1-V 15-ppm/oC CMOS Bandgap Voltage Reference without Requiring Low Threshold Voltage Device," *IEEE Journal of Solid-State Circuits*, vol.37, pp.526-530, Apr. 2002

Analog Design in ScalTech

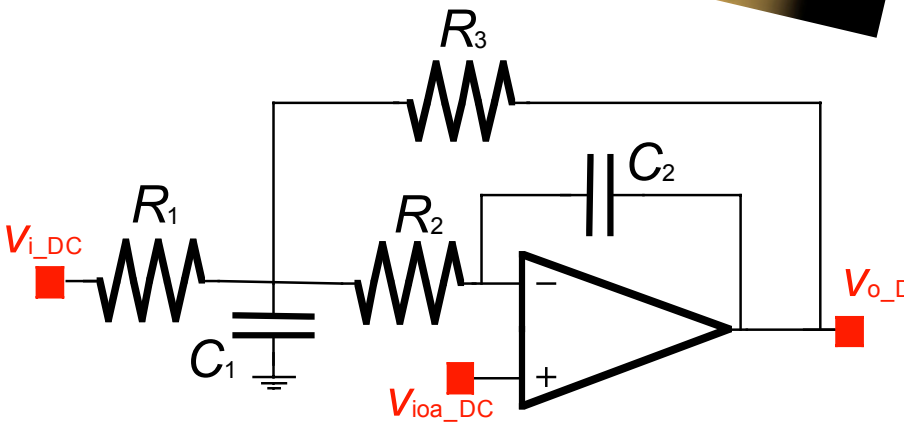
Outline

- CMOS technology scaling trends
  - Power reduction
  - $\{V_{DD}-V_{TH}\}$ reduction
  - Gain reduction
  - V_{TH} variation
- **ScalTech** Analog design
  - **ScalTech** at transistor level
    - Transistor in subthreshold
  - **ScalTech** at circuit level
    - Analog switch
    - Opamp design
    - Basic bandgap design
  - **ScalTech** at system level
    - Analog filter
    - ADC

ScalTech Analog Filter

Low voltage

- Active-RC filters guarantee the required linearity
- Analog filter critical points
  - Bias point
  - Low & non-linear output impedance
    - Frequency response accuracy
    - In-band & out-of-band linearity



$$HD3 \approx \frac{a_3}{2 \cdot a_1^4 \cdot \beta} \cdot V_o^2 \cdot \left(1 + \frac{V_o}{3 \cdot V_i}\right)$$

- Possible solution
  - Automatic filter design

Analog filters

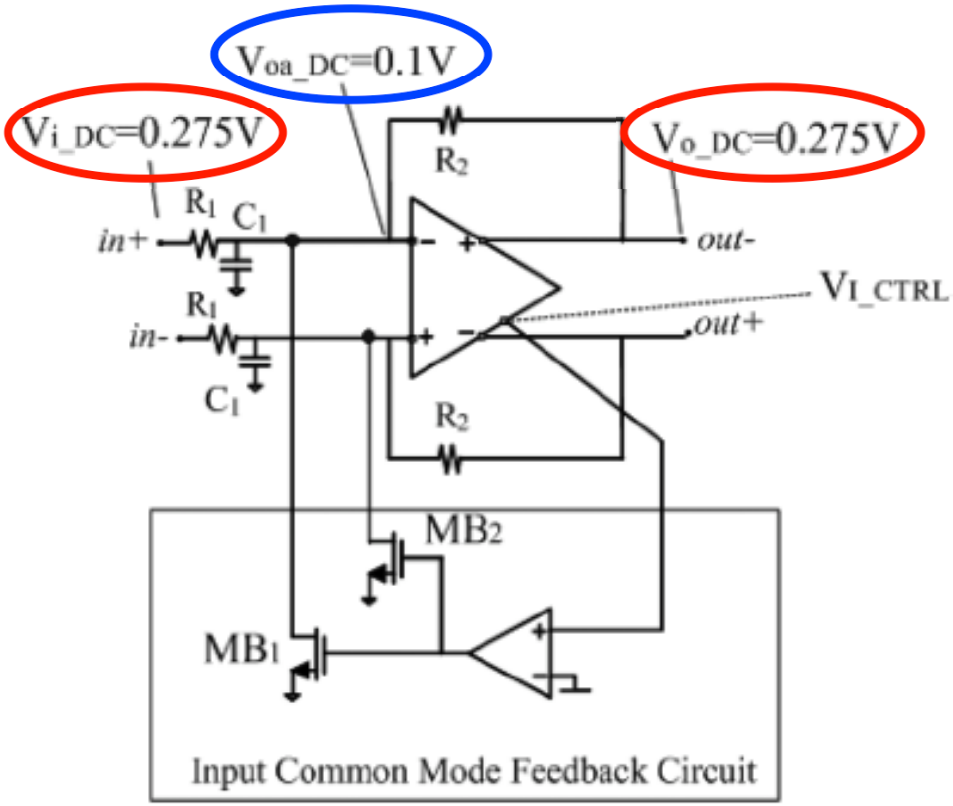
Very-Low-Voltage design example

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 9, SEPTEMBER 2009 2525

A 0.55 V 60 dB-DR Fourth-Order Analog Baseband Filter

Marcello De Matteis, Stefano D'Amico, *Member, IEEE*, and Andrea Baschirotto, *Senior Member, IEEE*

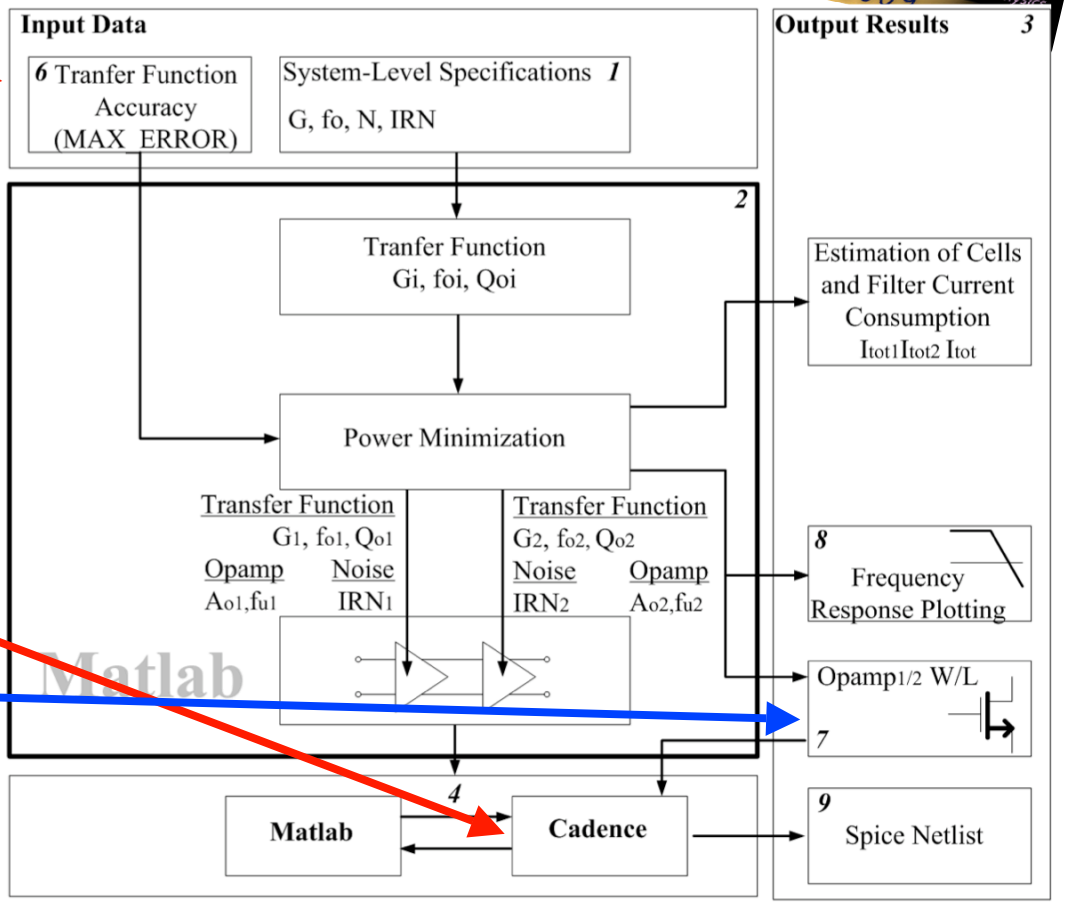
- Input Common-mode Feedback Circuit
  - Optimum bias
    - $Filter_{Input} = Filter_{Output} = V_{DD}/2$
      - Rail-to-rail output swing
    - **$Opamp_{Input}$** close to GND ≠ $Filter_{Input}$
- Active-Gm-RC structure
  - Lower power consumption, current, V_{GS}
- Equation-based Automatic design
  - Transistor quadratic law
  - Power consumption minimization



ScalTech Analog Filter

Simulator-based Automatic filter design

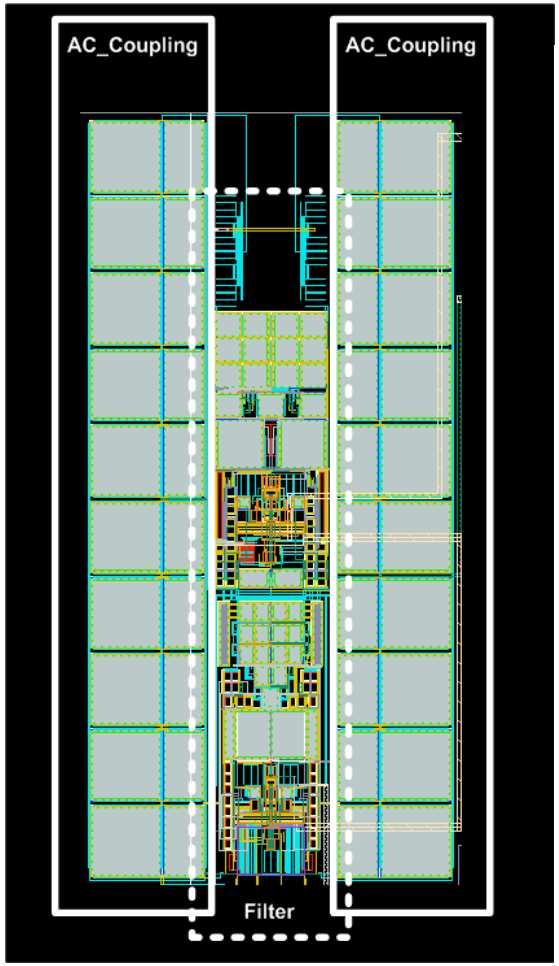
- A list of input data
- Performance achievement
  - Transfer function
  - Noise
  - In-band & Out-of-band linearity
  - ➔ Power consumption minimization
- Use of iterative SPICE simulation
  - Suited automatic-design algorithms achieve large signal performance
    - Even with **ScalTech** non-ideal effect



ScalTech Analog Filter

Simulator-based Automatic filter design

- 65nm Silicon prototype



Simulated performance

Parameter	Nominal	Worst Case
G[dB]	30.6	29.5
$f_{@-3dB}$[MHz]	7.8	7.25
V_{DD}[V]	1.2	1.1/1.3
CMOS Technology	65nm	-
V_{TH}	0.45V	0.5
Power Consumption[mW]	1.3	1.6
Output Integrated Noise[mV_{rms}] (100kHz÷10MHz)	1.73	1.9
IRN Spectral Density@7MHz [nV/√Hz]	18	20
Output 1dBcP – [$V_{zero\text{-}peak}$]	0.9	0.79
THD[dBc] – v_{out}=850m$V_{zero\text{-}peak}$@3MHz	40	38
SNR@THD=40dBc - [dB]	52	50.8
IIP3 [dBm] $v_{in}=v_{in1}+v_{in2}$[dBc] v_{in1}@4MHz and v_{in2}@6MHz	-10	-12

ScalTech Analog-to-Digital Converters

Low voltage

- ADC critical points
  - Bias point
  - Low & non-linear output impedance
  - Mismatch

- Popular ADC topology: Pipeline ADC
  - ☺ The internal speed-of-operation is the same of the external data-rate
  - ☹ Algorithm is based on opamp performance

- Alternative solutions
  - ☺ Adopt ADC topologies with low performance sensitivity to scaling
    - They operates at higher internal speed
      - Ex.: SAR & ΣΔ
  - ☺ Use the additional digital signal processing (low power & low area in **ScalTech**)
    - To improve analog performance
    - Different digital correction algorithms for Different analog critical performance errors
      - Effectiveness
      - Speed requirement
      - Complexity
      - Time to convergency

ScalTech Pipeline ADC

Performance requirement summary

- ADC requirement: N bit & Stage resolution: B bit
  - ➔ Stage requirements

Parameters	*Minimum requirement*
Opamp DC gain	$A > \frac{(2^{N-B})}{\beta} \Rightarrow A > 2^N$
Settling time (Single pole approximation)	$\tau < \frac{1}{2 \cdot F_s \cdot N \cdot ln(2)}$
DAC Accuracy	$\left\|\frac{\Delta C}{C}\right\| < \frac{1}{2^N}$
Noise	$V_{N,TH} << LSB = \frac{V_{FS}}{2^N}$

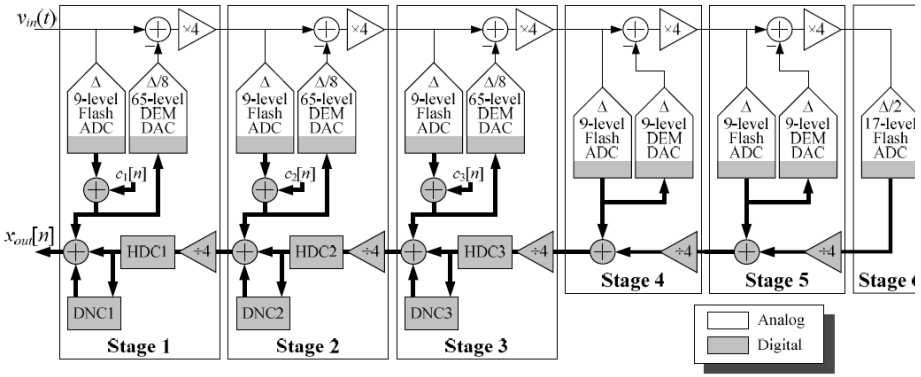
- In **ScalTech** DC-Gain spec is difficult to achieve

- Also linearity has to be considered

ScalTech Pipeline ADC

Digital correction algorithms

- Harmonic Distortion correction in residue amplifiers
  - Panigada, Galton, "A 130mW 100MS/s Pipelined ADC with ***69dB SNDR*** Enabled by Digital Harmonic Distortion Correction", ISSCC09 & IEEE TCAS Sept.09
  - B. Murmann, B. Boser, "A 12b 75MS/s Pipelined ADC ***using Open-Loop Residue Amplification***," IEEE JSSC, Dec. 2003



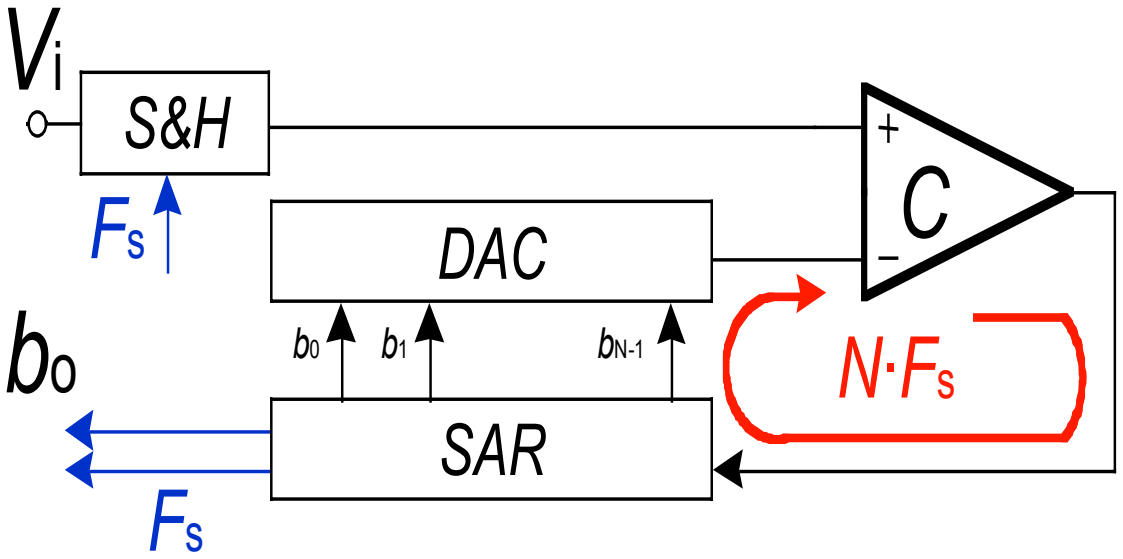
- Residue Amplifier Gain Calibration
  - E. Siragusa, I. Galton, "A Digitally Enhanced 1.8V 15b 40MS/s CMOS Pipelined ADC," IEEE JSSC, Dec. 2004
  - R.G. Massolini, G. Cesura, R. Castello,"A fully digital ***fast convergence*** algorithm for nonlinearity correction in multistage ADC", IEEE TCASII, May 2006.
  - G. Ahn *et al*., "A 12b 10Ms/s pipelined ADC using reference scaling", *Proc.IEEE Int. Symp. on VLSI Circuits*, pp. 220-221, Sep. 2006

- DAC Calibration
  - E. Siragusa, I. Galton, "A Digitally Enhanced 1.8V **15b** 40MS/s CMOS Pipelined ADC," IEEE JSSC, Dec. 2004.
  - I. Galton, "Digital cancellation of D/A converter noise in pipelined A/D converters", TCASII Mar. 2000
  - Sourja Ray, Bang-Sup Song, "A **13-b** Linear, 40-MS/s Pipelined ADC With Self-Configured Capacitor Matching", IEEE JSSC Mar 2007
  - S. Sutarja, P.R. Gray, "A pipelined 13-bit 250-ks/s 5-V analog-to-digital converter", IEEE Journal of Solid-State Circuits, Dec. 1988

ScalTech SAR ADC

Key features

- The ***N***-bit digitalization process needs ***N*** clock cycles
  - For a given output data-rate (F_s)
    - the internal circuit operates at higher frequency $\approx \boldsymbol{N} \cdot F_s$
- No input signal processing
  - Only a (passive) S&H
- Active blocks:
  - A critical DAC
  - A non-critical comparator
- Very low power consumption
  - No opamp
  - Power is consumed by the comparator, the **DAC**, the logic



ScalTech SAR ADC

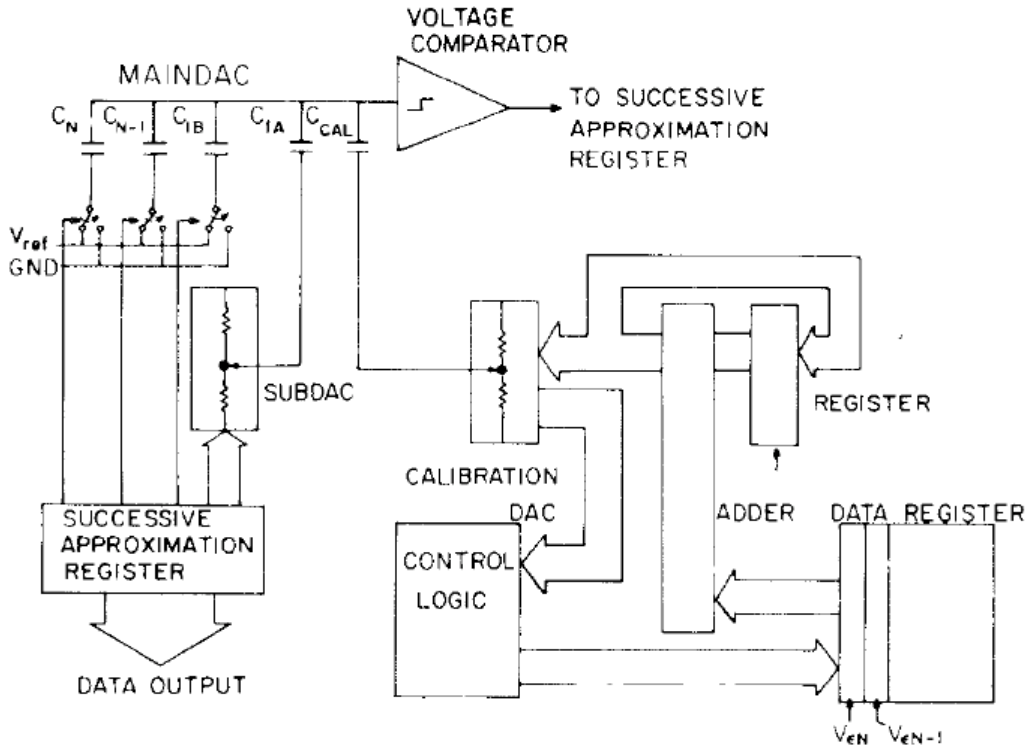
Digital correction

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-19, NO. 6, DECEMBER 1984

Special Papers

A Self-Calibrating 15 Bit CMOS A/D Converter

HAE-SEUNG LEE, STUDENT MEMBER, IEEE, DAVID A. HODGES, FELLOW, IEEE, AND PAUL R. GRAY, FELLOW, IEEE



UNIVERSITÀ DEGLI STUDI DI MILANO BICOCCA

ScalTech SAR ADC

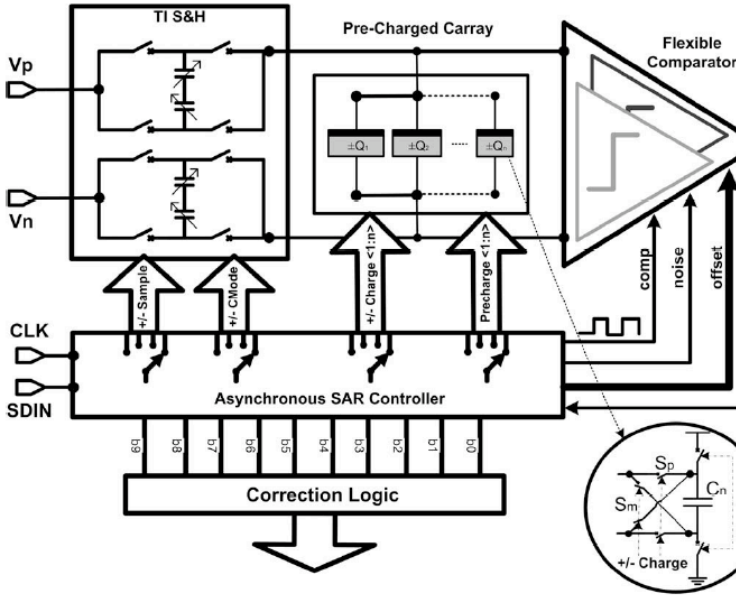
Digital correction

ISSCC 2008 / SESSION 12 / HIGH-EFFICIENCY DATA

12.1 An 820µW 9b 40MS/s Noise-Tolerant Dynamic-SAR ADC in 90nm Digital CMOS

Vito Giannini[1], Pierluigi Nuzzo[1], Vincenzo Chironi[2], Andrea Baschirotto[2], Geert Van der Plas[1], Jan Craninckx[1]

[1]IMEC, Leuven, Belgium, [2]University of Salento, Lecce, Italy

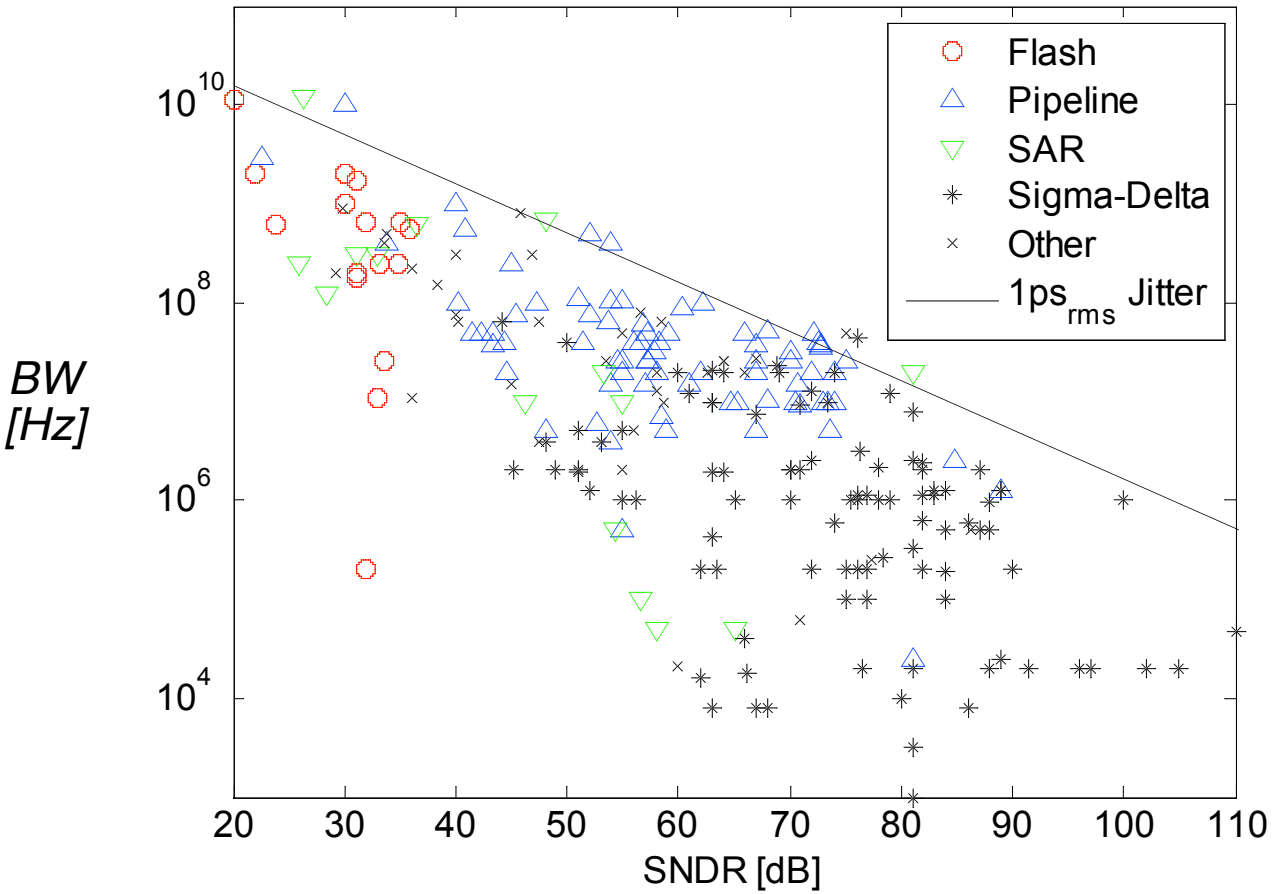


- Charge-sharing implementation
  - Minimum power consumption
- Conversion step redundancy
  - Performance robustness
- Adjustable comparator input noise
  - Minimum power consumption
- Asynchronous SAR
  - Highest sampling frequency

Ref.	Tech	ERBW	ENOB	VDD	Power	FoM
Shrivastava - ISCAS06	0.13µm	2.1MHz	11.41	1.2	6.6mW	577fJ/conv
Hesener - ISSCC07	0.13µm	20MHz	13.49	1.5	66mW	143fJ/conv
Craninckx - ISSCC07	90nm	10MHz	7.8	1	290µW	65fJ/conv
This work	***90nm***	***32MHz***	***8.56***	***1***	***820µW***	***54fJ/conv***

SAR ADC

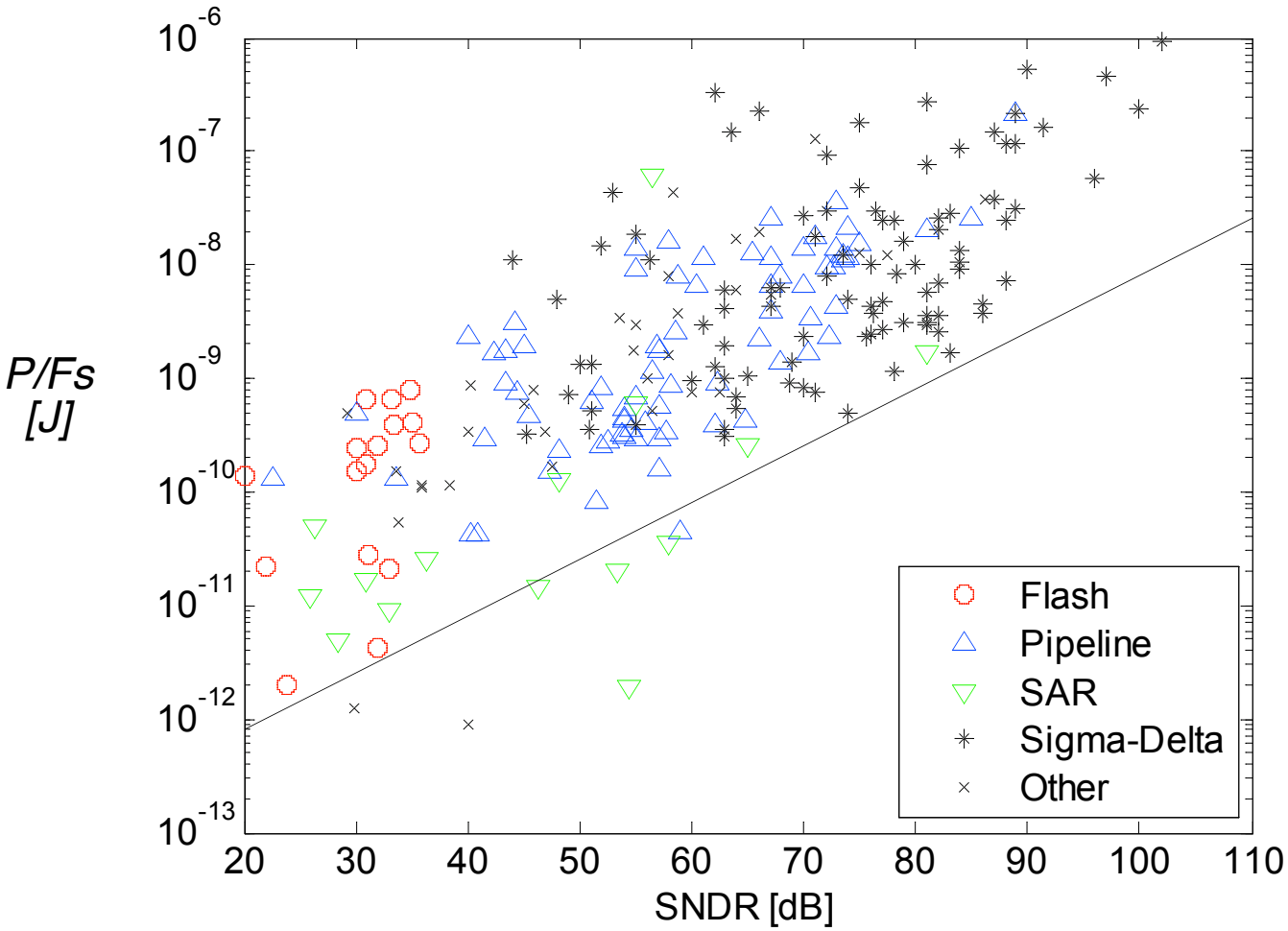
Performance Scenario *



* B. Murmann, "ADC Performance Survey 1997-2009," [Online]: http://www.stanford.edu/~murmann/adcsurvey.html

SAR ADC

Performance Scenario *



* B. Murmann, "ADC Performance Survey 1997-2009," [Online]: http://www.stanford.edu/~murmann/adcsurvey.html

(Low-Power) Analog Design in Scaled Technologies

A. Baschirotto[1], G. Cocciolo[2], S. D'Amico[2], M. De Matteis[2], P. Delizia[2]

Thank you !!!

ScalTech ➔ LV

Low-Voltage vs. Low-Power - V_{DD} reduction

- V_{DD} scaling affects analog circuit **performance**

$$FoM_P = \frac{4 \cdot k \cdot T \cdot DR^2 \cdot BW}{P}$$

FoM$_P$ ⇔ the power dissipation

$$FoM_I = \frac{4 \cdot k \cdot T \cdot DR^2 \cdot BW}{I}$$

FoM$_I$ ⇔ the current consumption (F_I=F_P·V_{DD})

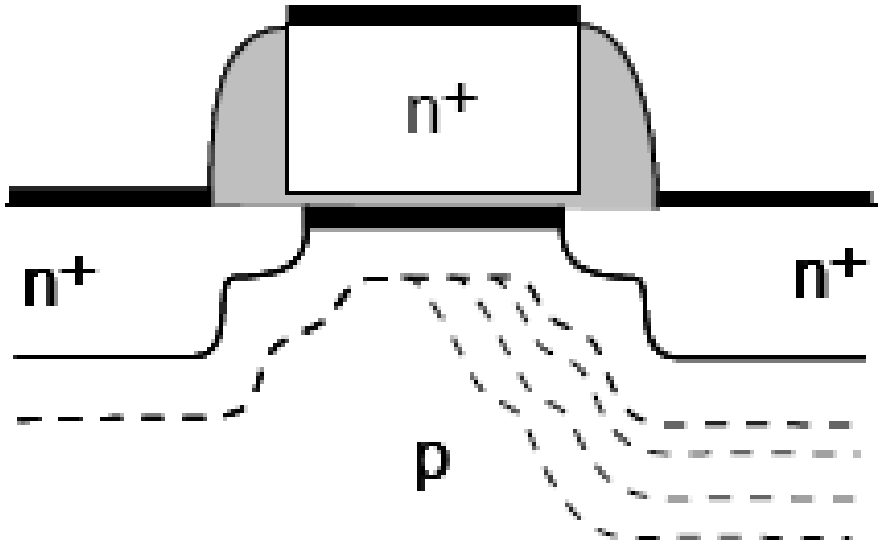
- ➔ F_I does not consider P reduction due to the V_{DD} scaling
- ➔ F_I considers only the P increase for maintaining the DR

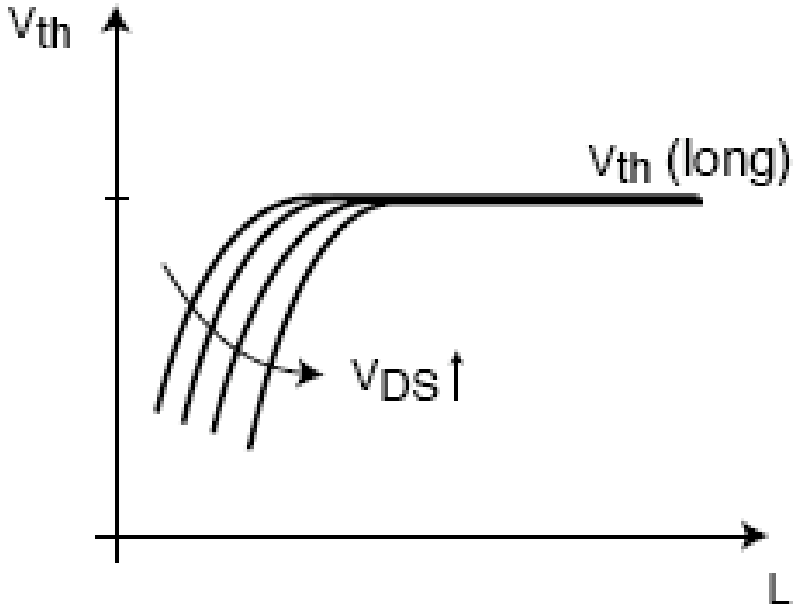
Reference	*Year*	*V_{DD} [V]*	*DR [dB]*	*BW [kHz]*	*P [mW]*	*F_P [× 10^6]*	*F_I [× 10^6]*
Dessouky	*2001*	*1*	*88*	*25*	*1.00*	*261*	*261*
Peluso	*1998*	*0.9*	*77*	*16*	*0.04*	*332*	*299*
Libin	*2004*	*1*	*88*	*20*	*0.14*	*1493*	*1493*
Rabii	*1997*	*1.8*	*99*	*25*	*2.50*	*1316*	*2369*
Williams	*1994*	*5*	*104*	*50*	*47.00*	*443*	*2214*
Nys	*1997*	*5*	*112*	*0.4*	*2.18*	*483*	*2415*
Wang	*2003*	*5*	*113*	*20*	*115.00*	*575*	*2875*
YuQing	*2003*	*5*	*114*	*20*	*34.00*	*2448*	*12240*

CMOS Technology scaling

Drain Induced Barrier Lowering (DIBL)

- For **short L**, V_S and V_D influence the channel surface potential and tends to make it far what would be obtained from the long-channel approximation
  - ➔ I_D Increase, particularly in weak and moderate inversion
- Depletion region associated with drain junction expands
  - $V_{DS}\uparrow \Rightarrow$ additional V_{TH} shift

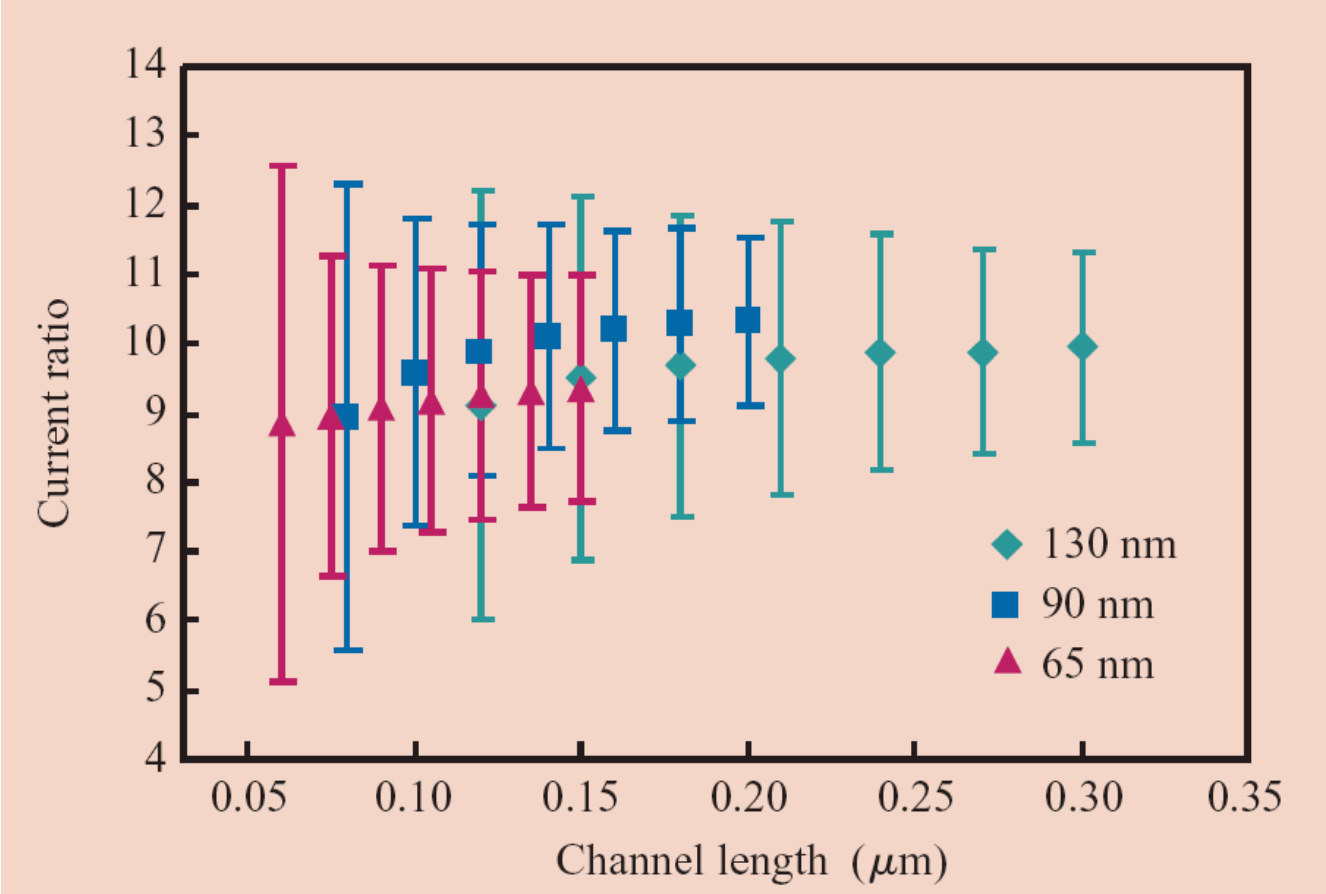




CMOS Technology scaling

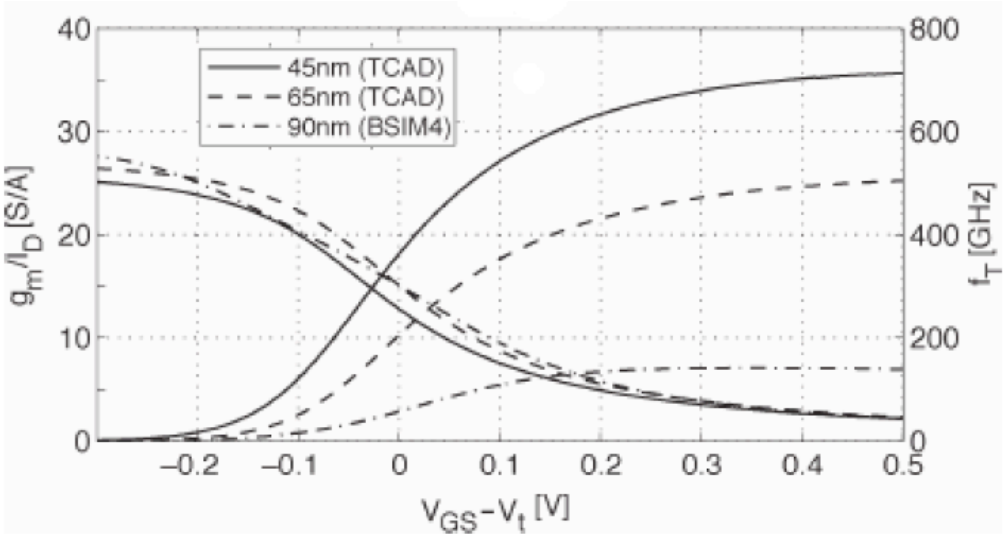
Geometrical mismatch

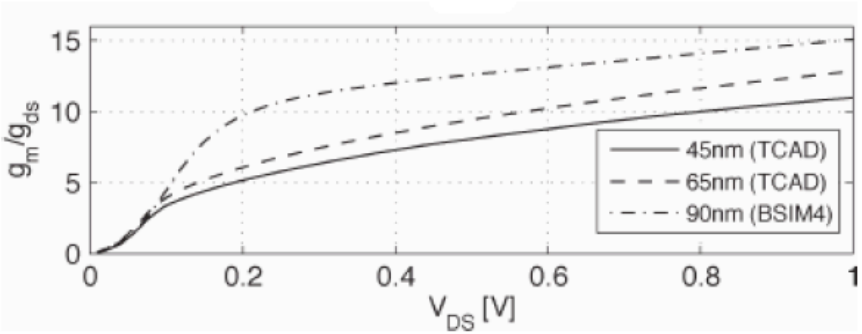
- Basic Current Mirror
  - Current-ratio variability of 10:1 current mirror



CMOS Technology scaling

Overall trends





- $g_m/I_d \approx$ Constant
- f_T ↗
- g_m/g_{ds} ↘
- V_{DD} ↘

⇓

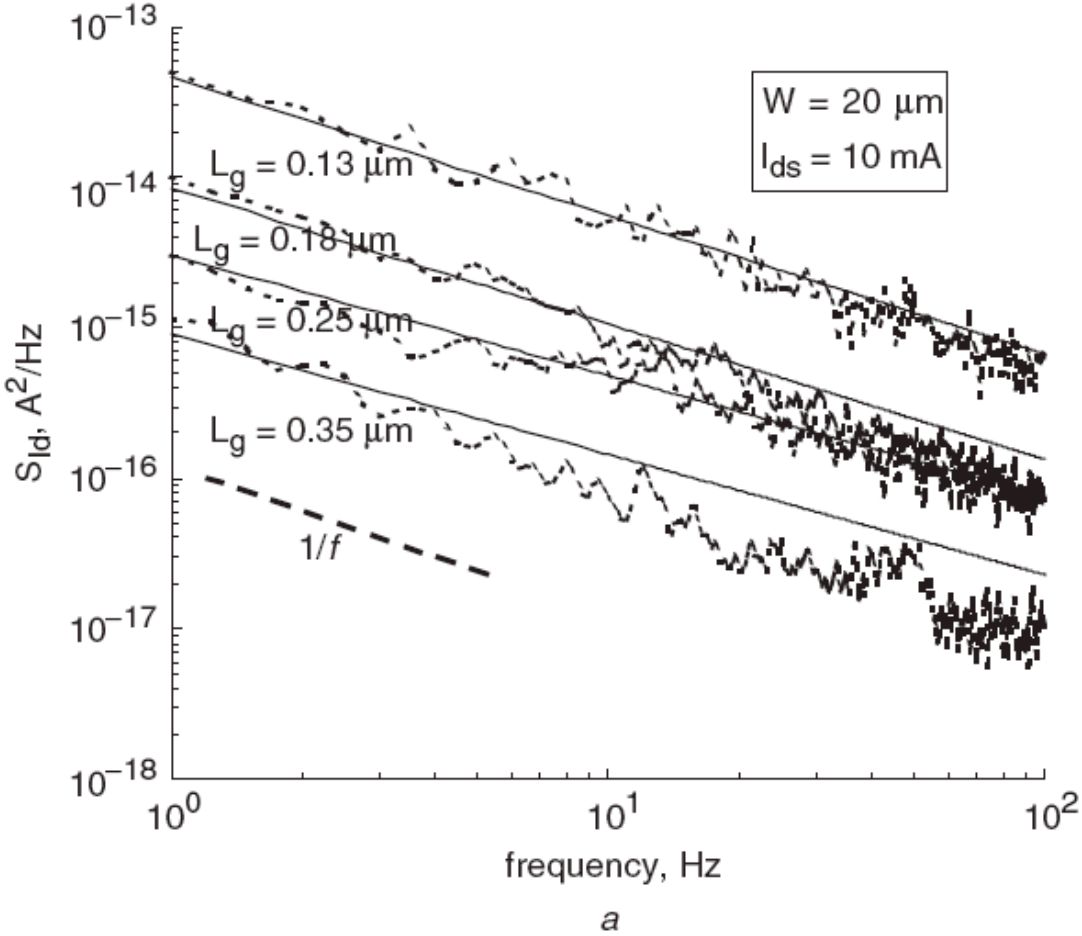
- Speed ↗
- Signal-to-distortion ratio (SDR) ↘
- Signal-to-noise ratio (SNR) ↘

CMOS Technology scaling

1/f noise *

- Effect of technology scaling drain current noise spectra of thin gate oxide, minimum channel length NMOS

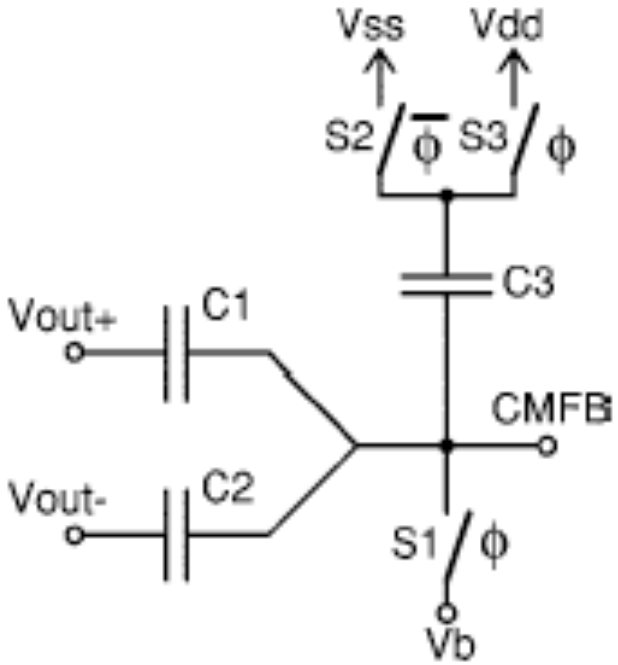
- V_{DS} for each technology node corresponds to its respective V_{DD}



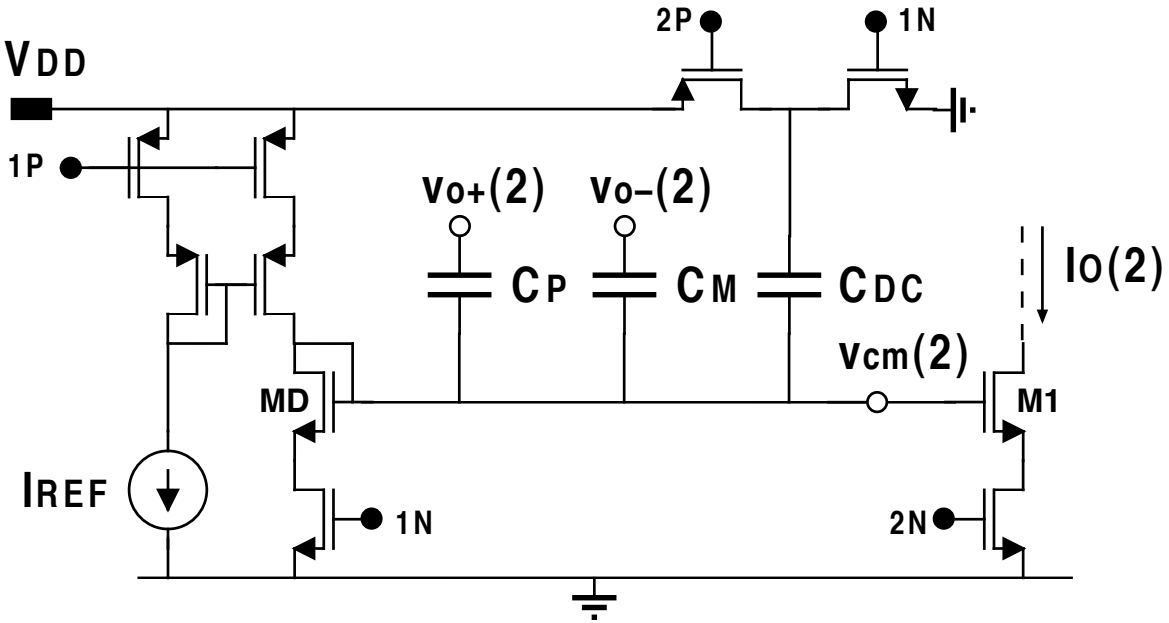
* K.W. Chew, K.S. Yeo and S.-F. Chu, "Impact of technology scaling on the 1/*f* noise of thin and thick gate oxide deep submicron NMOS transistors", IEE Proc.-Circuits Devices Syst., October 2004

Passive Switched-Opamp CMFB circuit

- No opamp
  - Basic solution



  - S_1 increases V_{DDmin}
  - Improved solution



  - All switches connected to GND or V_{DD}

ScalTech Analog Filter

Non-constant opamp gain Distortion

- The opamp V_i-to-V_o:

$$V_o = a_1 \cdot V_i + a_2 \cdot V_i^2 + a_3 \cdot V_i^3 + ...$$

- Non-constant opamp gain results in signal distortion

$$HD2 \approx \frac{a_2}{2 \cdot a_1^3 \cdot \beta} \cdot V_o \cdot \sqrt{1 + \left(\frac{V_o}{2 \cdot V_i}\right)^2} \qquad HD3 \approx \frac{a_3}{2 \cdot a_1^4 \cdot \beta} \cdot V_o^2 \cdot \left(1 + \frac{V_o}{3 \cdot V_i}\right)$$

- The distortion can then be reduced
  - using a very large opamp gain (i.e. increasing a_1)
  - making constant low-gain (i.e. reducing a_2 and a_3)
  - even order harmonics are greatly reduced by using fully-differential structures

Analog-to-Digital Converters

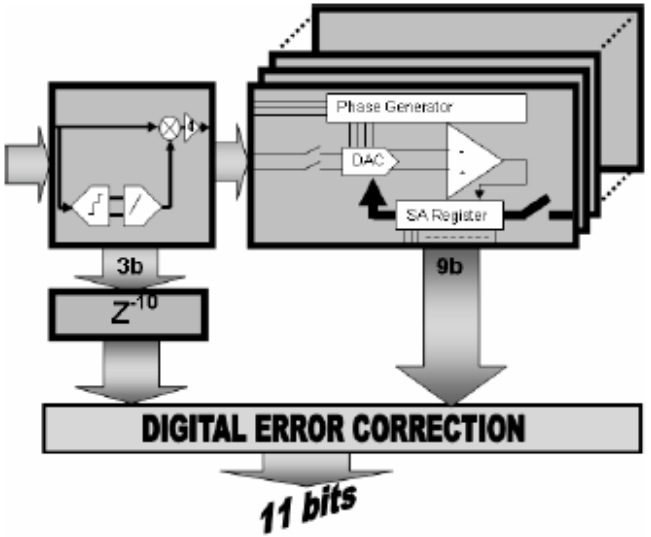
65nm design example

IEEE 2008 Custom Intergrated Circuits Conference (CICC)

A 1.2v 11b 100Msps 15mW ADC realized using 2.5b pipelined stage followed by time interleaved SAR in 65nm digital CMOS process

Pratap Narayan Singh, Ashish Kumar, Chandrajit Debnath, Rakesh Malik
STMicroelectronics India

- The 9b SAR ADC reduces power consumption
- An MSB pipelined stage holds the signal for the SAR
  - No sampling skew problem associated with time interleaved SAR ADCs.



Analog-to-Digital Converters

45nm design example

ISSCC 2009 / SESSION 4 / HIGH-SPEED DATA CONVE

4.2 A 1.1V 50mW 2.5GS/s 7b Time-Interleaved C-2C SAR ADC in 45nm LP Digital CMOS

Erkan Alpman[1,2], Hasnain Lakdawala[1], L. Richard Carley[2], K. Soumyanath[1]

[1]Intel, Hillsboro, OR
[2]Carnegie Mellon University, Pittsburgh, PA

- A small-area C-2C SAR architecture
  - ➔ low input capacitance
- High-speed boosted switches
  - ➔ overcome high device threshold
- A background comparator offset calibration and radix calibration
- A redundant-ADC-based gain, offset and timing calibration
  - ➔ TI errors reduction

Process	45nm LP CMOS
Active Area	1mm^2
Resolution	7 bits
Sample Rate	2.5GS/s
Supply Voltage	1.1V
V_{ref_max}	700mV
V_{ref_min}	200mV
Input Range	1.0$V_{pp\text{-}diff}$
Power Consumption	50mW
DNL/INL	±0.5LSB / ±0.8LSB
Single ADC SNDR/SFDR	>38dB/ <-49dBc
Single ADC ENOB	6.1b within Nyquist
Single ADC FOM	180fJ/conv
TI SAR ADC SNDR/SFDR	>34dB/ <-43dBc
TI SAR ADC ENOB	>5.4b within Nyquist
TI SAR ADC FOM	480fJ/conv

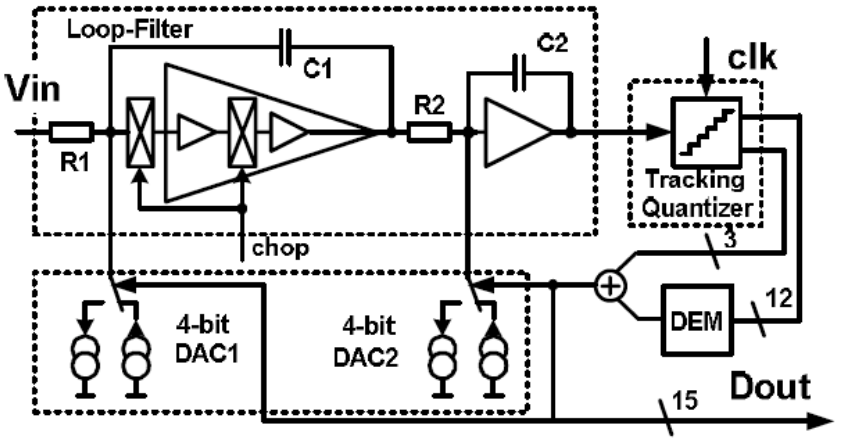
Analog-to-Digital Converters

65nm design example

A 2.2mW, Continuous-Time Sigma-Delta ADC for Voice Coding with 95dB Dynamic Range in a 65nm CMOS Process

Lukas Dörrer, Franz Kuttner, Andreas Santner, Claus Kropf, Thomas Hartig, Patrick Torta, Patrizia Greco
Infineon Technologies Austria AG
Villach, Austria
lukas.doerrer@infineon.com

- A ΣΔ feedback topology
- A chopped first operational amplifier
  - Gain = 50dB
- A tracking quantizier
- A RZ-DAC in the first stage
  - ➔ No preamplifier or anti-aliasing filter



Analog-to-Digital Converters

45nm design example

ISSCC 2008 / SESSION 27 / ΔΣ DATA CONVERTERS

27.8 A Continuous Time ΔΣ ADC for Voice Coding with 92dB DR in 45nm CMOS

Lukas Dörrer, Franz Kuttner, Andreas Santner, Claus Kropf, Thomas Puaschitz, Thomas Hartig, Manfred Punzenberger

Infineon Technologies, Villach, Austria

- Current-steering DAC provides spectral information (harmonics) about dynamic MOS transistor mismatch.
- The SC quantizer reveals dynamic mismatch of capacitances.
- The optional chopped filter input stage separates flicker noise of weakly and strongly inverted transistors.
- Excess loop delay and jitter can be seen in the power spectral density (PSD) plot