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Application of a new interconnection technology for the ATLAS pixel upgrade at SLHC

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We present an R&D activity aiming towards a new detector concept in the framework of the ATLAS pixel detector upgrade exploiting vertical integration technologies developed at the Fraunhofer Institute IZM-Munich. A new Solid-Liquid-InterDiffusion technique is investigated as an alternative to the bump-bonding process. We also investigate the extraction of the signals from the back of the electronic chip through Inter-Chip-Vias to achieve a higher fraction of active area with respect to the present pixel module design. We will present the layout and the first results obtained with a production of test-structures designed to investigate the SLID interconnection efficiency as a function of different parameters, i.e. the pixel size and pitch, and the planarity of the underlying layers.

Summary

Our R&D activity is focused to develop a new detector concept for the upgrade of the ATLAS pixel system at SLHC.
The Solid-Liquid-InterDiffusion (SLID) is a new interconnection technology between sensors and front-end electronics, developed by Fraunhofer IZM-Munich. SLID is investigated in this R&D activity because it can in principle overcome some limitations inherent to the present bump bonding process, namely the high cost and the minimum feature size required. Moreover SLID allows the stacking of different ASIC layers because the bonding process does not affect the SLID connections realized in a previous step.
Pixel sensors, with an active thickness of 75 and 150 um, produced at the MPI Halbleiterlabor (MPI-HLL) in collaboration with industrial partners, will be connected by the SLID process to the FE-I3 chips. The contact scheme in the passivation layer of the pixel sensors has been modified to be compatible with the SLID interconnection. In all the other details the design of the active area is unchanged with respect to the present ATLAS pixels. The SLID interconnection will be obtained in the "chip to wafer"approach. This offers the possibility of singularizing the chips thus helping to increase the process yield. On the other hand it introduces a placement uncertainty due to the chip positioning on the handle wafer needed to support the ASICs during the SLID interconnection. The signals that in the present layout are extracted via wire-bonding to the bonding pad in the cantilever will be routed through Inter-Chip-Vias from the ASIC backside where post-processing bonding pads will be created. For this purpose the ATLAS FE-I3 wafer will be thinned down to about 50 um.
We will present the layout and the first results obtained with a production of test-structures designed to investigate the performance of the SLID interconnection. The basic test devices are daisy chains with different pad sizes and pitches. In some of the chains we introduced a imperfect planarity of the surface beneath the SLID pads to study the effect on the interconnection efficiency. The "sensor"and "chip"structures, produced at MPI-HLL have been connected both "wafer to wafer"and "chip to wafer". The deposition of the metal system for SLID and interconnections have been performed at IZM-Munich. A good interconnection efficiency has been measured for all pad geometries. The size of the misalignment between sensors and chip structures has been evaluated. We will report on the results of the observations of the interconnected wafers with an infrared microscope to study the definition of the SLID metal system.

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