An integrated DC-DC step-up charge pump and step-down converter in 130 nm technology

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Abstract

After the LHC luminosity upgrade the number of readout channels in the ATLAS Inner Detector will be increased by one order of magnitude and delivering the power to the front-end electronics as well as cooling will become a critical system issue. Therefore a new solution for powering the readout electronics has to be worked out. Two main approaches for the power distribution are under development, the serial powering of a chain of modules and the parallel powering with a DC-DC conversion stage on the detector. In both cases switched-capacitor converters in the CMOS front-end chips will be used. In the paper we present the design study of a step-up charge pump and a step-down converter. In optimized designs power efficiency of 85 % for the step-up converter and 92 % for the step-down converter has been achieved.

I. Introduction

The present design of Upgraded Atlas Inner Detector assumes about 10 times higher number of silicon strips compared to the present Semiconductor Tracker. Although the power consumption per channel is expected to be reduced significantly, the supply current will be reduced to a lesser degree and delivering power to the front-end chips is a big challenge. Two main approaches for power distribution are under development; the serial powering of a chain of modules and independent powering of modules from DC-DC converters located on the module. In either case switched-capacitor converters in the front-end chips will be used.

In the serial powering scheme, the 1.2 V clean supply voltage for the analog part of the front-end chip must be produced from 0.9 V digital power supply obtained from a shunt regulators. Therefore a linear voltage regulator must follow the step-up converter. Since the current consumed by the analogue part is constant and has moderate value (max. 30 mA), the optimization of the converter is focused on minimization of the output ripple. In this case, the output impedance and power efficiency is not of primary importance.

In the second possible scheme the digital part of the front-end electronics will be supplied directly from the on-chip DC-DC step-down converter providing 0.9 V. Due to high variations of the digital current consumption during chip operation and keeping in mind that the digital current is the substantial part of the global current in the chip, the main parameters to be optimized are the power efficiency and the output impedance.

II. Realization

A. Step-up DC-DC converter

1) Architecture and principle of the voltage pump

The developed step-up DC-DC converter is based on the concept of the voltage doubler proposed by P. Farvat et. al [1] and Y. Moisiadis et. al [2]. It consists of four building block: a non-overlapping clock generator, buffers, level shifters and a voltage doubler.

The core of the circuit is the voltage doubler, shown in Fig. 1. It consists of two cross-coupled, low V_t NMOS transistors (M1 and M2), four PMOS transistors with thick gate oxide working as serial switches (M3-M6), three external SMD capacitors (C_{PUMPX} and C_{HOLD}) and one small capacitance integrated on the chip (C_{POL}). For the simulation purposes a load resistance (R_{LOAD}) of 60 Ω was added at the output of the converter. An equivalent series resistance of SMD capacitors of 50 $m\Omega$ was taken into consideration as well. The 470 nF value of the external capacitors C_{PUMPX} and C_{HOLD} has been chosen making a compromise between the capacitance value and the size (0603).

Except the level shifters which are working with 1.6 V output voltage the rest of the circuit is supplied with 0.9 V. The nominal output current for the charge pump is specified to be around 25 mA. The output voltage obtained for this current is 1.6 V. The calculated power efficiency is in the range of 84 % for an optimized clock frequency of 500 kHz.

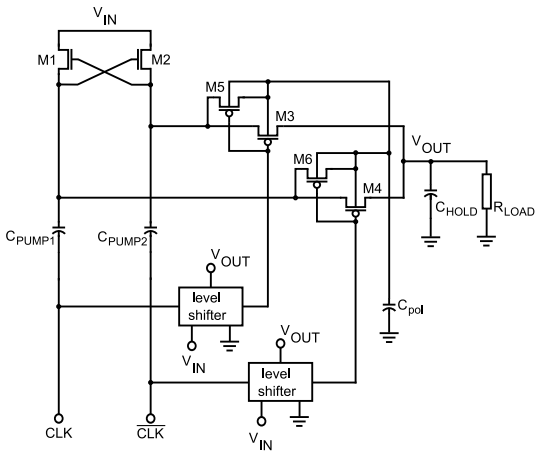

Figure 1: Schematic diagram of the voltage doubler.

Although the power efficiency is not of primary importance, the circuit has been optimized in order to obtain the highest possible efficiency for its nominal output current. Special attention was paid to optimize the W/L ratio of serial PMOS (M3 and M4) switches which can have high impact on the resistive losses in the converter. In order to decrease the R_{ON} of the switches their length was set to minimum value available in IBM 0.13 μm technology, which is 240 nm for thick gate oxide PMOS transistor (120 nm for low V_t NMOS transistor with thin oxide). The width of the switches was optimized using Spectre simulations.

For further improvement of the power efficiency an auxiliary charge pump was added to the main voltage doubler. This charge pump consists of two PMOS transistors M5 and M6 and integrated capacitance C_{POL}. It shares two external capacitances (C_{PUMPX}) with the main voltage doubler as well. Transistors M5 and M6 help to eliminate the effects of vertical bipolar parasitic structures by binding n-wells of main serial switches (M3 and M4) to the high potential. The auxiliary charge pump works without the resistive load which results in its high power efficiency.

The principle of voltage pumping is the following. When CLK signal is in high state ($\overline{CLK}$ is in low state, respectively) transistor M1 is turned off and M2 is turned on. At the same time M3 is turned off and M4 is turned on. Thus the top plate of the capacitor C_{PUMP2} is charged to the supply voltage V_{IN}. In the same time capacitors C_{PUMP1} and C_{HOLD} are connected in parallel. During the second phase (CLK - low and $\overline{CLK}$ - high) the bottom plate of C_{PUMP2} remains at V_{IN} while on the C_{PUMP2} there is still charge equal to $V_{IN}C_{PUMP}$ from the previous phase. This charge is then transferred to the output capacitance (C_{HOLD}).

2) Level shifting

Because of poor driving capability of used big PMOS serial switches (M3 and M4) two level shifters are needed. Fig. 2. shows the schematic of such a level shifter which requires two voltage supply domains: input voltage supply (0.9 V) and output supply (1.6 V) taken from the output of the charge pump. This architecture was proposed by J. Rocha et. Al [3] and Q. A. Khan [4]. The circuit shifts the high state of CLK_{IN} from V_{IN} (0.9 V) to V_{OUT} (1.6 V). Each level shifter consists of eight transistors. All of them, apart from two transistors used in the inverter, are MOS transistors with thicker gate oxide. PMOS transistors M7 and M9 are added to increase the speed of the circuit. In order to reduce current injection to the bulk, triple-well NMOS transistors are used.

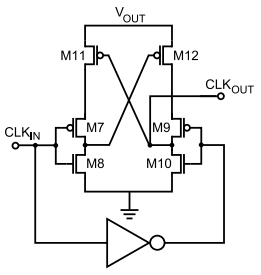

Figure 2: Schematic diagram of the level shifter.

3) Non-overlapping clock generator and buffers.

The clock generator shown in Fig. 3. is a modification of the circuit proposed by L. Pylarinos [5]. In order to obtain better power efficiency it is very important to ensure that the driving clock signals do not overlap. It is possible by using current starved inverters with a current limitation set in this case to 120 μA. Schmitt inverters were also used. Capacitors shown in Fig. 3. are integrated. Their capacitance is as high as 1 pF which is sufficient to separate clock signals.

The clock signals are additionally buffered to drive efficiently large switching transistors. Each buffer consists of a chain of seven scaled inverters. In last five inverters triple-well NMOS transistors were used.

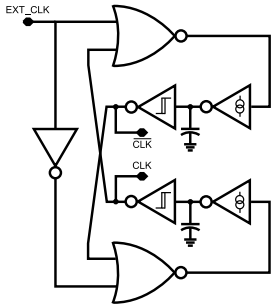

Figure 3: Schematic diagram of the non-overlapping clock generator.

B. Step-down DC-DC converter

1) Architecture and principle of operation

The core of the DC-DC step-down converter [6], [7], [8] is shown in Fig. 4. It is built of four stacked transistors (one PMOS and three NMOS) and three external SMD capacitors with low ESR. The whole circuit is supplied with 2.0 V. The nominal output current is specified to be around 60 mA. The output voltage obtained for this current is in the range of 920 mV. The power efficiency obtained for the nominal current is up to 92 %, but the converter can operate at 100 mA with high power efficiency, even up to 87 %. All CMOS devices used in the design are transistors with thicker gate oxide (5.2 nm) allowing the maximum supply voltage of 2.5 V.

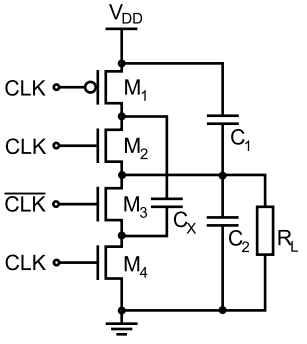

Figure 4: Schematic diagram of the switched capacitor DC-DC step-down converter.

The optimization of the power efficiency of the converter was performed in the following steps. First, the W/L ratio of all switches was optimized. The main goal was to reduce the resistance of the switches by using the minimum length of the transistor channel allowed in the IBM 0.13 μm technology. For MOS transistors working with supply voltage up to 2.7 V the minimum length is 240 nm. In order to reduce the bulk effect and to obtain better power efficiency, triple-well NMOS transistors were used. This solution also allowed us to reduce transistor dimensions. Transistors used in the design are relatively big. In case of M1 the W/L ratio is 8000μm/0.24μm, 4000μm/0.24μm for M2, M3 and 2000μm/0.24μm for M4.

The principle of circuit operation is the following [9]. When CLK is high ($\overline{\mathrm{CLK}}$ is low) transistors M1, M3 are turned off and M2, M4 are turned on. Load current charges the output capacitor $\mathrm{C_1}$. Simultaneously it discharges parallel capacitors $\mathrm{C_2}$ and $\mathrm{C_X}$. In the second phase, when CLK is low ($\overline{\mathrm{CLK}}$ is high) switches M1, M3 are off and M2, M4 are on. The top capacitor $\mathrm{C_1}$ is connected in parallel with flying capacitors $\mathrm{C_X}$. It means that load current charges $\mathrm{C_1}$ and $\mathrm{C_X}$ while discharging the bottom capacitance $\mathrm{C_2}$.

2) Level shifting, buffers and clock generator

Due to the better driving capability of switches, working with lower output voltage, there is no need to use additional level shifters.

Chains of scaled inverters were used as buffers in this design as well. Each buffer consists of four inverters. Similarly to the step-up DC-DC charge pump design triple-well NMOS transistors are used in the inverters. This causes the significant reduction of the current injected into the bulk. The W/L ratio of the PMOS transistor used in the last inverter is 400μm/0.24μm, because there is no need for driving large external SMD capacitors but only the internal gate capacitance of the CMOS switches.

A very simple clock generator proposed by L. Pylarinos [3] is used in the design.

III. Simulation results

A. Step-up charge pump.

The performance of the charge pump was simulated and some of the results are shown in Fig. 5. For the input voltage (dotted line) ramped from 0 V up to 0.9 V within 50 μs the output voltage (solid line) reaches its nominal value of 1.6 V after 70 μs. In Fig. 5(b) output voltage ripple is shown. The output ripple is less than 15 mV p-p, which is acceptable assuming that a linear regulator will follow the charge pump.

The simulations were performed for several clock frequencies. The results are shown in Fig. 6. The efficiency is relatively flat for clock frequencies from 150 kHz to 500 kHz, however for lower frequencies the output voltage ripple is higher. At 500 kHz we have still satisfactory efficiency of 85 % and the ripple is below 15 mV p-p.

Power efficiency is strongly dependent on the output current. This dependence is shown in Fig. 7(a). As it was mentioned before the circuit was optimized to obtain good power efficiency for the nominal output current of 25 mA. For currents higher than 25 mA the power efficiency decreases rapidly due to losses on the resistance of serial PMOS switches M5 and M6 (Fig. 1). The plot shown in Fig. 7(b) indicates a strong dependence of the output voltage on the output current. From this chart one can easily calculate the output impedance of the designed step-up charge pump, which is about 8 Ω.

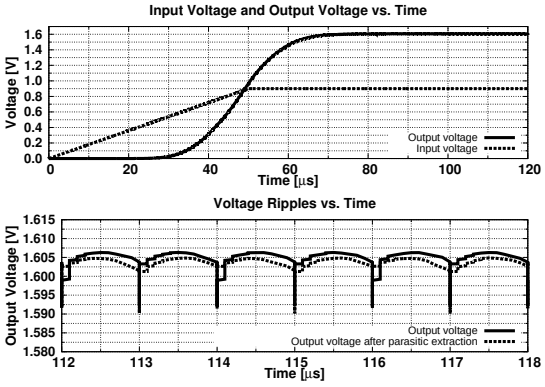

Figure 5: Simulation of step-up response for voltage doubler.

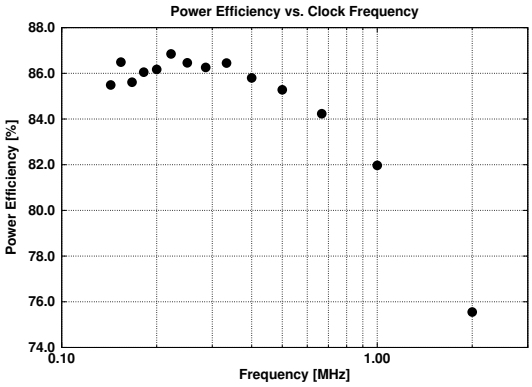

Figure 6: Power efficiency versus clock frequency.

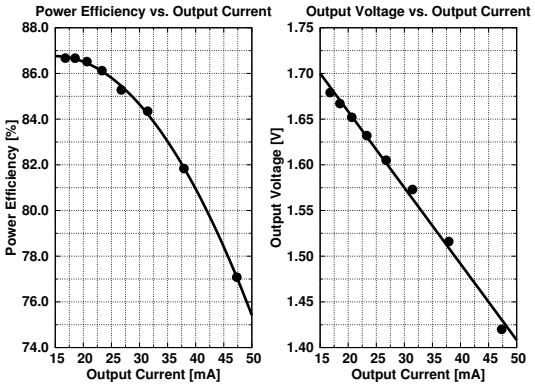

Figure 7: Power efficiency versus output current and output voltage versus output current.

The corner analysis for designed step-up charge pump was

also performed. The results are shown in Fig. 8. For the typical transistor models the power efficiency measured from Spectre simulation was as high as 86 %. For 3 σ fast device characteristics the power efficiency reaches 87 % with an output voltage of 1.65 V. On the other hand, for 3 σ slow device characteristics the power efficiency is still high, 84 %. These results have been obtained by proper optimization of the level shifters, which give better driving capability of PMOS switches.

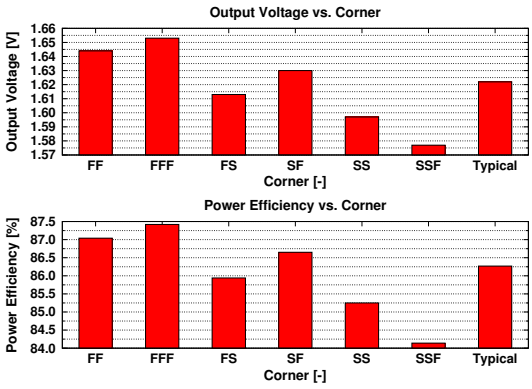

Figure 8: Results from the corner analysis of the voltage doubler (FF – fast-fast, FFS – fast-fast functional, FS – fast-slow, SF – slow-fast, SSF – slow-slow functional).

B. *Step-down DC-DC converter.*

The simulation results of transient analysis for the step-down converter are shown in Fig. 9. Input voltage (dotted line) reaches its nominal voltage of 2.0 V after 5 μs. After about 7 μs, the output voltage (solid line) reaches 0.92 V. The output voltage ripples (shown in Fig. 9(b)) are below 10 mV p-p. The power efficiency calculated from Spectre simulations (for nominal output current of 60 mA) is as high as 92 %.

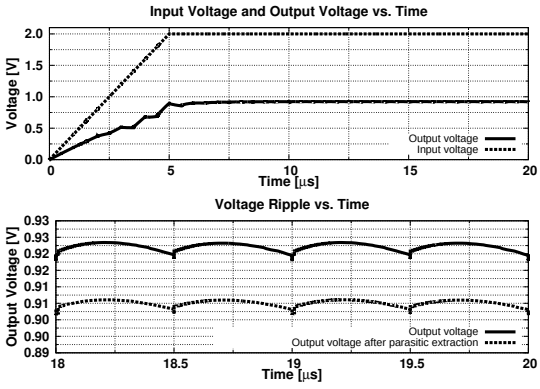

Figure 9: Simulation of step-down response for voltage divider.

The power efficiency is strongly dependent on the output current (Fig. 10). The output impedance calculated from this characteristic is about 1 Ω.

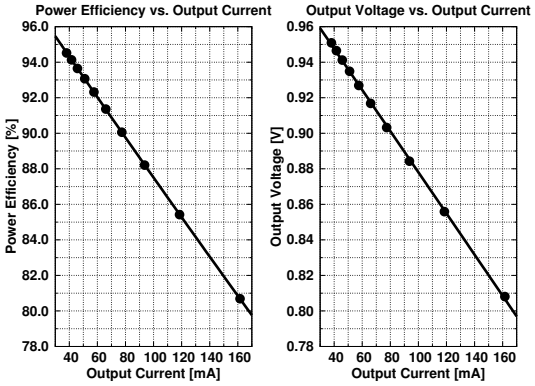

Figure 10: Power efficiency versus output current and output voltage versus output current.

The corner analysis for step-down converter was performed as well. Results obtained from simulations are shown in Fig. 11. The output voltage for the typical parameters is 0.92 V. Even for the 3 σ slow device parameters, the output voltage is above 0.9 V. For typical device models the power efficiency is 92 % but in the worst case it is still above 90 %.

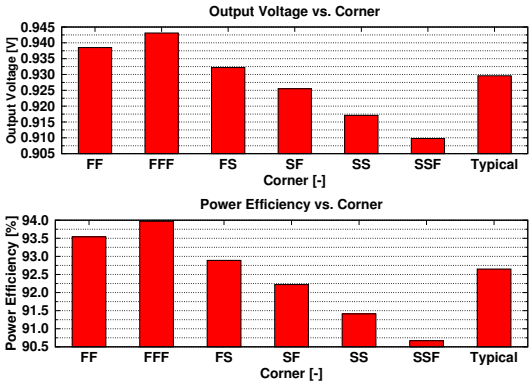

Figure 11: Results from the corner analysis of the voltage divider (FF – fast-fast, FFS – fast-fast functional, FS – fast-slow, SF – slow-fast, SSF – slow-slow functional).

IV. Conclusions

We have elaborated the designs of the DC-DC step-up and step-down converters, which are fully compatible with the 130 nm CMOS technology. A solution has been worked out for the DC-DC step-up charge pump to overcome limitations due to low input voltage. The charge pump uses 3 external capacitors of 470 nF each. The nominal output current is 25 mA and output voltage is 1.6 V. The power efficiency obtained from Spectre simulations is up to 85 % at 500 kHz clock and output ripples below 15 mV p-p

The switched capacitor step-down DC-DC converter is based on the classical structure and uses also 3 external capacitors of 470 nF each. The design has been optimised for switching frequency of 1 MHz. The power efficiency for the nominal

output current of 60 mA and output voltage of 0.92 V is up to 92 %.

In both cases the corner and Monte Carlo simulations were performed. Also layouts of both circuits have been prepared.

V. Acknowledgements

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