An integrated DC-DC step-up charge pump and step-down converter in 130 nm technology

M. Bochenek[1,2], W. Dabrowski[2], F. Faccio[1], J. Kaplon[1]

1) Conseil Européen pour la Recherche Nucléaire (CERN), Geneva, Switzerland
2) Faculty of Physics and Applied Computer Science, AGH-UST, Kraków, Poland

Abstract

After the LHC luminosity upgrade, the number of readout channels in the ATLAS Semiconductor Tracker will be increased by one order of magnitude. Therefore, a new solution for powering the readout electronics has to be elaborated. Two main approaches for power distribution under development are the serial powering of a chain of modules and the parallel powering scheme using DC-DC conversion. In either case switched-capacitor converters on the front-end chips will be needed.

In the serial powering scheme, the 1.2 V clean supply voltage for the analog part of the front-end chip must be produced from 0.9 V digital power supply obtained from shunt regulators. Therefore a linear voltage regulator must follow the step-up converter. Since the current consumed by the analog part is constant and has moderate value (max. 30mA), the optimization of the converter is focused on minimization of the output ripples. In this case, the output impedance and power efficiency is not of primary importance.

In the second possible scheme the digital part of the front-end electronics will be supplied directly from the on-chip DC-DC step-down converter providing 0.9 V. Due to high variations of the digital current consumption during chip operation and keeping in mind that the digital current is the substantial part of the global current in the chip, the main parameters to be optimized are the power efficiency and the output impedance.

We present design study and the implementations in 130 nm technology of two DC-DC on-chip converters.

Architecture of a step-down DC-DC converter

The core of the DC-DC step-down converter shown in Fig. 1 is built of four transistors (one PMOS and three NMOS) and three external SMD capacitors. All transistors used in the design are transistors with thicker gate oxide working with maximum supply voltage of 2.7 V. To reduce the bulk effect and to obtain good power efficiency, triple-well NFETs were used. The whole circuit is supplied with 2.0 V. Due to the better driving capability of switches, working with lower output voltage, there is no need to use any level shifters. The output voltage is as high as 920 mV for a nominal current, which is 60 mA, but the converter can operate at 100 mA with power efficiency up to 88 %.

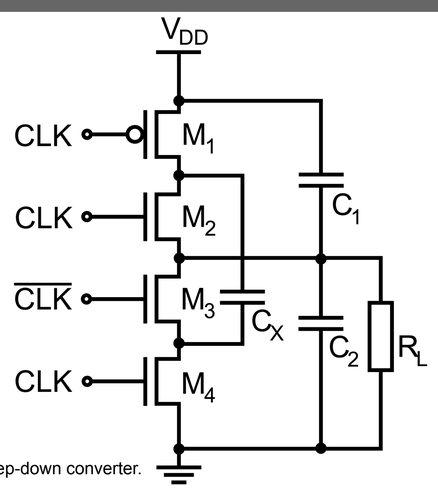


Fig. 1. Switched capacitor DC-DC step-down converter.

Simulation results

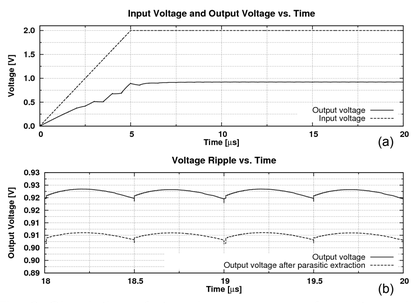


Fig. 2. Simulation of step-down response for voltage divider.

Results from SPICE simulations are shown in Fig. 2. Input voltage (dotted line) reaches its nominal voltage of 2.0 V after 5 µs. After about 7 µs, the output voltage (solid line) reaches 0.92 V.

The amplitude of the output voltage ripples (shown in Fig. 2(b)) is below 10 mV. The power efficiency calculated from SPICE simulations (for nominal output current of 60 mA) is as high as 92 %.

For DC-DC step-down converter a strong dependence of power efficiency on the output current can be observed, as shown in Fig. 3(a). The power efficiency of this converter was optimized for a nominal output current of 60mA.

In Fig. 3(b) the dependence of output voltage on output current is shown. The output impedance calculated from this characteristic is around 1 Ω.

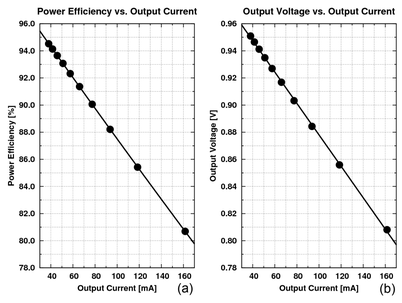


Fig. 3. Power efficiency versus output current (a) and output voltage versus output current (b)

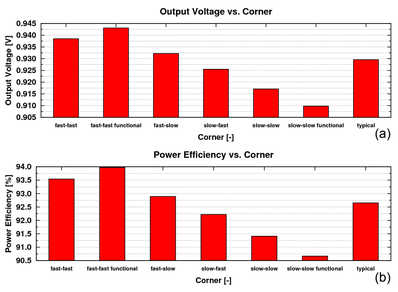
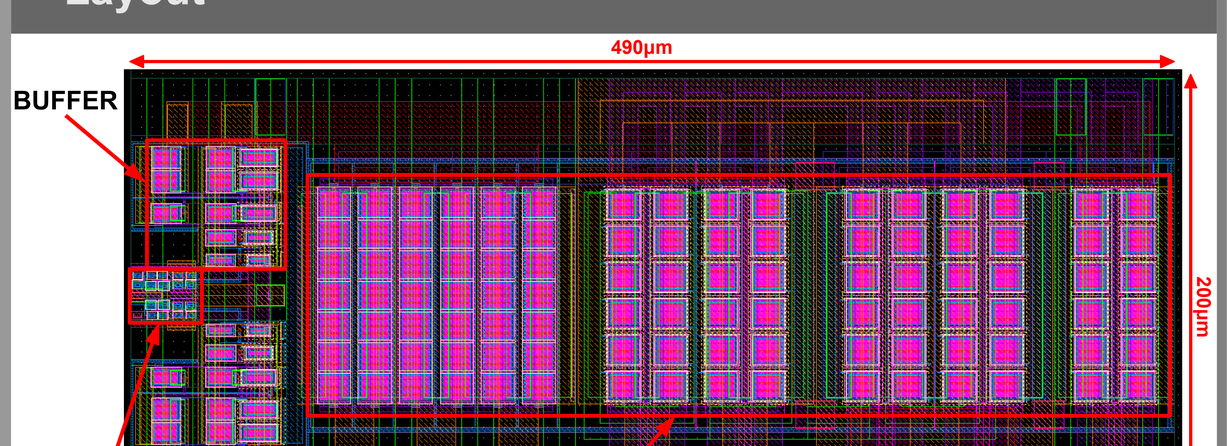


Fig. 4. Results from the corner analysis of the proposed voltage divider.

The corner analysis for step-down converter was performed as well. Results obtained from simulations are shown in Fig. 4. The output voltage for the typical parameters is above 0.93 V. Even for the 3σ slow device parameters, the output voltage is above 0.9 V.

For typical device models the power efficiency is above 92 % and in the worst case, it is still above 90 %.

Layout



Architecture of a step-up charge pump

The switched capacitor step-up charge pump shown in Fig. 5(a) is based on the voltage doubler circuit. The main part of the circuit consists of two cross-coupled NMOS transistors (M1 and M2), four PMOS transistors working as serial switches (M3 – M6), three external SMD capacitors (C_{PUMPX} and C_{LOAD}) and one capacitor integrated on the chip (C_{pol}). The optimized working frequency is around 500kHz.

Due to the poor driving capability of the PMOS serial switches, two level shifters (shown in Fig. 5(b)) are needed. Those voltage shifters require two voltage supplies, the input signal voltage supply (0.9 V) and the output signal voltage supply (V_{OUT} = 1.6 V) taken from the output of the charge pump.

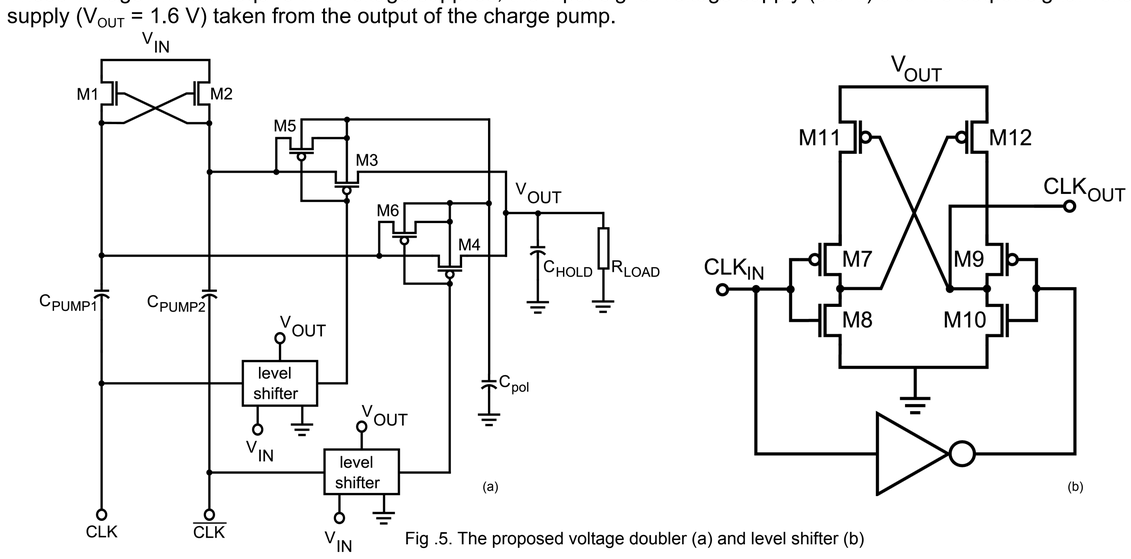


Fig .5. The proposed voltage doubler (a) and level shifter (b)

Simulation results

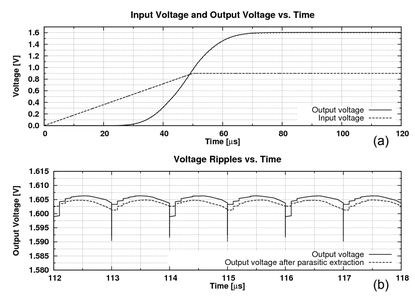


Fig. 6. Simulation of step-up response for voltage doubler.

The performance of step-up DC-DC converter was simulated and the results are shown in Fig. 6(a). Input voltage (dotted line) is rising from 0 V up to 0.9 V within 50 µs. The output voltage (solid line) reaches its nominal value of 1.6 V after 70 µs.

The output voltage ripples amplitude is less than 15 mV, which is acceptable for the linear regulator to be used.

The power efficiency calculated from post-layout SPICE simulations is up to 86 %.

Power efficiency is highly dependent on the output current. This dependence is shown in Fig. 7(a). The circuit was optimized to obtain high power efficiency for the nominal output current of 25 mA. For currents higher than 25 mA the power efficiency is decreasing rapidly due to the resistance of serial PMOS switches M5 and M6. The plot shown in Fig. 7(b) indicates the high dependence of output voltage on output current. From this chart, one can easily calculate the output impedance of the designed step-up charge pump, which is below 8 Ω. This resistance is crucial for obtaining a good power efficiency of the device.

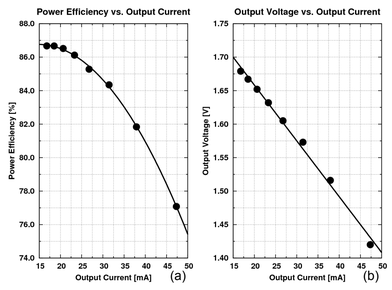


Fig. 7. Power efficiency versus output current (a) and output voltage versus output current (b)

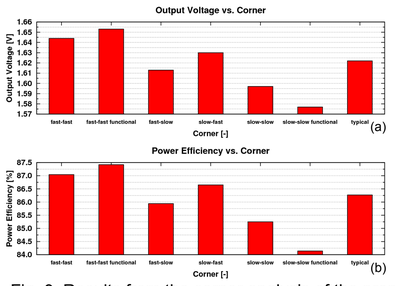
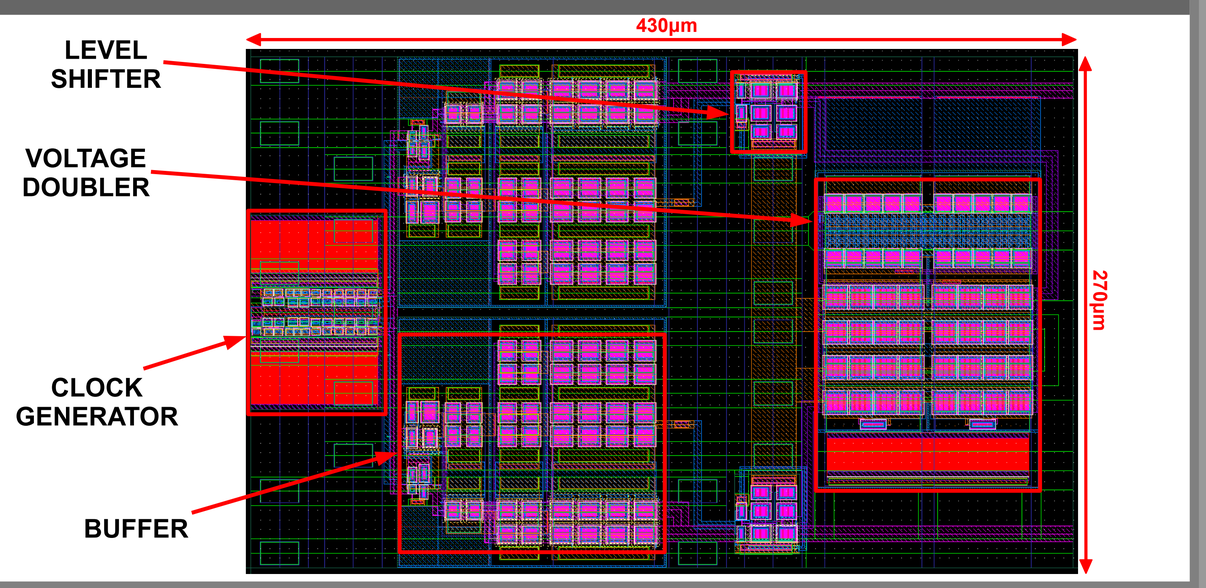


Fig. 8. Results from the corner analysis of the proposed voltage doubler.

The corner analysis for designed step-up charge pump was also performed. The results shown in Fig. 8 are very promising. For the typical model of transistors, power efficiency measured from SPICE simulation was as high as 86 %. For 3σ fast device characteristics the power efficiency reaches 87 % with an output voltage of 1.65 V. On the other hand, for 3σ slow device characteristics the power efficiency is still high – 84 %. These results have been obtained by proper optimization of the level shifters, which give better driving capability of PMOS switches.

Layout



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