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An integrated DC-DC step-up charge pump and step-down converter in 130 nm technology

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After the LHC luminosity upgrade the number of readout channels in the ATLAS Semiconductor Tracker will be increased. Therefore a new solution for powering the readout electronics has to be found.

The two main approaches for power distribution are under development, the serial powering of a chain of modules

Summary

The High Luminosity Upgrade sets very demanding requirements on the granularity of the ATLAS Inner Detector resulting in an increase of the number of readout channels. Therefore two new approaches for power distribution are currently under development, the serial powering of a chain of detector modules and the parallel powering with DC-DC conversion on the modules.

In the serial powering schema, the chain of modules is powered from a current source, while the voltage is stabilized by the shunt regulator integrated on each readout chip. This solution improves overall power efficiency of the system by significant reduction of the number of power cables. There are several possible options for power management on the module level in the serial powering schema. Some of them require switched capacitors DC-DC converters integrated in the readout chips.

In the parallel powering option the modules are supplied from a high voltage source and the voltage is then reduced in DC-DC converters mounted of each module. In case of two-stage DC-DC conversion scheme a switched capacitor DC-DC converter can be integrated in the readout chip.

In the paper we present two designs of switched-capacitor DC-DC converters, a step-up charge pump and step-down

The switched capacitor step-up charge pump is based on the voltage doubler concept. The main part of the circuit consist of two low threshold voltage, cross-coupled NMOS transistors, four thick oxide PMOS transistors working as serial switches and four capacitors including three external SMD and one fully integrated on the chip. The circuit works at 500 kHz frequency and pump voltage on both clock edges. For the input voltage of 900 mV, it delivers an output voltage of 1.6 V at the output nominal current. The power efficiency extracted from SPICE simulations is up to 84%. To eliminate the effect of parasitic vertical bipolar transistors an auxiliary charge pump was added. It allows the bulk of PMOS serial switches to be put on the highest potential. Further improvements are related to switching capability, which can be significantly increased by adding a level shifter circuit.

An optional solution assuming input voltage of 2.0 V and a step-down DC-DC converter is considered as well. The core of the circuit is built of four transistors with thick gate oxide and three external SMD capacitors. The whole circuit is supplied with 2.0 V. Due to the better driving capability of the switch working with lower output voltage there is no need to use any level shifters. The output voltage is as high as 920 mV for nominal current which is 60 mA. The power efficiency calculated from SPICE simulations is up to 92%.

The power efficiency of different powering systems and different power management options in the readout chips will be estimated based on an analytical model including the parameters of the power cables, linear regulators integrated in the readout chips and expected supply voltages, and the power consumption of the readout chips in 130 nm technology.

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