Construction and Performance of a Double-Sided Silicon Detector Module Using the Origami Concept

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Abstract

The APV25 front-end chip with short shaping time will be used in the Belle II Silicon Vertex Detector (SVD) in order to achive low occupancy. Since fast amplifiers are more susceptible to noise caused by their capacitive input load, they have to be placed as close to the sensor as possible. On the other hand, material budget inside the active volume has to be kept low in order to constrain multiple scattering.

We built a low mass sensor module with double-sided readout, where thinned APV25 chips are placed on a single flexible circuit glued onto one side of the sensor. The interconnection to the other side is done by Kapton fanouts, which are wrapped around the edge of the sensor, hence the name Origami. Since all front-end chips are aligned in a row on the top side of the module, cooling can be done by a single aluminum pipe.

The performance of the Origami module was evaluated in a beam test at CERN in August 2009, of which first results are presented here.

I. INDRODUCTION

The Belle Detector [1] is located at the interaction point of the KEK B-factory (KEKB), a low-energy but high luminosity asymmetric electron-positron collider in Tsukuba, Japan [2]. The energies of KEKB are 8 GeV for e^- and 3.5 GeV for e^+, respectively. Since its inauguration in 1999 the luminosity of the collider was increased continuously and reached a new world record of $2.11 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$ in June 2009.

A major upgrade of the KEKB and the Belle detector (Belle II) is foreseen until 2013/2014. The target luminosity is $8 \times 10^{35}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$, which is about 40 times the present value. Accordingly, a similar increase of background at the interaction region is expected. This leads to significant increase of the occupancy of the silicon vertex detector (SVD), which is currently about 10% for the innermost layer and thus already at the limit with respect to track finding. Moreover, the trigger rate will rise from 450 Hz to up to 30 kHz (10 kHz in average). In the present vertex detector (SVD2) [3], the sensors are read out by VA1TA [4] front-end chips. The VA1TA is operated at only 5 MHz and has a sample-hold circuit, which is blocked during read out. Since this would lead to an enormous dead time, it is clear that the VA1TA can not be used at such high trigger rates. Both issues, occupancy and dead time, can be solved by using a front-end chip with shorter shaping time, faster readout clock and integrated pipeline for the Belle-II silicon vertex detector (SuperSVD) readout.

II. APV25

The APV25 front-end chip, originally developed for CMS at CERN, was identified to fulfill the requirements of the SuperSVD not only in terms of occupancy and dead time, but also concerning radiation hardness. Due to its shaping time of 50 ns an occupancy reduction by a factor of 12.5 can be achieved compared to the VA1TA with 800 ns shaping. This factor not only results from the quotient of the peaking times, which is 16, but also considers measured shaper waveforms of the chips as well as thresholds. Moreover, the APV25 offers a so called *multi-peak mode*, which allows to read out six consecutive samples of the shaper output. By processing this data with FPGAs, the actual hit timing can be determined with a precision of few nanoseconds, hence resulting in an additional occupancy reduction [5, 6]. Thanks to the clock frequency of 40 MHz and an 192 cells deep analog pipeline, the APV25 can be read out continuously up to a trigger rate of about 50 kHz without appreciable dead time.

Unfortunately, faster shaping comes along with a higher susceptibility to noise, but robust tracking requires high spatial resolution and thus in practice a minimum cluster signal-to-noise ratio (SNR) of ten. The cluster SNR is given by the sum of cluster signals divided by the square sum of RMS noise of all strips in the cluster. Since the signal is limited by the sensor thickness ($300\mu\mathrm{m}$), it is nessesary to minimize noise. The noise figure of the APV25 is given by $ENC = 250\,\mathrm{e} + 36\,\mathrm{e/pF}$ and thus worse then that of the slow VA1TA, for which it is $ENC = 180\,\mathrm{e} + 7.5\,\mathrm{e/pF}$. There is no possibility to reduce the constant term of this equation, but the second one is proportional to the capacitive input load of the chip, which is mainly given by the sensor geometry and the length of the interconnections between sensor and readout chip. Since the geometry is defined by physics requirements, the only way to reduce the capacitive load and thus ensure high SNR is to place the APV chips as close as possible to the sensors.

III. LADDER DESIGN

The current SVD2 is composed of four layers of 4 inch double sided silicon detectors (DSSD). From the first to the fourth layer, it consists of cylindric arranged ladders with 2, 3, 5 and 6 DSSDs, respectively. The radius of the innermost layer is 20 mm, that of the outermost is 88 mm. Since KEKB is a low energy machine and thus multiple scattering has to be considered with respect to vertex resolution and tracking efficiency, material budget in the sensitive area is an important issue. Therefore, in SVD2 up to three sensors were concatenated

(ganged) and commonly read out by hybrids located outside of the acceptance region at the edge of each ladder. Fig. 1 shows a photograph of all four ladder types. As all ladders are readout by the same numbers of hybrids, this scheme further reduces the number of readout channels, but also creates ambiguities, which have to be resolved by the tracking algorithm.

Figure 1: The ladders of all four layers of the present Belle Silicon Vertex Detector (SVD2). In the ladders of the outermost layer, three sensors are ganged and read out by hybrids on either side.

On the other hand, sensor ganging significantly increases the capacitive load of the readout chips. As described in section II., this is no problem in case of SVD2 because of the moderate peaking time and thus low noise figure of the VA1TA chip. However, the situation looks different in case of SuperSVD and AVP25, where the resulting high capacitive load of ganged sensors would be to high. In the past we built a prototype module using two 4” DSSDs read out by four APV25 chips on each side. Aiming to compare the SNR of a single and two ganged sensors, we concatenated 384 of the 512 strips on each side, so that one of the APV chips on each side is only connected to a single sensor.

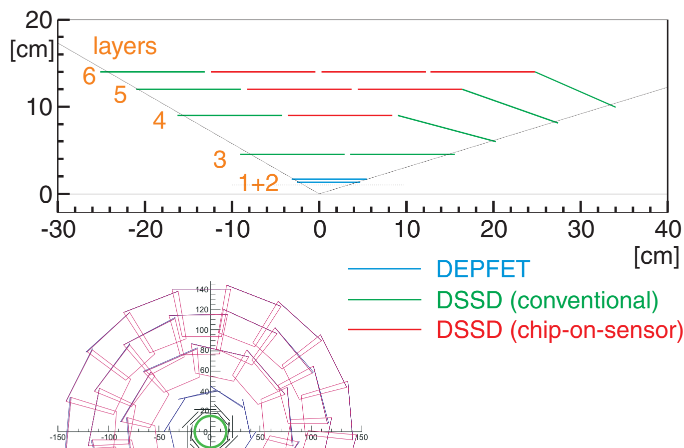


Figure 2: Tentative layout of the SuperSVD with two DEPFET pixel layers surrounded by four cylindrical DSSD layers. The green sensors are read out conventionally, the red ones use the Origami chip-on-sensor concept.

Measurement results had shown, that even ganging of two 4” sensors leads to a poor cluster signal-to-noise ratio of 10 (n-side) or below (p-side), depending on the pitch, while the values of a single sensor are reasonable [8]. Hence ganging of two ore more detectors is not an option with fast shaping.

Furthermore it has to be considered that the SVD in Belle II will extend to a radius of 140 mm. As shown in fig. 2, it will again consist of four cylindrical layers of double-sided silicon sensors and two additional DEPFET pixel [7] layers in the innermost region, hence the SuperSVD will have six layers in total. Since the length of the ladder and thus also the number of sensors and readout channels, respectively, increases with the radius, sensors made of 6” wafers are prefered.

In order to achieve reasonable SNR and thus a good spatial resolution, each sensor will to be read out individually by four or six APV25 chips per side, depending on its pitch and location. In case of the innermost layer, but also the sensors located on the edges of layer 4 to 6, this can be be done using conventional hybrids mounted outside the acceptance. The inner sensors will be read out by hybrids following the Origami chip-on-sensor concept, which will be described in the next section.

IV. Origami Chip-on-Sensor Concept

As a conclusion of the discussion about fast shaping and sufficient signal-to-noise ratio it is obvious that the APV25 chips have to be placed as close as possible to the sensor strips, leading to a chip-on-sensor concept. This means that the readout chips together with the hybrid circuit sit on the top of the sensor in order to minimize the length of the fanouts. Using such a concept allows to read out a single side of a DSSD. In 2006 we built a prototype module based on this scheme, where the short strips of a 4” DSSD (n-side) were read out by APV25 chips located on a hybrid made of a double-layer Kapton circuit [8] separated from the sensor by a sheet of rigid foam called Rohacell [9]. The module was tested in several beam tests, where it showed excellent performance. The achieved SNR was about 18 and thus significantly higher than that of modules using the same sensor but conventional read out.

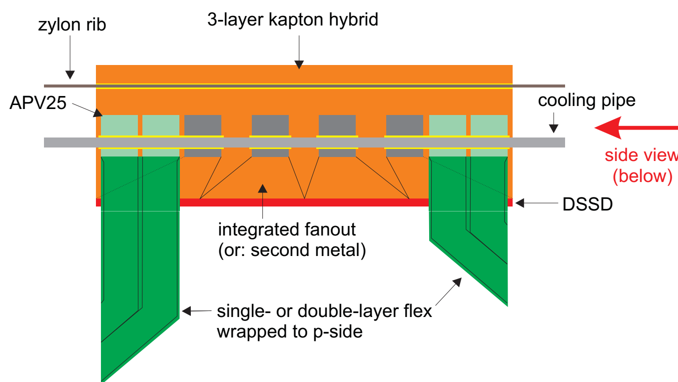
Keeping the material budget in mind, there was the question how it is possible to extend this chip-on-sensor concept to double-sided readout without doubling everything.

The solution is the ”Origami chip-on-sensor concept”, which we already presented earlier [8]. Nevertheless, we will briefly describe this idea here. Fig. 3 shows drawings of top and side views of an Origami chip-on-sensor module. In that scheme, the APV25 chips of both sides are placed on a single flexible circuit, mounted onto one side of the sensor. This flex-hybrid is made of only three copper layers and contains integrated pitch adapters to connect the strips on the same side as the hybrid. The channels of the opposite side are attached by small flexible fanouts wrapped around the edge of the sensor, hence the name Origami. All connections between flex pieces, sensor and APV chips are made by wire bonds. The depicted design is indented for a 4” DSSD with 512 strips on both sides, each read out by four APV25 chips, respectively.

Thermal and electrical insulation between hybrid and sensor is given by a 1 mm thick layer of low mass, but rigid foam (Rohacell). Nevertheless, sufficient cooling of the APVs is required,

since the power dissipation of each chip is about 350 mW. By testing several cooling options using a thermo-mechanical mockup of a future SVD ladder, liquid cooling was identified to be the only feasible solution [8] and thus foreseen in the concept. Arranging all front-end chips in a row allows cooling by a single aluminum pipe, that eventually can also be used as a mechanical support, together with a zylon rib, which is foreseen in longitudinal direction. The mechanical structure of the concept is held very simple and mainly based on the design of the present SVD ladders. A detailed study, which also addresses the stability of a whole ladder as well as thermal issues, has been started recently.

a) Top view:



b) Side view (cross section):

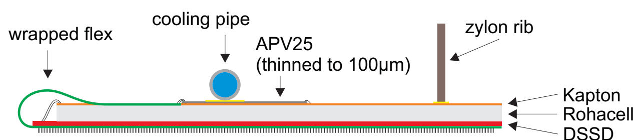


Figure 3: Top and side views of the Origami chip-on-sensor concept for a 4" DSSD. Both are dimensional, but on a different scale. a) Top view: The four APV25 chips which read out the strips on the opposite side are shown in green for clarity and the flex pieces to be wrapped around the edges are straightened out. b) Side view: The wrapped flex, which connects the strips of the bottom side, is located at the left edge.

It is clear that using such a hybrid inevitably increases the material budget in the sensitive volume, but there is no alternative solution, particularly in the outer layers, to ensure reasonable SNR with fast shaping. To achieve lowest possible material budget, the APV chips will be thinned down to approximately 100 μm. However, the calculated average material budget is about 0.72 $\% X_0$ and thus about 1.5 times that of the conventional design, but offering a significant improvement of signal-to-noise ratio.

V. APV THINNING

The APV25 is about 300 μm thick, but its active electronics is only in the surface. We plan to thin it down to 100 μm in order to minimize the material budget of the Origami modules. Since this was never tested in the past, we sent one wafer with 319 good dies to the French company EDGETEK/WSI, for thinning and dicing. We received 314 good dies with a thickness of 106 μm in average. Only 5 pieces were lost, corresponding to a yield of 98.4%. We randomly took 16 of them to equip 4 (conventional) hybrids. Moreover, we also assembled one hybrid with normal (unthinned) APVs for comparison. Electrical tests of all five hybrids have shown that there is no measurable difference with respect to signal quality and noise of both thinned and normal APV25 chips, respectively. Hence, we conclude that we can actually use thinned chips.

VI. PROTOTYPE ASSEMBLY

In order to show that our idea is in principle feasible, we built the first fully functional prototype of an Origami chip-on-sensor module. Therefore we used the same 4" DSSD from Hamamtsu, Japan, as for the prototype modules described in sections III. and IV.

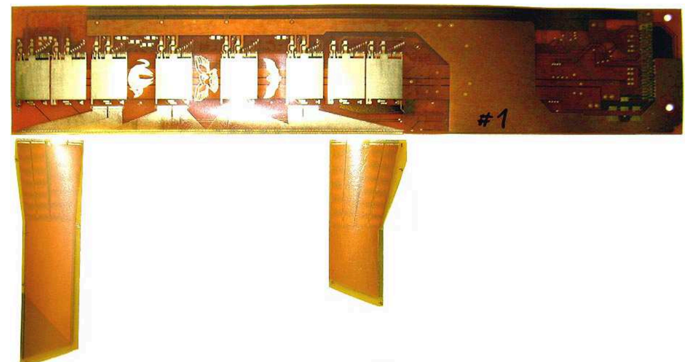


Figure 4: An Origami hybrid and the two flex fanouts.

We started with designing the layout of the three flex circuits, which were later produced by the CERN PCB workshop. An image of the final flex pieces is shown in fig.4. The hybrid is composed of only three copper and two Kapton layers with thicknesses of 10 μm and 25 μm, respectively. The component layer as well as the bonding pads of the fanouts are gold-plated. With respect to the design rules of the PCB workshop, both fanouts as well es the pitch adapters on the hybrid were implemented in a staggered 2-layer design.

A. Attaching Flexes on Bottom Side

Assembling an Origami module requires about 12 steps in total from which the most interesting or critical ones will be described here. First of all, the two flex fanouts were glued onto the sensor side with the long strips, which later becomes the bottom side of the module. Therefore a two component epoxy paste adhesive (Araldite 2011) was used. The sensor was placed on a custom jig (jig1) with a porous stone inlay and held by vacuum. At this point, precise alignment of the flexes against the bonding pads of the sensor and the hybrid is very important. To adjust the distance between the two flexes we used a dummy prototype of the hybrid (fig. 5). Since this is not suitable for serial production, more precise alignment tools should be used instead.

Figure 5: Gluing of the flexes onto the bottom side (long strips) of the DSSD. The pieces are aligned against the bonding pads of the strips and a sample origami hybrid (top left) using a microscope.

After curing of the glue, wire-bonding between sensor and flexes is the next and also the last task, which has to be performed on this sensor side. In order to flip the sensor and the flexes, a second very similar jig (jig2) was stuck onto the first one with three alignment pins. Once the whole thing (both jigs and the module) is turned over and vacuum is switched to jig2, jig1 can be removed.

B. Hybrid Assembly

In parallel to A. we equipped the hybrid with all passive electronic components, glued it onto the Rohacell foam, attached the APV chips and did wire-bonding of the power and control lines of the APV25s. Then we performed the first electrical tests and found several open vias in the Kapton hybrid, which could mostly be repaired by soldering of thin wires. Lately, we found out that the broken vias were caused by a failure during hybrid production (the vias were not entirely filled with metal), which should not occur again in future. In the end 7 of 8 APV25 chips worked well. We performed an internal calibration run with excellent results. The last chip still had a broken via in one of its two differential output lines, which could not be repaired. Afterwards the hybrid was glued onto the the sensor and aligned to the bonding pads of both sensor and fanouts, respectively (fig. 6), followed by wire-bonding between sensor and the pitch adapters of the top-side APVs.

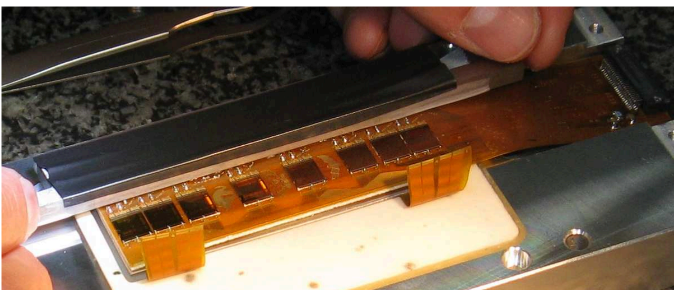


Figure 6: The Origami hybrid after it was glued onto the top side of the sensor. A piece of metal is put onto it to press it down during curing of the glue.

C. Bend and Glue Fanouts

Initially we thought that bending of the fanouts around the edge of the sensor without damaging underlying wire bonds of the top-side will be the most critical task. Thanks to using a micro-positioner with a custom vacuum nozzle, this task was fairly easy. This tool is depicted in fig. 7 and allows very precise positioning as well as lowering of the the fanout and moreover was used to hold the pieces in place while the clue was curing. Afterwards the input channels of all APV chips where connected to their pitch adapters by wire bonding.

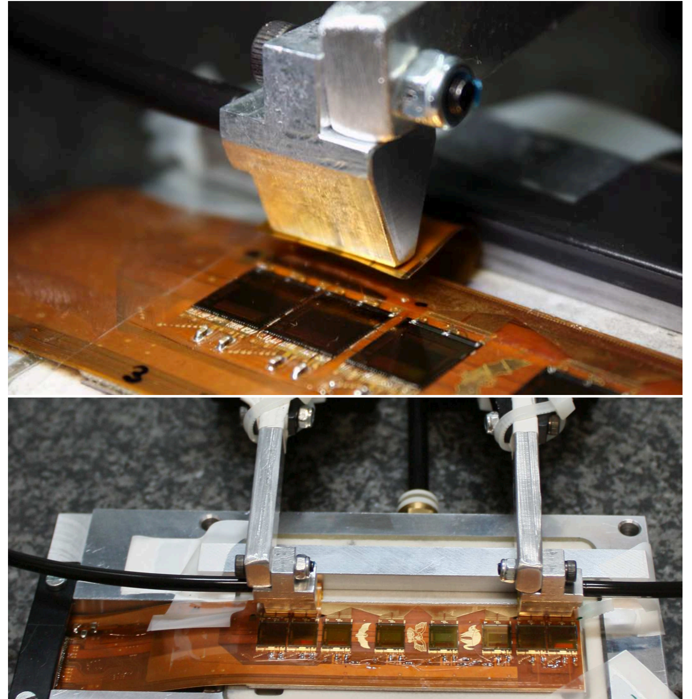


Figure 7: Bending and positioning of the flex fanouts using a custom vacuum tool attached to a positioner, which is normally used for probe needles.

D. Attaching Cooling Pipe and Frame

One of the remaining tasks was to attach the cooling pipe onto the front-end chips. The area of the preamp/shaper of the APV25 has been identified as the region with the highest power dissipation by measurements with an infrared camera. In order to maximize cooling efficiency, this location was chosen to attach the cooling pipe. Since the chips of both top and bottom sides reside at the voltage potential of that side of sensor to which they are connected, i.e. ± 40 V, a thin electrically insulting but thermally conductive foil is placed between the chips and the pipe together with heat-conductive paste. Moreover, the cooling pipe is slightly flattened to improve the thermal contact. The connection to the cooling system (chiller) is done by two fittings located on either end of the pipe.

Finally, the mechanical support was attached and the module was built into a frame for beam tests. For availability reason we used a 5 mm high rib made of epoxy rather than Zylon as support structure of the prototype module. A photograph of both sides of the final module is shown in fig. 8.

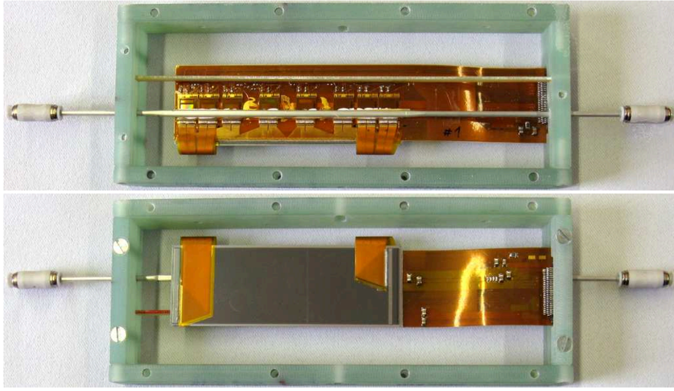


Figure 8: Top and bottom views of the final Origami module, built into a frame for beam tests.

VII. Beam Test Performance

In August 2009 we performed a beam test at the CERN SPS beam line, where the Origami prototype module was tested together with other, already well tested, Belle DSSD prototype modules for comparison. The beam was a mixture of pions, protons and kaons at 120 GeV/c. The Origami module has been operated for several hours both with and without cooling, respectively, were it has shown excellent performance. For cooling we used a chiller and distilled water at a temperature of 13°C, chosen to be slightly above the dew point to avoid condensation.

	w/o cooling		w/ cooling	
Side:	top	bottom	top	bottom
Cluster SNR:	16.7	11.5	18.5	12.8

Table 1: Cluster SNR of the Origami prototype module without and with cooling, respectively.

As shown in tab. 1 a signal-to-noise ratio of about 16.7 was achieved for the top-side, which has the short strips, without cooling. Due to the narrow pitch as well as both the longer strips and larger fanouts, the result for the bottom side (p-side) is slightly worse, but still above ten. Anyhow, considering the results of the reference modules, we observed that the noise level of the whole system was about 10% higher than in our previus beam tests, caused by a cabling failure resulting in a ground loop. That means, with correct system cabling, slightly better values can be expected. Moreover, tab. 1 shows, that cooling leads to about 10 percent improvement of the signal-to-noise ratio of.

We further applied a hit time finding algorithm [8] to the data and compared the results to that of previous beam tests. The results of this analysis are plotted in fig. 9. It is clearly visible, that the present results (red crosses) and particularly that of the Origami module (red dots), are showing similar precision than previous measurements (gray crosses).

VIII. Summary and Outlook

Motivated by the Belle II upgrade, we developed the Origami chip-on-sensor concept, allowing to read out both sides of a DSSD by APV25 chips using a single flexible circuit, sitting on the top-side of the sensor. This concept renders both low material budget and short connections between sensor and the front-end chips in order to ensure sufficient signal-to-noise ratio at fast shaping. A prototype using a hybrid composed of a flexible 3-layer Kapton circuit and a 4” DSSD was built and successfully tested in a beam.

Recently, we started to design the mechanical structure of the future Belle II SVD, aiming to build a complete prototype ladder of its outermost layer using 6” sensors and an enhanced Origami based readout.

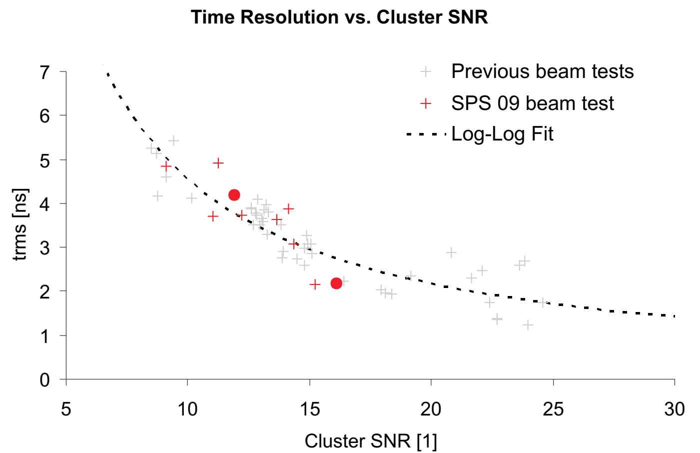


Figure 9: Time resolution in relation to signal-to-noise ratio of various Belle II prototype modules, measured at several beam tests.

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[9] Rohacell (`http://www.rohacell.com`) is a rigid type of styrofoam produced by Degussa.

[10] Zylon (`http://www.toyobo.co.jp/e/seihin/kc/pbo/`) is a stiff, but light-weight material made by Toyobo.