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Thin, Fully Depleted Monolithic Active Pixel Sensor with Binary Readout based on 3D Integration of Heterogeneous CMOS Layers

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On the way towards fast, radiation tolerant and ultra thin CMOS sensors, we propose new generation of devices based on commercial availability of vertical integration of several CMOS wafers (3D Electronics). The proposed prototype device is a 245x245 pixel array with a pitch of 20 μm, In the first silicon layer charge sensing diode and the input buffer amplifiers are integrated, using 0.6 μm CMOS on high resistivity epitaxial wafers. Following stage of processing electronics (charge integration, time invariant shaping and signal discrimination), are placed in the second silicon layer (0.13 micron CMOS). Third layer (same 0.13 CMOS) is used for implementation of fast, digital (binary) readout.

Summary

A On the way towards fast, radiation tolerant and ultra thin CMOS sensors, we propose new generation of devices based on commercial availability of vertical integration of several CMOS wafers (3D Electronics). In this process, each wafer is thinned down to less than 10 microns end equipped with through-silicon vias (TSV) allowing for electrical interconnection between wafers at very small pitch (few microns) and with minimum material budget. The proposed prototype device is a 245x245 pixel array with a pitch of 20 μm, providing active area of 5x5 mm2. In the first silicon layer charge sensing diode and the input buffer amplifiers (source follower in this case) are integrated, using 0.6 μm CMOS process on high resistivity epitaxial wafers. Pioneering application of such substrate which is fully depleted at less than 5V for particle tracking sensors results in higher signal seen at the seed pixel, reduces strongly cluster multiplicity and in particular, due to fast charge collection (<5ns), improves radiation hardness with respect to non-depleted CMOS MAPS by at least order of magnitude. Outputs of first layer buffer amplifiers are vertically coupled (through poly-poly capacitor) to the following stage of processing electronics (charge integration, time invariant shaping and signal discrimination), placed in the second silicon layer (0.13 micron CMOS). For this stage we have chosen a "shaperless front-end"(SFE) structure already fabricated in similar 0.13 μm process, tested and evaluated. Expected equivalent noise charge (ENC) is less than 15 electrons, for a pulse peaking time of about 500 ns, voltage gain at the discriminator input of 150 μV/e (300 μV/e for the second versions) and for total (analog) power dissipation of ˜5μW/pixel. In connection with fully depleted, 14 μm thick epitaxial substrate as a charge sensing layer, this brings very comfortable signal-to-noise ratio of more than 40 for detection of minimum ionizing particles. Third silicon layer (also 0.13 micron CMOS) is used for implementation of digital (binary) readout, with a fast, data driven, self-triggering data flow. The idea is to read in less than 2 μs the X and Y projection of a hit pattern, following a trigger signal set by the first hit pixel. In addition to the presented sensor, other pixel structures have been submitted for production at the same time, aiming testing of different, more power efficient solutions for analog processing (rolling-shutter architecture and novel, very high gain (1-2 mV/el) and low power (<1μW/pixel) time invariant amplifier-discriminator). Integrated three silicon layer stack described above can be in principle thinned down to less than 50 μm, still keeping full sensor functionality and quality. This may pave a way for the construction of new generation of high precision vertex detectors.
Details of the proposed design (recently submitted for fabrication) and preliminary test results will be presented. Possible extensions and applications will be discussed.

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