Total dose effects on deep sub-micron SOI technology for Monolithic Pixel Sensor development

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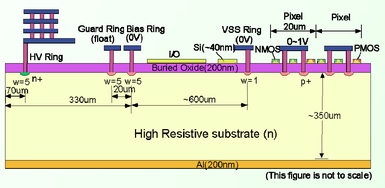
Monolithic pixel detectors in 0.20µm Silicon On Insulator (SOI) technology have been developed, realized and characterized. This work shows the decisive effect of the substrate bias condition during irradiation on the total dose damage of the electronics.

SOI technology for monolithic pixel sensors:

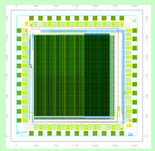
- In the SOI technology CMOS electronics is implanted on a thin silicon layer on top of a buried oxide (BOX): this ensures full dielectric isolation, small active volume and low junction capacitance (higher latch-up immunity, lower power consumption, higher speed applications)



[Y. Arai, KEK]

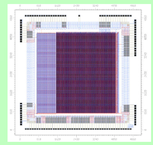
- OKI (Japan) provides 0.15µm and 0.20µm Fully Depleted (FD) SOI processes with **high-resistivity substrate** (700 Ω·cm) and **vias** etched through the oxide which contact the substrate from the electronics layer, so that pixel implants can be created and a reverse bias can be applied.
- Only results on 0.20µm process are shown in the poster, as this process is optimized for low leakage currents and will be used for the development of future detectors.

Chip production:



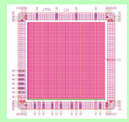
SOI-1 (2007)

- 0.15µm OKI FD-SOI technology
- 160×50 digital pixels (10×10µm²)
- 160×100 analog pixels (10×10µm²)
- MIPs detection
- First radiation damage tests



SOI-2 (2008)

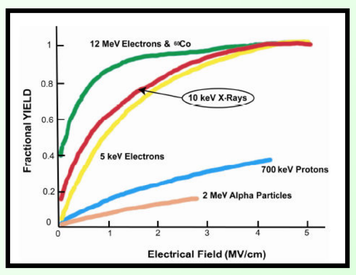
- 0.20µm OKI FD-SOI technology
- 128×172 digital pixels (20×20µm²)
- 40×172 analog pixels (20×20µm²)
- Optimized for low leakage current
- Currently under test



SOI-2-IMAGER (2009)

- 0.20µm OKI FD-SOI technology
- 256×256 analog pixels (13.75×13.75µm²)
- 4 analog outputs
- 5mm chip, 3.2mm active
- Just delivered

Fractional Yield:



- When exposed to ionizing radiation, electron-hole pairs are created inside the thick oxide.
- If a depletion voltage is applied to the detector (substrate), a strong electrical field is present inside the BOX.
- **The electron-hole pairs escaping recombination (fractional yield) lead to *positive charge trapping* throughout the BOX and consequently to an increase of the top-gate leakage current.**

THE TOTAL DOSE DAMAGE ON THE TRANSISTOR STRONGLY DEPENDS ON THE BIAS GIVEN TO THE SUBSTRATE DURING IRRADIATION

Total dose tests:

The X-ray irradiation facility installed at the INFN National Laboratory of Legnaro (Padova, Italy) and used for the total dose damage studies described in this poster is the Seifert Rp-149 Semiconductor Irradiation System

X-ray machine:

- Tube with **W** (7.4-12.06 keV L-lines) anode.
- Maximum tube voltage 60 kV. Maximum tube current 50 mA.
- X,Y (motorized) and Z (manual) axis for accurate position setting of the tube.
- Irradiation in air at room temperature.
- Dose rate: 165rad(SiO_2)/sec.

Test structures:

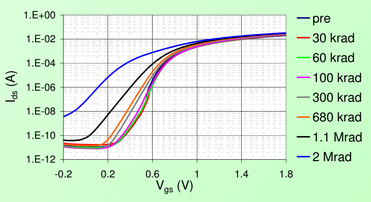
- OKI 0.20µm FD process
- 16 NMOS and 16 PMOS transistors with source in common, gate and drain separated
- ***Each transistor is surrounded by 1µm PSUB guard ring***
- Both Body floating and Body Tie transistors
- W/L = 500
- Normal, Low, High Voltage Threshold

Bias conditions during irradiation:

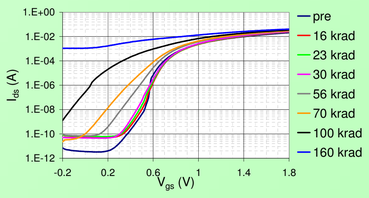
- NMOS and PMOS Body of Body Tie transistors at 0V.
- Drain and source at 0V, gate NMOS HIGH (1.8V), gate PMOS LOW (0V).
- Substrate bias voltage (V_{back}) :
  - V_{back} = 0V, 5V, 10V with PSUB guard-ring floating
  - V_{back} = 10V with PSUB guard-ring at 0V (is the PSUB guard-ring effective in containing the electrical field through the BOX?).

NMOS transistor: (L = 0.50µm, W = 250µm, Normal V_{thr}, Core transistor, Body Tie) for four different bias conditions:

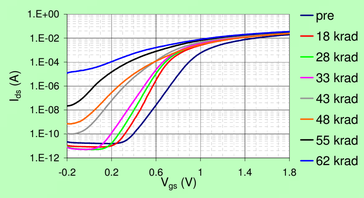
V_{back} = 0V (PSUB guard-ring Floating)



V_{back} = 5V (PSUB guard-ring Floating)

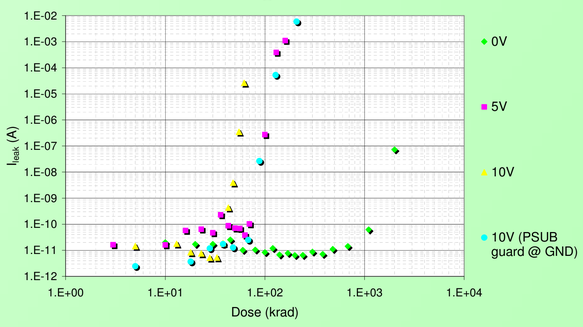


V_{back} = 10V (PSUB guard-ring Floating)

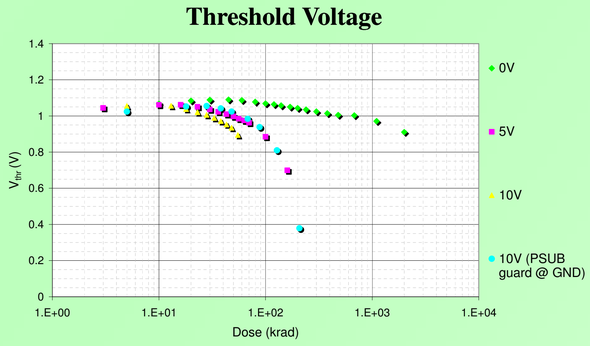


- The leakage current and the threshold voltage strongly depend on the bias condition during irradiation: the higher V_{back}, the higher I_{leak} and the lower the V_{thr} (greater damage on the BOX).

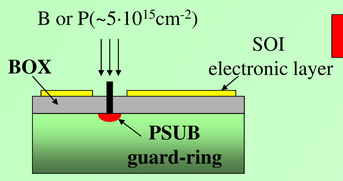
Leakage current



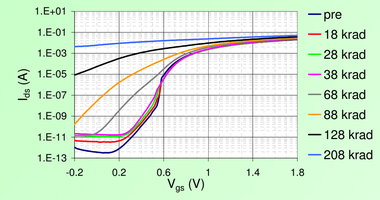
Threshold Voltage



PSUB GUARD-RING

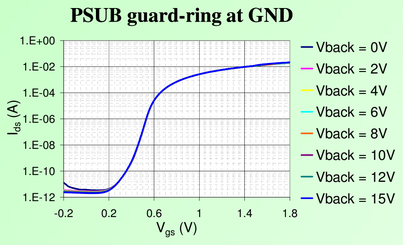


V_{back} = 10V (PSUB guard-ring @ GND)

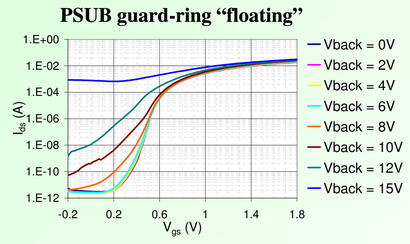


- The PSUB guard-ring tied at GND during irradiation indeed limits the electrical field through the BOX and improves the radiation hardness of the device.
- The PSUB guard-ring is effective in limiting the backgate effect

PSUB guard-ring at GND

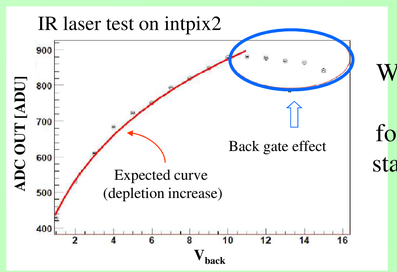


PSUB guard-ring "floating"



For V_{back} = 0V the transistor is still working properly up to doses of ~1Mrad.

C-V measure on SOI-2 chip:
measured depletion is smaller than expected
(700Ω·cm is the nominal resistivity)

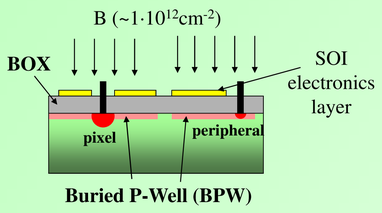


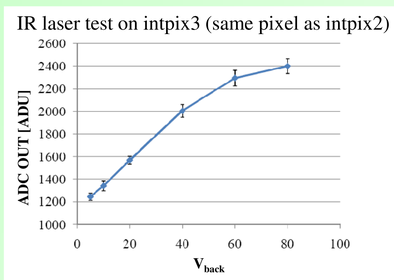
With a standard PSUB implantation, for V_{back} > 10V, output starts decreasing due to back gate effect

[Toshinobu Miyoshi (KEK) presented at STD7, Hiroshima, 2009]

- A new implant method was provided by OKI in 2008, consisting of a lightly doped P-well implanted below the BOX through the SOI layer.

BURIED P-WELL (BPW)

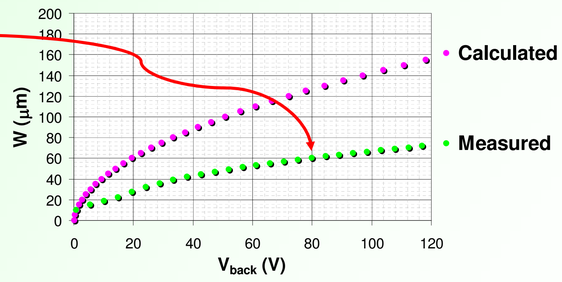




[Toshinobu Miyoshi (KEK), presented at STD7, Hiroshima, 2009]

- With the BPW, no back gate effect up to 80V (~60µm).
- A lower electric field in the BOX should also improve radiation hardness

Depletion depth



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We are also grateful to Prof. Yasuo Arai (KEK) for the effective collaboration in the development of SOI pixel detectors and for providing us with the test structures.

Conclusions and future studies:

- We verified the dependence of the total dose damage from the substrate bias condition during irradiation;
- A low electrical field through the BOX would allow the transistors to work properly up to doses of ~ 1Mrad
- Both the backgate effect and the radiation sensitivity would improve, provided a method to keep low the potential under the BOX. Different solutions should be investigated:
  - a different geometry of PSUB guard-ring implantation on the substrate
  - a buried P-Well under the BOX in the next version of the SOI-2-imager

References:

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