

# Total dose effects on a deep-submicron SOI technology for Monolithic Pixel Sensor development

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A monolithic pixel detector in deep-submicron Silicon On Insulator (SOI) technology has been developed and characterized. This summary presents the first assessments of the effect of ionizing radiation as regards the total dose damage on single transistors in the technology used for the development of the first prototype chip. This work shows the decisive effect of the substrate bias condition during irradiation on the radiation induced damage on the electronics.

## Summary

SOI technology allows the fabrication of CMOS integrated circuits on a thin Silicon layer, electrically isolated from the rest of the silicon wafer by means of a thick oxide layer. The isolation of the electronics from a high-resistivity substrate, used as sensitive volume, allows the production of monolithic pixel sensors for particle tracking and imaging. Vias etched through the oxide contact the substrate from the electronics layer, so that pixel implants can be created and a reverse bias can be applied.

A prototype chip, named LDRD-SOI-1, has been obtained in 2007 in a 0.15 $\mu\text{m}$  Fully Depleted (FD) SOI technology. In the chip, some single transistor test structures are implemented, including both I/O and core transistors (n-type and p-type).

The thick buried oxide (200nm) is expected to be sensitive to ionizing doses, which lead to positive charge trapping and consequently to an increase of the top-gate leakage current. This effect is even larger for the kind of structures we are studying. In fact, when a depletion voltage is applied to the detector, a strong electrical field is present inside the BOX. When exposed to ionizing radiation, electron-hole pairs are created inside the thick oxide. Due to the presence of the electrical field, these charges are immediately separated and do not recombine. This greatly increases the amount positive charge which is trapped throughout the BOX. The total dose damage is hence expected to be strongly dependent on the substrate voltage.

The test structures were characterized as regards their tolerance to total dose effects, by measuring the  $I_{\text{ds}}-V_{\text{gs}}$  curves of each transistor before and after irradiation with X-ray photons. The irradiations were performed with the transistors in the worst-case bias conditions. A first chip was irradiated with a dose of 15krad (SiO<sub>2</sub>), in one single step. The substrate bias was  $V_{\text{sub}} = 40\text{V}$ , to maximize the number of electron-hole pairs escaping recombination. A second chip was irradiated up to a dose of 54krad(SiO<sub>2</sub>) with the same transistors bias conditions, but applying a  $V_{\text{sub}} = 10\text{V}$  (a typical operative value for the substrate bias of the pixel detector).

On the same dose given to the transistor, the two bias voltages induce two different damages: while the irradiation with  $V_{\text{sub}} = 10\text{V}$  increments the leakage current less than one order of magnitude, the same dose given with  $V_{\text{sub}} = 40\text{V}$  during irradiation induces an increase of the leakage current of a factor 104. The positive charge trapped inside the buried oxide in the first irradiation ( $V_{\text{sub}} = 40\text{V}$ ) is sufficient to invert the back-channel interface, which forms a conducting path between the source and the drain and leads to a huge increase of the leakage current (the transistor is "ON" state even without any voltage applied to the gate).

Further investigation on the substrate bias conditions are planned for a 0.20 $\mu\text{m}$  FD SOI technology of the same producer, which was used for the development of the second prototype chip (LDRD-SOI-2). Also the effects of different dose rates will be addressed to.

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