

AFTER, the front end ASIC of the T2K Time Projection Chambers

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Abstract

The T2K (Tokai-to-Kamioka) experiment is a long baseline neutrino oscillation experiment in Japan. A near detector, located at 280m of the production target, is used to characterize the beam. One of its key elements is a tracker, made of three Time Projection Chambers (TPC) read by Micromegas endplates. A new readout system has been developed to collect, amplify, condition and acquire the data produced by the 124,000 detector channels of these detectors. The front-end element of this system is a new 72-channel application specific integrated circuit. Each channel includes a low noise charge preamplifier, a pole zero compensation stage, a second order Sallen-Key low pass filter and a 511-cell Switched Capacitor Array. This electronics offers a large flexibility in sampling frequency, shaping time, gain, while taking advantage of the low physics events rate of 0.3 Hz. We detail the design and the performance of this ASIC and report on the deployment of the front-end electronics on-site.

I. INTRODUCTION

T2K (Tokai-to-Kamioka) experiment [1] is dedicated to the study of neutrino oscillations. An intense artificial neutrino beam from the J-PARC (Japan Proton Accelerator Research Complex) facility in Tokai is sent 295 km across Japan towards the already existing Super Kamiokande detector [2] in Kamioka to study how neutrinos change from one type to another. The ND280 [3] detector complex is presently under construction for a scheduled completion by the end of 2009. Located at 280 m from the neutrino production target, its purpose is to measure properties of the neutrino beams at the J-PARC site before the neutrinos have had a chance to oscillate into other flavours. This near detector complex comprises an on-axis detector and off axis detectors mounted inside a magnet used formerly in the UA1 and Nomad experiments. Two Fine-Grain Detectors (FGD), a pi zero detector, an electro-magnetic calorimeter and muon detectors are housed together with three large Time Projection Chambers (TPCs) inside this magnet. These TPCs (schematic view shown on Figure 1), will measure the momenta of muons produced by charged current interactions in the detector, and will be used to reconstruct the neutrino energy spectrum. Each half TPC (2 m x 1 m x 2m) endplate is read by a 1.5 m² mosaic of 12 pixelated Micromegas modules manufactured using the bulk technology [4]. The front-end electronics modules are directly plugged on the Micromegas detectors, avoiding then the use of fragile fine pitch cables or

expensive kapton flex cables, to minimize noise and reduce cost.

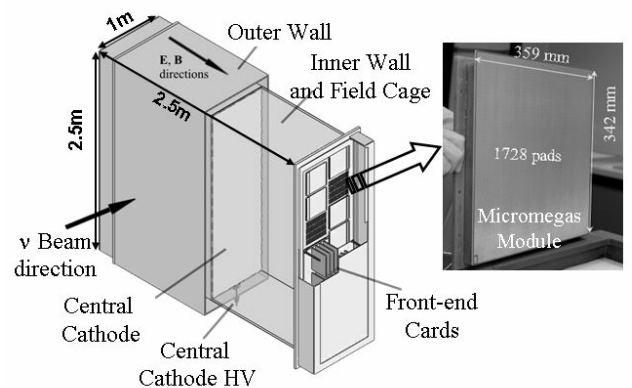


Figure 1: Schematic view of one of the 3 TPCs and picture of a 36 cm x 34 cm Micromegas readout module.

II. ELECTRONICS SYSTEM OVERVIEW

A. Requirements and Constraints

To reach the required reconstruction precision of tracks, the anode of each Micromegas detector is segmented in 1728 pads of 9.8 mm x 7 mm resulting in a total number of 124,416 signals to read. For each pad, the current signal is collected, shaped and recorded (synchronously for all the TPCs) during a duration corresponding to the maximum drift time in the TPC. Then, the X and Y coordinates of the track are reconstructed by computing the centroid of the charges recorded on the pads hit, while the Z coordinate is determined by the drift time of the electrons in the gas volume computed from the ~500-sample long waveform recorded for each pad. The maximum drift time in the TPC can vary from 10 μ s to 500 μ s depending on the gas used. For this reason, the sampling frequency must be adjustable from 1 MHz to 50 MHz. The charge delivered by a pad for a Minimum Ionizing Particle (MIP) is typically few tens of fC, depending on the Micromegas high voltages. A maximum dynamic range of 10 MIP is required with non-linearity smaller than 1% (in the 1-3 MIP range) together with a 100 signal to rms noise ratio for the MIP signal for accurate centroid calculation.

The neutrino beam is pulsed; there is one spill every ~3.5 s. The TPCs require an external trigger signal and must be able to

capture all beam spills and calibration events (cosmic rays and internal illumination by a laser) at up to 20 Hz. The maximum allowable dead-time for acquiring an event is 50 ms. In addition to these functional requirements, the front-end part operates in a modest magnetic field (0.2 T) with limited space available, a low power budget and no access during operation. There is no special constraint concerning radiation.

B. Architecture of the Electronics

After having collected, filtered and sampled the signals from the detector, the main functions of the electronics are to reduce and smooth the huge data flow coming out from the front-end and reaching 50 Tbps during the drift time in the gas to values compatible with the DAQ. For this purpose, the electronics takes advantage of the low rate of the events.

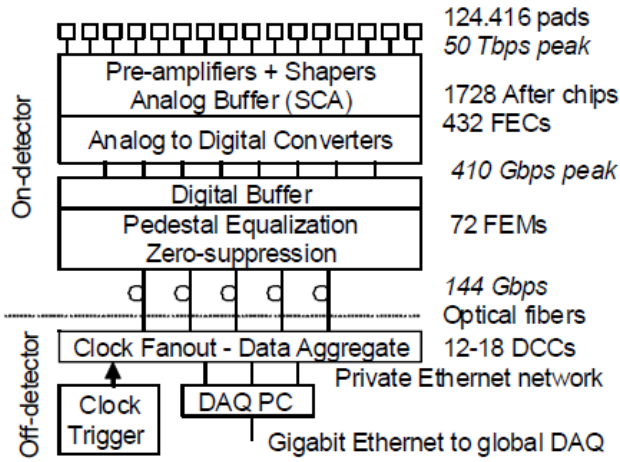


Figure 2: TPC readout flow.

The on-detector electronics, located inside the magnet, is based on a modular electronics unit, depicted in Figure 3, reading one whole Micromegas module. This unit, connected directly to the anodes, is composed of 6 Front-End Cards (FECs) and one Front-End Mezzanine (FEM) card. Each 288-channel FEC houses input spark protections, 4 custom-made 72-channel “AFTER” front-end chips (ASIC For TPC Electronic Readout) and a commercial 12-bit quad-channel ADC. The ASIC collects and filters the detector signals and samples them continuously in an analog memory, based on a Switched Capacitor Array (SCA) until an external stop signal, tagging the end of the drift time, arrives. Then, taking advantage of the inter-spill time, the analog data from all the channels of the chip is multiplexed towards one of the four channel of the external ADC achieving thus a first 72-to-1 data concentration.

This scheme permits to decouple the sampling frequency (settable from 1 MHz to 100 MHz) and the digitization and digital data treatment clock frequencies (which are set at a fix value). The FEM is a digital electronics card that controls up to 6 FECs, gathers events digitized by the FECs, performs optionally pedestal subtraction and zero suppression, and sends data outside the detector through a full-duplex gigabit optical link. Outside the detector, 6 Data Concentrator Cards (DCC) aggregate the data of the TPC endplates and send event fragments to a merger computer that performs a final data reduction and communicates with the experiment DAQ system via a standard network connection. At the DAQ level, the data has been reduced to less than 250 Kbyte/event.

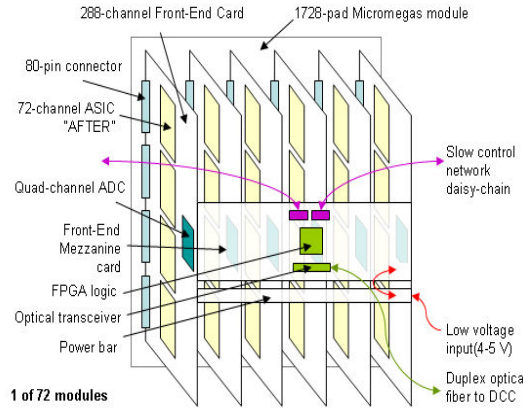


Figure 3: Front-end electronics of one Micromegas module.

III. THE AFTER CHIP

A. Description and Architecture.

The AFTER chip is the central component of the FEC board. It performs a first concentration of the data from 72 inputs to only one analog output connected to an external ADC. Defined before the final choice of the detector, it was developed to accommodate various kinds of detectors and gas mixtures. For this reason, it is very versatile so that its main parameters can be set, using a slow control serial link, to match the detector parameters. For instance 4 different gains are selectable to adapt the chip range to the detector gain and its shaping time and sampling frequency can be chosen to match the drift time in the gas. Moreover the chip can deal with both signal polarity to be compatible with wire chambers readout and is usable with a wide range of input capacitance, even if it is optimized for 20 pF, which is the nominal value expected for detector and routing. Several test modes are available, allowing pulsing one or several channels with a known charge for test or calibration purposes. The main chip specifications are summarized in Table 1.

Table 1: Main Specifications of the AFTER Chip

Parameter	Value
Number of channels	72
Samples per channel	511
Dynamic Range	2 V / 10 MIPs on 12 bits
MIP charge	12 fC to 60 fC
MIP/Noise ratio	100
Gain	4 values from 4 mV / fC to 18 mV / fC
“Detector” capacitor range	0 pF -40 pF
Peaking Time	100 ns to 2 μs (16 values)
INL	1% 0-3 MIPs ; 5% 3-10MIPs
Sampling frequency	1 MHz to 100 MHz
Readout frequency	20 MHz to 25 MHz
Polarity of detector signal	Negative (T2K) or Positive
Test	1 among 72 channels or all

The architecture of AFTER is shown on Figure 4 and a detailed description can be found in [5]. Each of its 72 channels comprises a front-end part dedicated to the charge collection and the shaping of the detector signal followed by a Switch Capacitor Array (SCA) that samples and stores the analog signal.

The front-end part is made of:

- a NMOS-input Charge Sensitive Amplifier with a folded cascod architecture and continuously reset by a resistor virtually multiplied by an attenuating current conveyor.
- a pole-zero amplifier, using a branch of the current conveyor to cancel the CSA dominant pole. It also amplifies the CSA output signal by a factor comprised between 6 and 30 depending on the gain setting and realises the first pole of the shaper.
- a Sallen-Key filter with 2-complex poles producing a relatively narrow response with a very small undershoot (0.8%).
- an inverting voltage amplifier doubling the signal and driving the SCA.

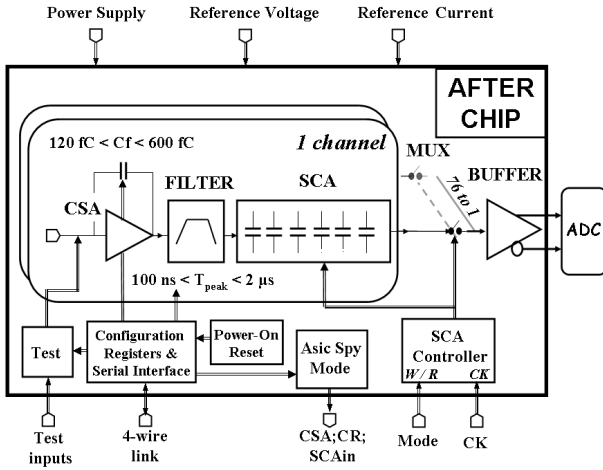


Figure 4: Architecture of the AFTER Chip

Each channel includes a 511-cell SCA using 4-switches high dynamic range analog memory cells [6] and a read amplifier. Four extra similar channels are available for optional common mode or fix pattern noise rejection (not used for T2K operation). Each SCA channel operates as a 511-cell circular analog buffer in which the signal coming out from each analog channel is continuously sampled and stored at a F_{wck} sampling rate (up to 100 MHz). When a stop signal is received, the SCA state is frozen and the analog data are sequentially read and multiplexed column by column towards an external commercial 12-bit ADC converting at a 20 MHz rate. The SCA can be totally or partially read. The readout time for the whole memory takes 2 ms corresponding to a fix dead time.

B. AFTER Chip Performances

The AFTER chip has been manufactured using the 0.35 μ m CMOS technology from AMS. The chip integrates 400,000 transistors on a 58 mm² area and is packaged in a 160-pin LQFP package. 5300 chips have been produced with

a parametric yield of 89%. 1728 of them are used to read the TPCs of T2K. 300 chips are also used, with different slow-control parameters, to read the Silicon Photo-multipliers (MPPC) of the T2K 280m Fine Grain Detectors.

All the measured characteristics are fulfilling the design specifications. The power consumption is 7mW/channel. The peaking time and the shape of the signal (shown on Figure 5) are corresponding to our expectations as well as the dynamic range and the integral non-linearity (better than 1.2% over all the four ranges).

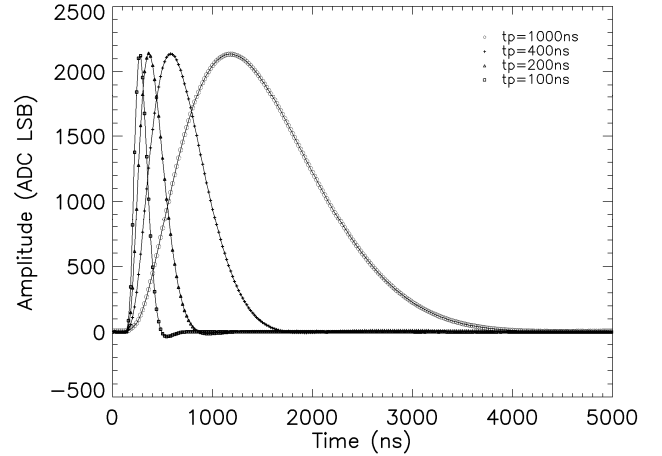


Figure 5: 60 fC test pulses recorded by AFTER with various peaking time (120 fC range).

The chip even operates perfectly at a 100 MHz write frequency although it has been designed for a target of 50 MHz.

A complete noise characterization has been made by varying input capacitor and shaping time. It has been used to extract a detailed noise parameterization reported and discussed in [5]. The parameters corresponding to a linear approximation of the ENC versus input capacitance function, valid in the 15 pF – 40 pF, are given in Table 2.

Table 2: Parameters for the linear approximation of the ENC versus detector capacitance characteristic for the various ranges and various peaking times. Approximation is usable in the 15 pF to 40 pF range.

		100 ns	200 ns	500 ns	2 μ s	Unit
120 fC	Offset	350	370	415	404	e-
	Slope	22.2	14.6	7.8	5.3	e-/pF
240 fC	Offset	690	700	775	750	e-
	Slope	13	8.5	4.5	3.1	e-/pF
360 fC	Offset	1015	1050	1135	1092	e-
	Slope	10.7	5.6	3	2.8	e-/pF
600 fC	Offset	1700	1740	1817	1780	e-
	Slope	6.5	3.2	3.3	1.8	e-/pF

Figure 6 shows this characterization for the 120fC range. For input capacitances smaller than 30 pF and shaping time shorter than 200 ns, which are the parameters foreseen for the operation with the TPC of T2K the noise is smaller than 1000 e- rms which was our target.

The on-chip crosstalk has been measured. It is derivative and its amplitude is less than +/- 0.4% decreasing with the

distance between channels. The voltage droop in the SCA is less than 1 ADC bin - 164 electrons (for the 120fC range) or 1/4096 of the whole dynamic range - within 2 ms with a mean value of 0.29 ADC bin. This effect remains negligible compared to the noise.

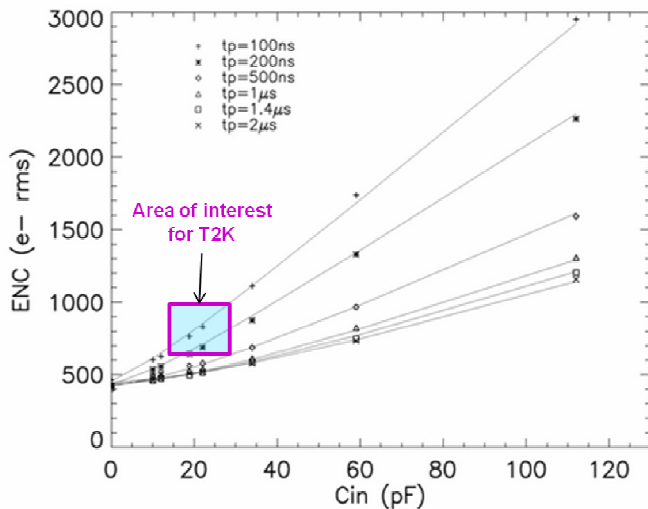


Figure 6: ENC versus input capacitance for different peaking times (120 fC range).

C. AFTER on-Detector Performances

The performances of the AFTER chip are unchanged when soldered on FEC and plugged on detector. In particular, the average rms noise measured for the complete chain in operating conditions on the TPC field cage is less than 800 electrons corresponding to 5 ADC counts, for the 120 fC range and a 200 ns shaping time. We show on Fig. 7 a typical map of the rms noise of the 1728 channels (48×36) of one detector module. The very small dispersion is due to differences of routing- and then of input capacitances which can go from 7 pF to 17pF- between the detector and the corresponding input of an AFTER chip.

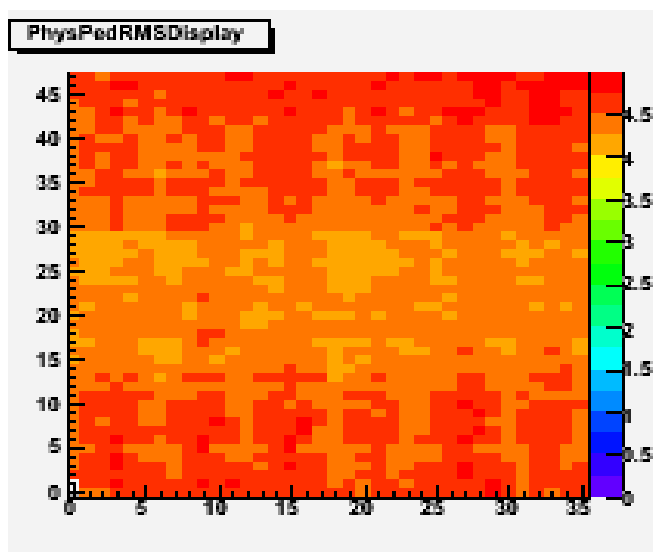


Figure 7: Map of the ENC on a typical Micromegas detector. (120 fC range, 200ns peak time). 1 ADC bin corresponds to 164 e-.

This excellent uniformity is emphasized by the distribution of the ENC for the 41,500 channels of the first equipped TPC shown on Figure 8. The mean ENC over the whole TPC is 720 electrons with a spread of only 28 electrons rms. As the maximum signal is 120 fC the dynamic range is 1040 corresponding to slightly more than 10 bit rms.

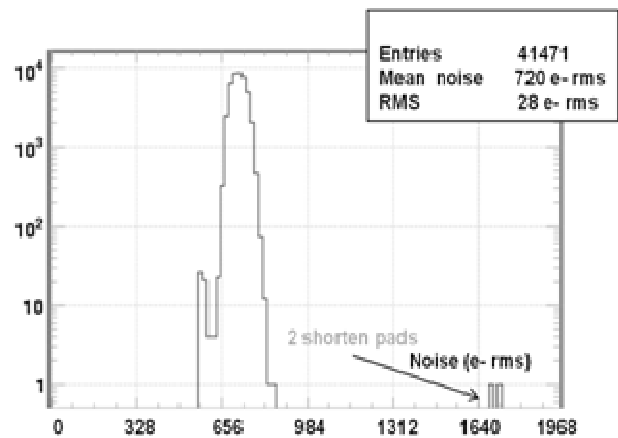


Figure 8: Map of the ENC on a typical Micromegas detector. (120 fC range, 200ns peak time). 1 ADC bin corresponds to 164 e-.

The only 2 pads exhibiting a pathological noise are short-circuited on the detector. Inter-channel capacitance due mainly to the routing increases slightly the crosstalk to 1.2% which is still a reasonable value. Extensive characterizations of the electronics associated with detectors have been made using radioactive sources before their integration on the TPC at Triumf. A ^{55}Fe spectrum measured with a AFTER-read Micromegas is shown on Figure 9. The 8.5% rms resolution measured on the 5.9 keV ray of iron is intrinsic to the detector itself and similar to the one obtain with high performance commercial preamplifiers.

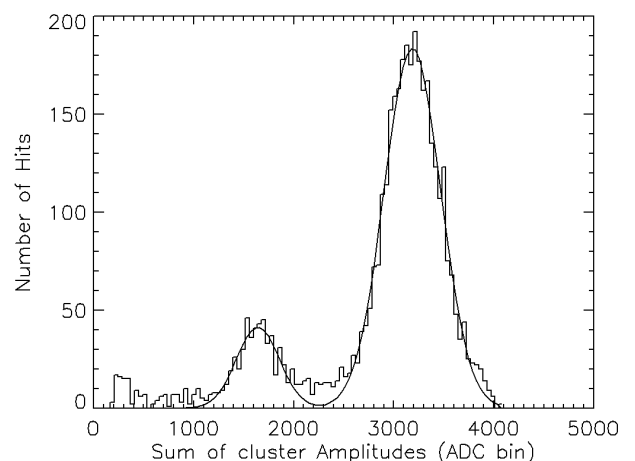


Figure 9: ^{55}Fe Spectrum acquired with AFTER (200 ns peaking time, 120 fC range).

The 3 TPCs have been equipped at Triumf and extensive studies with cosmic rays, the calibration laser and a test beam have been successfully made there before shipping them to Japan where they will start taking data at the end of 2009.

One of the first cosmic events measured by the first TPC is displayed in Figure 10.

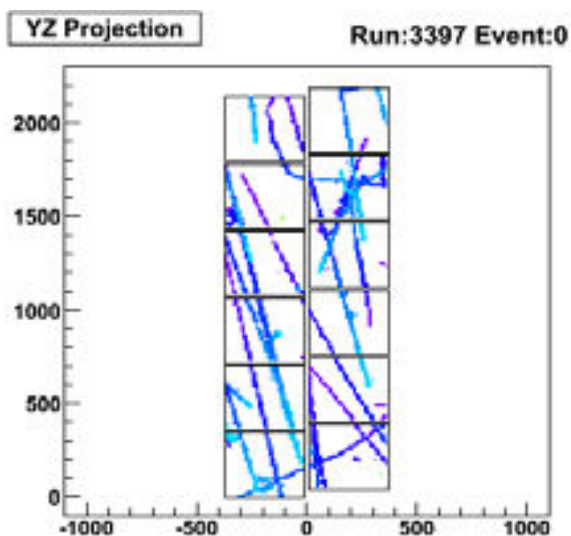


Figure 10: Cosmic event measured with the first TPC.

IV. CONCLUSIONS

A new front-end ASIC has been designed to read the Micromégas endplates of the TPCs of T2K. Its low noise performances are fulfilling the requirements initially defined for the experiment (10 bit rms dynamic range). Its architecture associating 72 channels with very low noise front-end and a S.C.A. inside a same chip offers a compact, reliable and low power solution. The whole electronics based on this ASIC for the TPCs of T2K have been produced,

tested and integrated on the detectors and are now ready for commissioning. In spite its limitations (fix 2ms dead time in case of full readout and need for external trigger), but because of its versatility, its easiness of use and also because it permits the access of the signal waveform, the AFTER chip is now routinely used to test MGPD and even other types of detectors.

V. REFERENCES

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