Low noise, low power front end electronics for pixelized TFA sensors

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Abstract

Thin Film on ASIC (TFA) technology combines advantages of two commonly used pixel imaging detectors, namely, Monolithic Active Pixels (MAPs) and Hybrid Pixel detectors. Thanks to direct deposition of a hydrogenated amorphous silicon (a-Si:H) sensor film on top of the readout ASIC, TFA shows the similarity to MAP imagers, allowing, however, more sophisticated front–end circuitry to extract the signals, like in case of Hybrid Pixel technology. In this paper we present preliminary experimental results of TFA structures, obtained with 10 μm thick hydrogenated amorphous silicon sensors, deposited directly on top of integrated circuit optimized for tracking applications at linear collider experiments. The signal charges delivered by such a-Si:H n-i-p diode are small; about 37 e-/μm for minimum ionizing particles, therefore a low noise, high gain and very low power of the front- end are of primary importance. The developed demonstrator chip, designed in 250 nm CMOS technology, comprises an array of 64 by 64 pixels laid out in 40 μm by 40 μm pitch.

I. Thin Film in ASIC

The next generation of particle colliders in high-energy physics experiments present many challenges for tracking detectors; concerning segmentation, readout speed, level of integration, power constrained low noise electronics, mechanical complexity and radiation immunity [1]. In parallel to commonly used MAP and Hybrid Pixel technologies, new trends and innovations aiming at improving detector performance are being developed [2]–[3]. One of these alternatives, called Thin Film on ASIC (TFA) technology, combines the advantages of both technologies mentioned above. In a TFA structure thin sensor film is deposited directly on top of the readout ASIC, allowing to get rid of the bump bonding, which imposes limitations on sensor segmentation, cost and material budget. A low deposition temperature of the TFA sensor elements, around 200 °C, is compatible with post processing on finished ASIC wafers. This allows for separate design, optimization and bias of the sensor and readout electronics, like in case of Hybrid Pixel detectors. A schematic diagram of the TFA structure is presented in Fig. 1

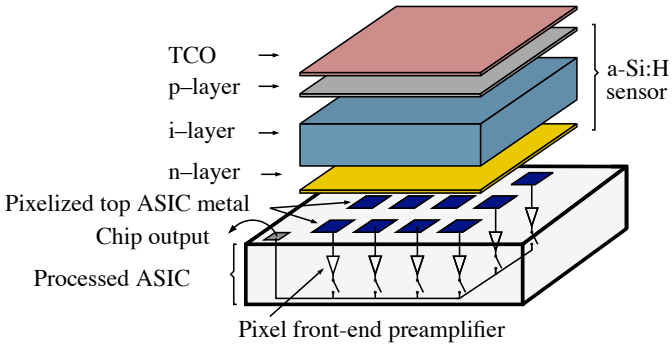


Figure 1: Schematic representation of the TFA structure, composed of a p-i-n diode deposited directly on an ASIC.

A. Sensor

The sensor is built on top of the ASIC by consecutive depositions of n-doped, intrinsic and p-doped films forming a n-i-p diode. The pixelized ASIC top metal, which serves as sensor bottom contacts (anodes), defines the sensor segmentation. In order to keep this segmentation without patterning the n-layer, which is common over all the ASIC surface, the n-layer is designed with a low conductivity, providing an isolation higher than 10 MΩ. The common top electrode (cathode), deposited on the sensor p-layer, is represented by a Transparent Conductive Oxide (TCO) made from Indium Tin Oxide. The sensing layer, made of hydrogenated amorphous silicon (a-Si:H), is placed between the ASIC top metal and the TCO electrode. This material has been studied over the past 30 years and is widely used in solar cells industry and in various imaging devices [4]. An attractive feature of the a-Si:H sensors is high radiation hardness [5], which makes them an interesting and promising option for tracking detectors in high-energy physics experiments. Although, the most recent results show that more studies need to be done on this material to conclude on its potential higher radiation hardness compared to crystalline silicon [4]. Despite significant progress in technology of depositing thin film hydrogenated amorphous silicon on ASICs, the signal charges delivered by such sensors are small, about 37 e-/μm for a minimum ionizing particle [6]. Taking into account reasonable diode thicknesses of 15 μm, fully depleted, one can expect the signals up to 600 e^-. Therefore a low noise and high gain front-end

circuit is of primary importance.

B. Readout electronics

A schematic diagram of the developed readout circuit is shown in Fig. 2. The circuit is based on a charge sensitive preamplifier built around an unbuffered cascode stage with feedback capacitor C_f of 1.3 fF, which provides sufficiently high gain of 800 mV/fC in the single stage amplifier.

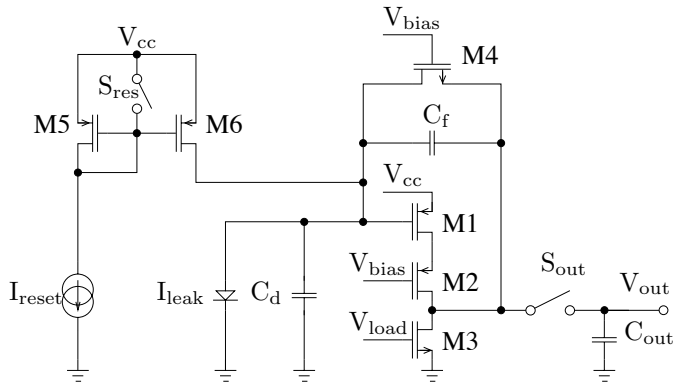


Figure 2: Schematic diagram of the charge sensitive preamplifier with the soft reset.

The dimensions of the input PMOS transistor M1 are 6 μm/0.28 μm, which allows us to keep the gate capacitance (C_g = 10 fF) small compared to the total input capacitance (C_{int} = 40 fF, including the detector capacitance C_d), which determine the noise performance of the circuit.

The preamplifier works as a gated integrator with acquisition time t_{acq} and integration time constant τ_i. The operation sequence starts with the reset phase, when switch S_{res} is open, and the reset current I_{reset} flows through current mirror M5-M6 feeding transistor M4. The gate of this transistor is biased by constant voltage V_{bias}, and therefore transistor M4 is kept in saturation, causing continuous discharging of the feedback capacitor C_f. During the reset phase, the switch S_{out} stays open and no incoming signals are sent to the preamplifier output. In the next step, the preamplifier operates in the acquisition mode, when the input signals are amplified and stored in the preamplifier output. In this phase, switch S_{res} is closed, and no current flows through transistor M4 in the feedback loop. The input signal is integrated on the feedback capacitor C_f and transferred through switch S_{out} to the output capacitor C_{out}. Simultaneously, switch S_{out} opens and the preamlifiers array is readout out. Since capacitor C_{out} is disconnected from the cascode output, the preamplifier is kept in the reset mode while the array of output capacitors is read out by a serial multiplexer. When data from the pixels array are sent out, the output capacitors needs to be discharged by short reconnection to the preamplifier.

During the reset phase, the feedback capacitance is discharged through the transistor biased with a constant current. This is a novel solution compared to commonly used voltage controlled reset transistor. We have investigated this new schema because otherwise the parasitic charge injection from the reset signal to the very small feedback capacitor C_f would lead to saturation of the preamplifier. From this point of view, a small reset current is favorable. On the other hand, the preamplifier stage working in a soft reset regime operates as a transimpedance amplifier with parallel noise sources originated from transistors M4 and M6. For higher reset currents, the gain of the cascode stage working in the reset mode is decreased, and one could expect lower output noise. However, this circuit is even more complex, since the two switchable modes, reset and acquisition, represent two different signal (and noise) input-to-output transfer functions.

II. Noise estimation

The presented design was optimised for the linear collider application, where the time window when interesting events may appear is short, in a range of hundreds nanoseconds. In order to minimize the influence of the sensor leakage current on the readout electronics, the preamplifier should be switched to the acquisition mode only when interesting events arrive to the sensor. During this time window the noise of the front-end electronics needs to be minimized to ensure high signal to noise (SNR) ratio. The noise estimation is performed separately for the reset phase and for the acquisition phase in the frequency domain. Since this circuit is time-variant and its input-to-output transfer function depends on the actual mode of the preamplifier operation, the noise calculation are more complex than in case of time-invariant circuits. Therefore, we have employed a simplified model. It is assumed that the SNR ratio in the acquisition phase is determined by two noise components:

- noise generated in the preamplifier during the acquisition phase,
- noise sampled at the reset phase.

The former term is due to the cascode input and load transistors (M1 and M3), as well as to the sensor lakage current. In order to describe the latter term, the following model is assumed: when the preamplifier operates in the reset mode, the noise at the output node is fed back to the input node through the feedback loop. When the preamplifier is switched from the reset to the acquisition mode, the noise at the input node is sampled. Subsequently, this sampled noise is transfered to the output node by the acquisition phase transfer function. The noise calculations were performed by using the models proposed by van der Ziel [7] slightly modified for weak and moderate inversion regions of the MOS transistor [8].

A. Noise in the acquisition phase

The main noise sources, which are taken into account, originate from the cascode input transistor M1, cascode load transistor M3 and from the detector leakage current. The analysis is performed based on van der Ziel expressions for noise power spectra densities [7] and Enz-Krummenacher-Vittoz (EKV) analytical MOS transistor model [8]. The following noise sources were taken into account in the analysis: for the input transistor M1 the channel thermal noise, gate induced current (GIC) noise, the flicker noise and the correlation term, while for the load transistor M3 the channel thermal noise term only. It is assumed that

the overall shaping function of the preamplifier is equivalent to a gated integrator, where the integration time constant is defined by the bandwidth of the unbuffered cascode stage loaded with input, output and feedback capacitances. A finite readout time cuts off the low frequency noise components. After a detailed analysis of the circuit, one obtains the approximate formula (1), which describes frequency transfer function $K_{acq}(f)$ used further for calculation of the Equivalent Noise Charge (ENC):

$$|K_{acq}(f)|^2 = \frac{1}{1+(2\pi f)^2\tau_i^2}\frac{(2ft_{acq})^2}{1+(2ft_{acq})^2}, \qquad (1)$$

where τ_i is the integration time constant given by formula (2):

$$\tau_i = \frac{C_{int}C_{out} - C_f(C_{int}+C_{out})}{-C_{int}g_{ds3} + C_f(g_{ds3}+g_{m1})}, \qquad (2)$$

g_{m1} is the tranconductance of transistor M1, g_{ds3} is the output conductance of transistor M3, C_{int} is the estimated total input capacitance including the a-Si sensor capacitance, parasitic capacitances extracted from the layout and the gate capacitance of the input transistor M1, C_{out} is the estimated total output capacitance and t_{acq} is the duration of the acquisition phase. Assuming that the acquisition time t_{acq} is much longer than the integration time constant τ_i, the charge gain of the circuit depends only on the value of feedback capacitor C_f.

Fig. 3 shows the ENC calculated as a function of the input transistor bias current I_D for the acquisition time t_{acq} of 1 μs and following values of capacitances extracted from the layout and estimated for the 10 μm thick a-Si sensor; C_{int} = 40 fF (including detector capacitance 5.5 fF), C_f = 1.3 fF, C_{out} = 120 fF.

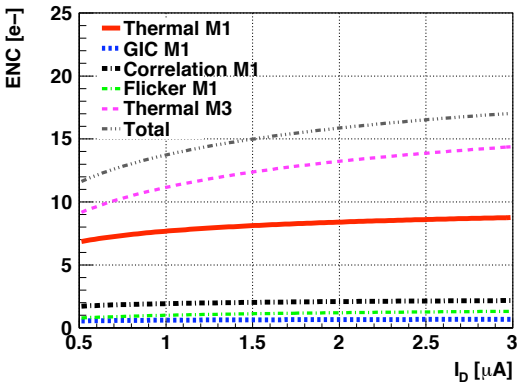


Figure 3: Calculated noise originating from the acquisition phase. Acquisition duration 1 μs.

The nominal bias current of 2 μA has been chosen as a compromise between power consumption, which is about 10 μW, and the integration time constant τ_i, equal to 80 ns, which defines minimum readout time t_{acq} and consequently, the sensitivity of the ENC to the parallel noise sources. For the nominal parameters of the circuit described above, the expected ENC is below 16 e−.

The noise related to the detector leakage current was calculated for three acquisition times: 1 μs, 0.5 μs and 0.3 μs. The ENC versus detector leakage current is presented in Fig. 4. The preamplifier is optimized assuming maximum sensor leakage current of 10 pA. This noise should be compared with the noise originating from the reset phase.

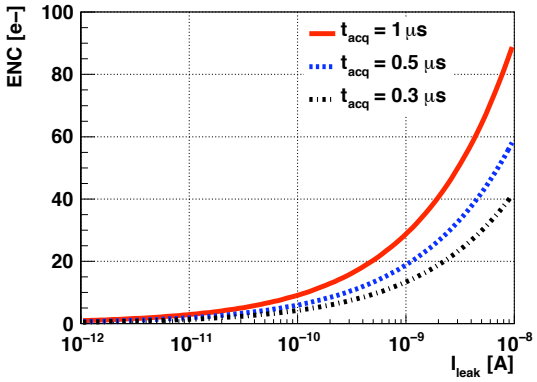


Figure 4: Calculated noise originating from detector leakage current.

B. *Noise in the reset phase*

The noise in the reset phase is due to the channel thermal noise of transistors M1, M3, M4 and M6. During the reset phase the feedback transistor M4 is biased with the reset current I_{reset}. Therefore, the preamplifier transfer function $K_{res}(f)$ differs from the one of the acquisition phase $K_{acq}(f)$ defined by (1). One should remember, the $K_{res}(f)$ strongly depends on the reset current I_{reset}, which sets the feedback transistor transconductance g_{m4} and consequently the active feedback resistance. Taking into account the equations describing the spectral densities of channel thermal noise related to MOS transistors listed above, and applying the preamplifier transfer function $K_{res}(f)$, one can calculate the root mean square (RMS) value of noise, which is fed back from the output to the input node. Subsequently, this value is transfered to the preamplifier output node by using the $K_{acq}(f)$. This noise value, expressed in ENC, as a function of reset current I_{reset} is presented in Fig. 5. As one can conclude, in order to minimize the total noise in the acquisition phase, the reset current should be set to low values.

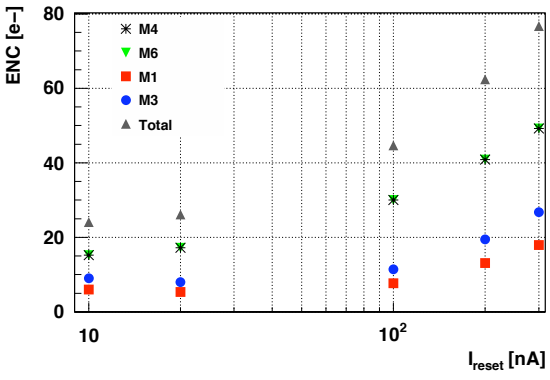


Figure 5: Calculated ENC originating from the reset phase as it it seen in the acquisition phase.

III. Experimantal results

A prototype chip, called Amorphous Frame Readout Pixel (AFRP), has been designed and manufactured in 0.25 μm CMOS process. The photo of AFRP demonstrator chip is presented in Fig. 6.

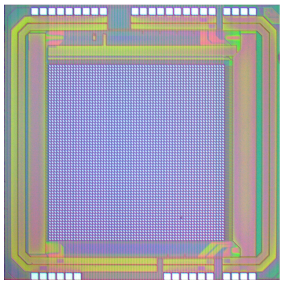


Figure 6: AFRP chip.

The device contains an array of 64 by 64 pixels with a 40 μm by 40 μm area, read out serially through a multiplexer. Due to the limited number of metal layers on the prototype chip, the active area of the input electrode is only 20 μm by 20 μm. The analog and digital grounds and power supply buses are separated to reduce the noise in the preamplifier. Two clock signals to read out rows and columns of the chip, as well as 10MHz master readout clock are supplied externally using the Low Voltage Differential Signaling (LVDS) standard. The readout time of the chip is less than 2.5 ms (600 ns/pixel). The 10 μm thick a-Si sensor was deposited directly on the AFRP chip surface. The deposition was done in the Institute of Microengineering (IMT, EPFL/STI), in Neuchatel by using Plasma Enhanced Chemical Vapor Deposition process.

A. Noise performance of the bare chip

A bare AFRP chip was tested to characterise the noise performance of its 4096 pixels. The noise map of the 64 by 64 matrix of pixels is presented in Fig. 7

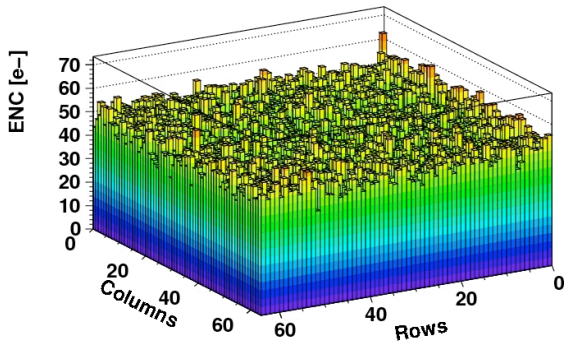


Figure 7: Bare chip noise map for I_{reset} = 10 nA and t_{acq} = 1 μs.

The noise on each pixel equals the RMS value of the output voltage, taken from 200 full chip scans, decreased by the voltage pedestal (mean value of 200 measurements) and expressed in ENC. The noise performance of the raw pixels is homogeneous over whole chip area. The noise distribution of the 4096 pixels, presented in Fig. 8, shows the ENC mean value of 49 e- and a standard deviation σ of 4 e-.

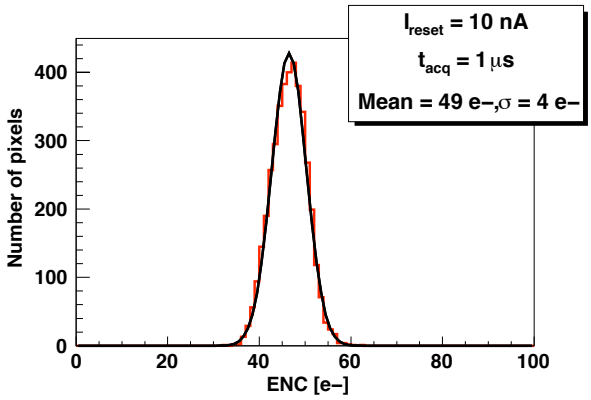


Figure 8: Bare chip noise spread over 4096 pixels for I_{reset} = 10 nA and t_{acq} = 1 μs.

The averaged noise dependence on reset current is shown in Fig. 9.

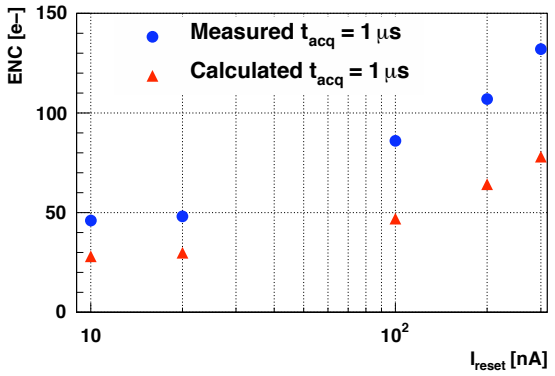
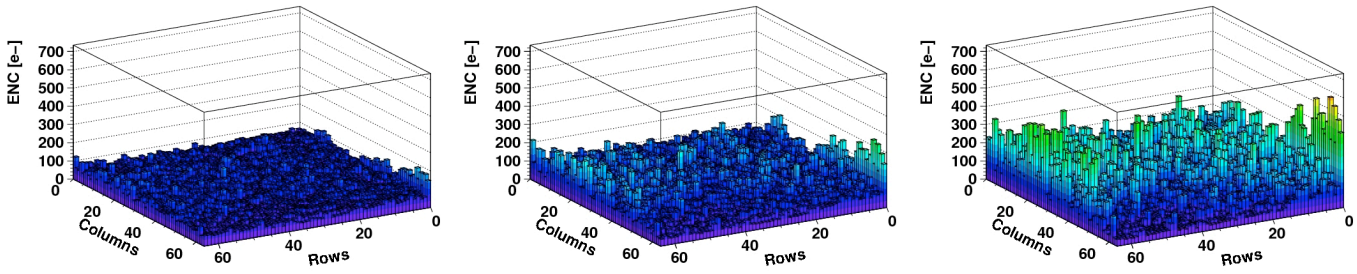


Figure 9: Calculated and measured noise comparison for the bare AFRP1 chip.

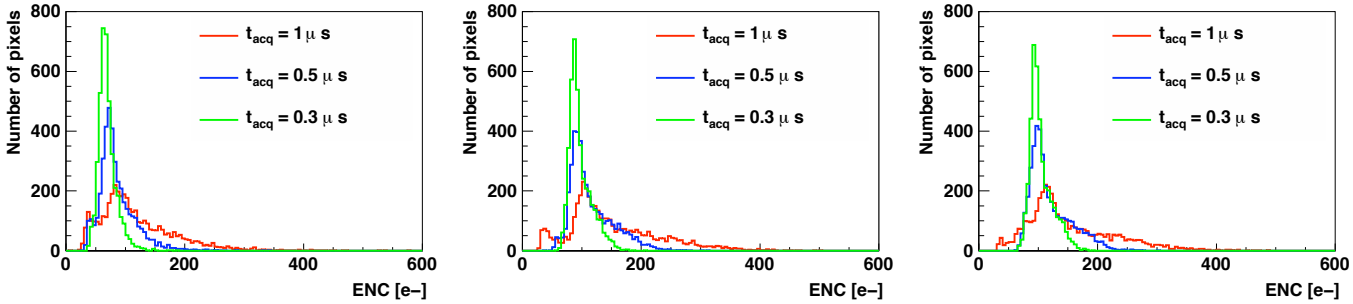
B. Noise performance of TFA

The noise performance of the TFA structure was investigated in the same way as for the bare AFRP chip. The chip noise maps for various values of acquisition time t_{acq} are presented in Fig. 10a – 10c. These noise maps show much larger spread across the pixel array compared to bare AFRP. This effect is even more pronounced for the longer acquisition times, which indicates that the spread is mainly due to variation of the sensor leakage current.



(a) $t_{acq} = 0.3\ \mu s$ (b) $t_{acq} = 0.5\ \mu s$ (c) $t_{acq} = 1\ \mu s$

Figure 10: TFA structure noise map for reset current of 10 nA and a-Si diode bias of 55V.



(a) Reset current of 10 nA (b) Reset current of 100 nA (c) Reset current of 200 nA

Figure 11: TFA structure noise spread on 4096 pixels for diode bias of 55V.

Figures 11a – 11c show distributions of noise for various acquisition times. One can note that besides relatively narrow peaks we observe long tails corresponding to pixels with a noise much higher than the average. These effects need to be most likely related to the leakage current variations, originated probably from non-uniformity of the sensor–ASIC interface. This issue needs to be investigated further. Fig. 12 shows comparison of calculated and measured noise, taking into account most probable values of measured ENC distributions.

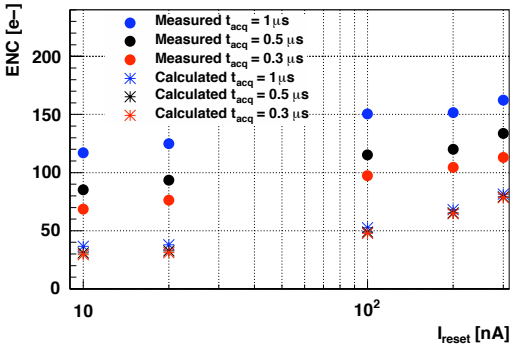


Figure 12: Calculated and measured most probable noise as a function of reset current. The 10 μm thick a-Si diode was biased with 55 V.

C. *Results obtained with a 405 nm blue laser*

Signals from 405 nm blue laser, obtained on 10 μm a-Si diode reversely biased with voltages from 5V to 60V were measured. In order to minimize the influence of the sensor leakage current on the front–end noise performance, the acquisition time was set to short value of 300 ns. During this time periods the blue laser was triggered and the signals were read out from 4096 pixels. Twenty full chip scans were made with laser pulse fired to the sensor surface. In order to illustrate the sensor response V_{signal} to the laser pulse, the pedestals, measured with no incoming laser pulses, were subtracted. The fully depleted sensor response, averaged over 20 scans, is presented in Fig. 13, clearly showing the laser pulse illumination map on our imaging device.

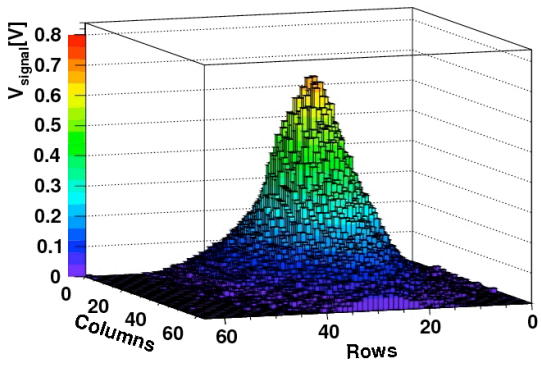


Figure 13: Signals from 405 nm blue laser, obtained on 10 μm thick a-Si diode biased with voltage of 55V.

The full depletion bias voltage of the 10 μm thick sensor

was measured by recording the maximum response $V_{\max\,signal}$ to the laser pulse for varying diode reverse bias voltages $V_{a-Si\,bias}$. This method, demonstrated in [4], is based on the variations of the inducted current for varying depletion thicknesses in an a-Si:H sensors. As shown in Fig. 14, the sensor response to a blue laser pulse increases as a square root of the applied voltage, and starts to saturate for a bias voltage of 55 V. Further increase of $V_{a-Si\,bias}$ does not increase the measured signal $V_{\max\,signal}$.

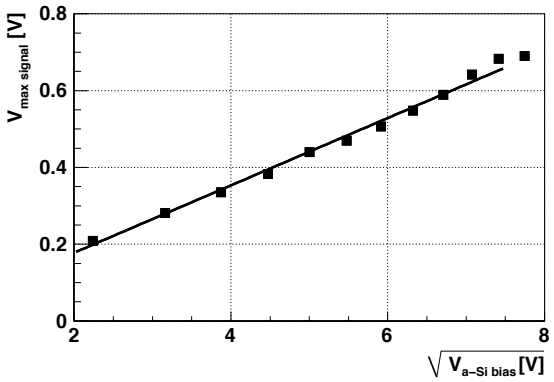


Figure 14: a-Si diode maximum response to the 405 nm blue laser pulse for I_{reset} = 100 nA, t_{acq} = 0.3 μs.

This result agrees with [4], where the full depletion bias voltage for a-Si sensor with a thickness d is estimated as $0.48 \times d^2$, leading to about 48 V for a 10 μm thick diode. The response of the TFA structure to 405 nm blue laser was calibrated by comparison with the response obtained on TFA sensors developed on the MacroPad chip [9], for which the calibration factors are known from measurements of X-rays. As a result, the gain of 713 mV/fC was found (simulated gain: 800 mV/fC) and this value was used for the ENC calculations, presented above.

The average leakage current per pixel was measured as a function of the a-Si:H reverse bias voltage. As shown in Fig. 15, for the fully depleted a-Si sensor, biased with 55 V, the leakage current per pixel is about 1 nA, which is much higher compared to the assumed level of 10 pA.

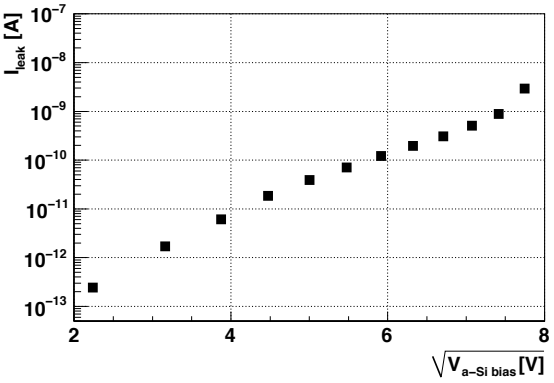


Figure 15: 10 μm thick a-Si sensor average leakage current per pixel.

IV. Conclusions

A 64 by 64 pixels array based on TFA technology was designed, manufactured and tested. The readout electronics has a gain of 713 mV/fC and power consumption of 10 μW/pixel. The noise performance of bare AFRP ASIC is higher than expected, but it is satisfactory taking into account expected response signal from the a-Si sensors. The noise performance of the present TFA prototype is limited by the leakage current. Since the preamplifier was designed and optimized for sensor leakage current of 10 pA, the readout electronics can not handle with 1 nA leakage current for acquisition times longer than 1 μs. The TFA structure was tested with 405 nm blue laser pulses, which were triggered precisely during the acquisition phase of preamplifier. Precise image of the laser spot provide a solid proof of principle for the developed novel pixel detector concept. The main problem of the TFA structure is related to the excessive leakage current, which strongly depends on the quality of an a-Si–ASIC interface. Therefore, further improvements of sensor deposition on ASIC, including the planarization of the ASIC surface, are needed.

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