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Low noise, low power front end electronics for pixelized TFA sensors

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In this paper we present the preliminary experimental results obtained with 10 μm thick hydrogenated amorphous silicon sensors, deposited directly on top of integrated circuit optimized for tracking applications at linear collider experiments. The signal charges delivered by such a-Si:H n-i-p diode are small; about 37 e-/μm for a minimum ionizing particle, therefore a low noise, high gain and very low power front-end circuitry is of primary importance. The developed demonstrator chip comprises an array of 64 by 64 pixels laid out in 40 μm by 40 μm pitch designed in 250 nm CMOS technology.

Summary

Thin Film on ASIC (TFA) technology combines advantages of Monolithic Active Pixel and Hybrid Pixel technologies thanks to the direct deposition of a hydrogenated amorphous silicon (a-Si:H) sensor film on top of the readout circuit. The sensor film comprises 3 layers; a n doped thin layer of a-Si:H in electrical contact to the electrodes of the readout chip, a thick layer of an intrinsic a-Si:H, and a top p-doped a-Si:H thin layer. The intrinsic a-Si:H layer is depleted by applying an electric field of about 5 to 10 V/μm. Compared to the Monolithic Active Pixel imagers, the TFA technology allows using more sophisticated front-end circuitry to extract the signal. In addition, compared to the Hybrid Pixel imagers, the TFA technology does not require bump bonding, which imposes limitations on sensor segmentation, cost and material budget. This technology approach is especially attractive for high sensitivity imagers sensing very low levels of light, low energy electrons and 1-50 keV X-rays. In this paper we present the preliminary experimental results obtained with 10 μm thick hydrogenated amorphous silicon sensors, deposited directly on top of integrated circuit optimized for tracking applications at linear collider experiments. The signal charges delivered by a-Si sensors are small, about 400 e- for a minimum ionizing particle in 10 μm thick sensor layer. For that reason design of a low noise, high gain and very low power front-end circuitry is essential.

The circuit is based on a charge sensitive preamplifier built around an un-buffered cascode stage with 1.3fF feedback capacitor Cf, which provides sufficiently high gain in a single amplifier stage. The dimensions of the input PMOS transistor are 6μm/0.28μm, so that contribution of the gate capacitance (cg = 7fF) to the total input capacitance (cin = 40fF) is reasonably small. During the reset phase the feedback capacitance is discharged through a feedback transistor biased with a constant current instead of a voltage controlled reset transistor, which is a commonly used solution. Investigation of a new solution is stimulated by limitation of the schema with voltage controlled reset transistor due to intolerable parasitic injection from the reset signal to the very small feedback capacitor. From this point of view a small reset currents will be favorable. On the other hand one has to keep in mind that the preamplifier stage working in soft reset regime operates as a transimpedance amplifier with parallel noise sources originated from the feedback transistor.

The integrated signals are stored subsequently on sample and hold buffer and sent out during the readout frame via analogue multiplexer. The device contains an array of 64 by 64 pixels laid out with 40 μm by 40 μm pitch. Total power dissipation is around 10μW per pixel. The developed demonstrator chip was designed in 250 nm CMOS technology. In the paper we will present detailed analysis of noise in the reset and the readout phase, optimization of the design as well as test results for the prototype chip.

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