Contribution ID: **141** Type: **Poster**

The Online Error Control and Handling of the ALICE Pixel Detector

Thursday, 24 September 2009 16:55 (20 minutes)

The SPD forms the two innermost layers of the ALICE experiment. It is equipped with a total of 120 modules (half-staves) with a total number of 9.8 x 106 readout channels. Each half-stave is connected via three optical links to the off-detector electronics made of FPGA based VME readout cards (Routers). The Routers and their mezzanine cards provide the zero-suppression, data formatting and multiplexing and the link to the DAQ system. This paper presents the hardware and software tools developed to detect and process errors occurring at the level of the Router originating from either front-end electronics, DAQ or the off-detector electronics. The error handling system then automatically transmits this information to the detector control system and to dedicated MySQL database for further analysis.

Summary

The ALICE SPD consists of two barrel layers at average radii of 3.9 and 7.6 cm, respectively. The SPD is made of 120 half-staves with a total of about 107 readout channels. Each half-stave is made of two sensors flip chip bonded to five front-end chips each, one Multi-Chip Module (MCM) and an Al/kapton multilayer bus to connect each front-end chip with the MCM. The MCM is connected with the off-detector electronics via three 800Mbit/s bidirectional optical links.

The off-detector electronics consists of 20 VME based readout cards (Routers), each holding three mezzanine cards (LRx) for zero-suppression and data formatting. Each LRx card connects to two half-staves in the detector. The Router card performs the data multiplexing and interfaces to the ALICE Central Trigger Processor (CTP) and Data Acquisition (DAQ) to transmit the data stream.

The hardware tools for error detection consist of two different units implemented in VERILOG modules that were added to the standard off-detector components in the Routers managing the data taking. All error information is processed at 40 MHz. The first unit identifies the error typologies coming from different parts of the SPD system, e.g.: optical connection status and data format errors, front-end and back-end errors/status, SEE (Single Event Effect), wrong trigger sequences or missing/spurious trigger signals, etc. The second unit is a set of VERILOG modules that manage and transmit the error information to the SPD Front-End-Device server (FED). The maximum number of potential error topologies in the full SPD amounts to 3200, which can be processed at 40 MHz. Usually one error condition generates a cascade of secondary errors that then will also be registered by the error detection hardware units. The hardware units are capable to distinguish between the original error and secondary effects and will flag the cause of the problem.

The Software components consist of one low and one high tier. The low tier is driver written in C++ included in the FED. It establishes the communication with the hardware units in the Routers and transmits the error information to the dedicated MySQL Database. In parallel the error information from the FED is sent to the Detector Control System (DCS) to make aware the operator.

A statistical errors analysis (histograms, cross-correlations, etc.) of the different error types can be done using the MySQL database to evaluate the main error sources in the SPD hardware. This will allow monitoring the SPD stability over the lifetime in the ALICE experiment.

The error detection system has been thoroughly tested in the integration lab using final system components and was then implemented in the SPD system in the ALICE experiment. This paper presents the hardware and software tools developed in order to recognize and process errors in the SPD front-end and off-detector electronics. The first operation experience in the experiment are also reported.

Primary author: Dr CASELLE, Michele (CERN - Università Degli Studi di Bari)

Presenter: Dr CASELLE, Michele (CERN - Università Degli Studi di Bari)

Session Classification: POSTERS SESSION

Track Classification: Systems, installation and commissioning