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Buffer Control Chip (BCC) for the ATLAS Tracker Upgrade

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The ATLAS Tracker Upgrade project is developing large modules of up to two hybrids each. Each hybrid comprises two columns of ABCN-25 readout ASICs, each with a data rate twice the bunch-clock. A hybrid readout link thus handles two streams at quadruple the bunch-clock rate. To allow hybrids to operate at different potentials (as required by serial-powering), control signals make use of a novel AC coupled DC LVDS scheme. The BCC ASIC, designed to provide signal buffering, clock multiplication and data multiplexing, is described. Functionality, operation and results of testing and integration onto a tracker module will be presented.

Summary

The ATLAS Tracker Upgrade project has progressed to building large objects nearing the scale and complexity of that is needed for the final system. These comprise 12 modules grouped into a super-module, each module having two hybrids. Each hybrid has 2 columns of ABCN-25 ASICs for reading out the strips. This design introduces a module-controller-chip (MCC) as a means to manage the module. As this component is complex with a long development cycle, an alternative for early testing was developed. The buffer-control-chip (BCC) multiplies the bunch clock and aggrigates data from each column. It also impliments a special AC/DC LVDS buffer.

As there are options for individual hybrids to operate at different potentials (as would be the case with serial powering) it is essential that control signals are AC coupled. To reduce complexity, power and noise generated by always-on balanced coding, a novel DC LVDS over AC method is used. An extra LVDS driver in the receiver feeds-back the signal to hold the input at the state it last transitioned to. These are are being tested for both multi-drop 40MHz
control signals and point-to-point 160MHz readout signalling.

The BCC provides an interface between the off- and on-hybrid signals. As such it receives a 40MHz beam crossing clock (BCO), a command line (COM) and a combined level-1 trigger and reset line (L1R). The ASICs are driven via two clocks - the BCO and a data-clock that is derived from the BCO. The BCC can optionally invert/disable either of these clocks, as well as double the frequency of the data-clock.

The command line is decoded on the BCC, providing multiple functions:
1) Write to the BCC configuration register
2) Readback the BCC configuration register
3) Readback the BCC ID
4) Carry a payload that is forwarded onto the ASICs on either their COM, RESETB or L1 lines

In the readout path, the BCC provides a means of switching to the redundant data output of a column of ASICs. The column data lines are then multiplexed onto the readout data line. An optionally invertable clock is used to sample the data and the phase of the multiplexing clock and various debug modes are provided - accessed via configuration register bits.

The BCC will return from fabrication mid-June 2009. Each die will be bonded
to a PCB for testing. When confirmed functional, the PCB will then be bonded
to a hybrid for use as part of a module. These results will be presented.

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