3D electronics for hybrid pixel detectors

ATLAS read-out chip upgrade

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3D for hybrid pixel detectors

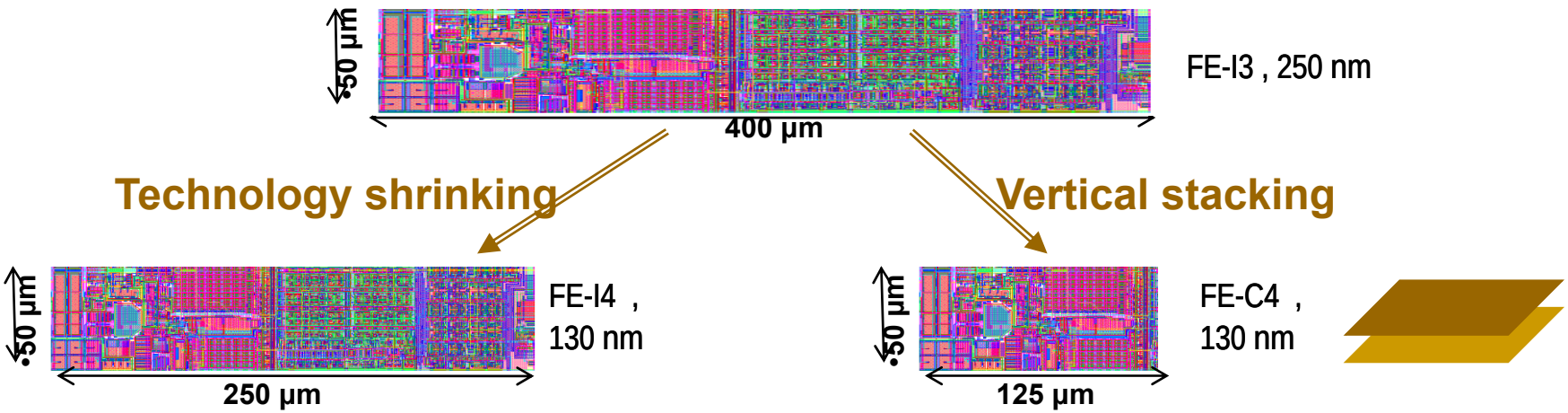
Atlas read-out chip upgrade

- 3D FE-TC4 project :
  - Motivations
  - Context
  - Steps : 2D and 3D circuits
- 2D test results
- 3D design
  - Technology description
  - Tiers description
  - Final assembly
- Conclusion & futures plans

3D motivations for ATLAS upgrades

- **Improve spatial resolution**
- **Deal with an increasing counting rate**
- ➔ **Decrease pixel size**

3D pixel road map (A.Rozanov, ATLAS-France Paris, June 22, 2009) :



3D benefits :

- Pixel size reduction
- Pixel functionalities splitting
- Technologies mixing

FETC4 – Atlas 3D read-out chip project

Bonn, CPPM, and LBL collaboration

- Goal : to reach a pixel dimension of 50*125 µm
- Solution :
  - split pixel functionalities into 2 parts
  - stack vertically these 2 “tiers”

- Context / Opportunity :
  - Interest (and funding !) of IN2P3 on 3D electronics
  - First MPW run for High Energy Physics organized by FNAL with a consortium of 15 institutes (France, Germany, Italy, Poland and United-States)
  - This process combines :
    - **Chartered 130nm technology**
    - **Tezzaron 3D technology**

3D project steps

FEI4_P1 design 14*61 "analog" pixel matrix (50 * 166µm)
(8 metal levels, 130nm,IBM)

Translation into 2D Chartered technology
(8 metal levels, 130nm) : **FEC4_P1**

- Pixel structure : identical to FEI4_P1
- Objective : test Chartered technology (functionalities, performances, radiation…)

First 3D design : **FETC4_P1**
Chartered (5 metal levels , 130nm) + Tezzaron

- One tier for the analogue pixel part,
- One tier for the digital

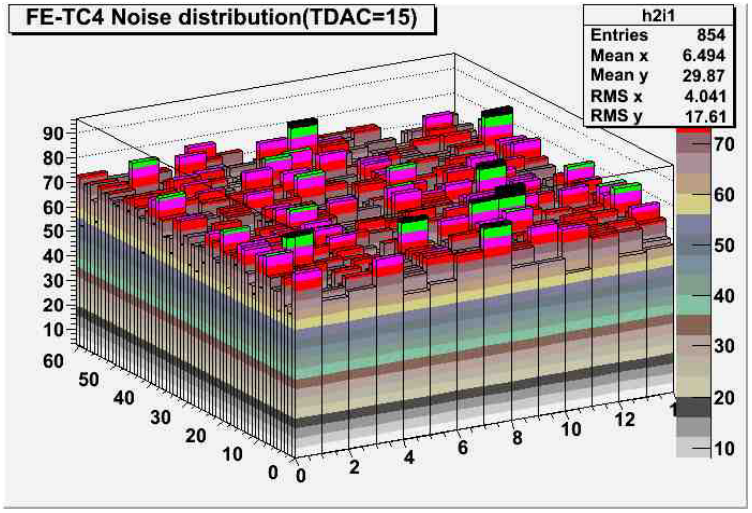
Submission: March 08
Test: Summer 08

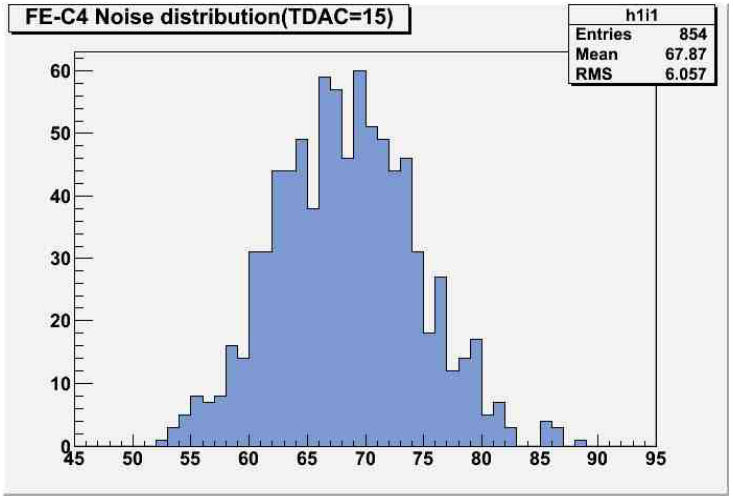
Submission: February 09
Test: April 09

Submission: Summer 2009

FEC4_P1 test results

- Due to schedule no optimization of transistors has been done
- Surprisingly, main results are equivalent to IBM ones
  - Threshold min around 1100 e-
  - Un-tuned threshold dispersion 200 e-
  - Noise lower than 80 e-



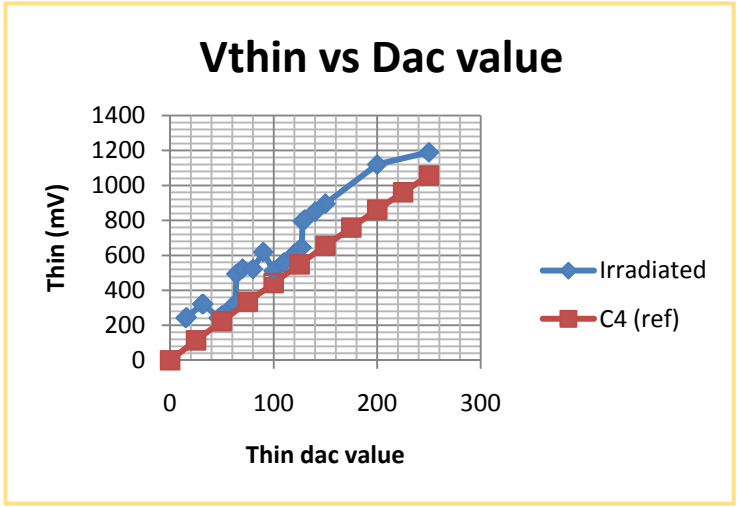


FEC4_P1 test results : Irradiations

- Irradiation performed at CERN/PS facility (24 GeV protons) up to 400 MRad
  - Problem discovered after 160 MRad on latches (output tends to be blocked in "1" state)
    - Difficult to work with the circuit by after
    - Problem reproduced in simulation "corners"

    … but

    Analog is still working even with increased of noise : 250 e- (threshold dispersion is meaningless)

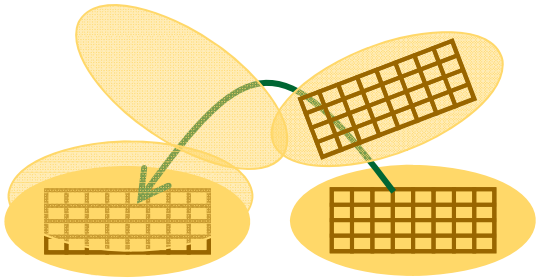


Tezzaron-Chartered 3D technology :

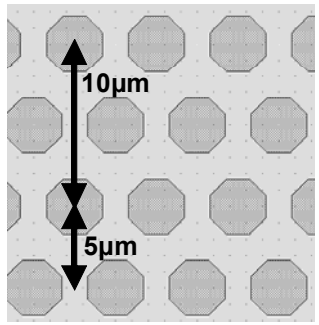
Vertical integration

Characteristics :

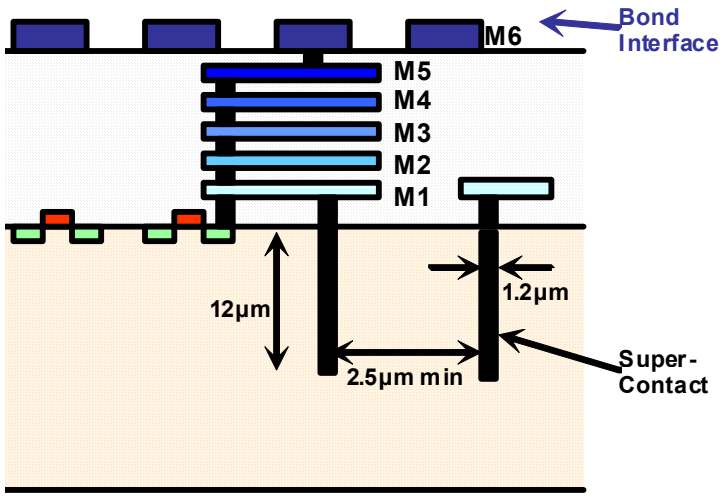
- 2 wafers (tier 1 and tier 2) are stacked face to face with Cu-Cu thermo-compression
- Via First technology : Super-Contacts (Through Silicon contacts) are formed before the BEOL of Chartered technology.
- Wafer is thinned to access Super-Contacts
- Back-side metal for bonding (after thinning)



Wafer to wafer bonding



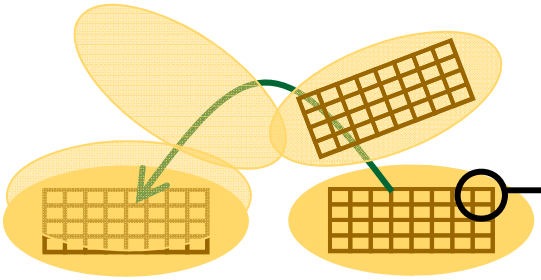
Bond interface layout



One tier

Chartered-Tezzaron MPW run

- **2 identical wafers are stacked => tier 1 and tier 2 are in the same reticle**



Chartered reticle : 26mm x 31mm shared between all participants

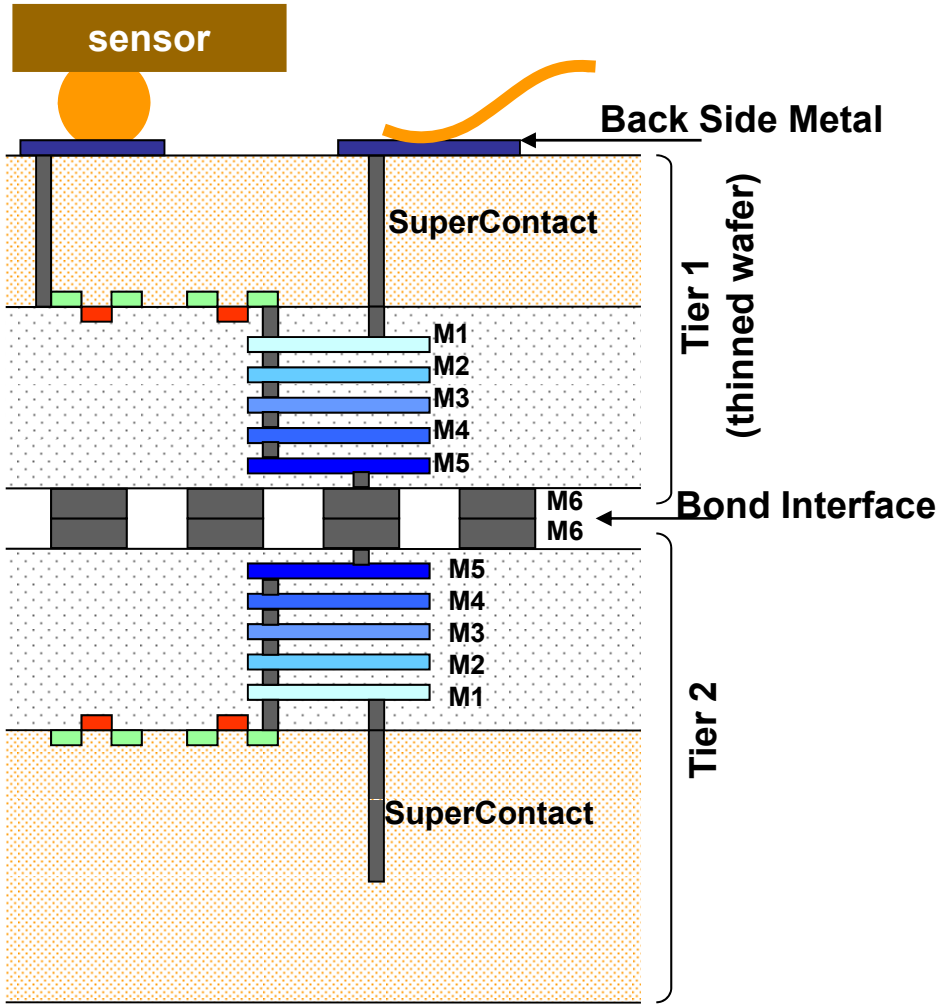
TX1	TY1	TY2	TX2
A1	B1	B2	A2
C1	D1	D2	C2
E1	F1	F2	F2
G1	H1	H2	G2
J1	K1	K2	J2

4 sub-reticles for SLHC chips projects : FE_TC4_P + OmegaPix

- ***C1, D1 = analog tier "FE-TC4-AE" + analog OmegaPix***
- ***C2 = first version for digital tier : FE-TC4-DS***
- ***D2 = second version for digital tier : FE-TC4-DC***
  read-out structure "FEI4-like"+ digital OmegaPix

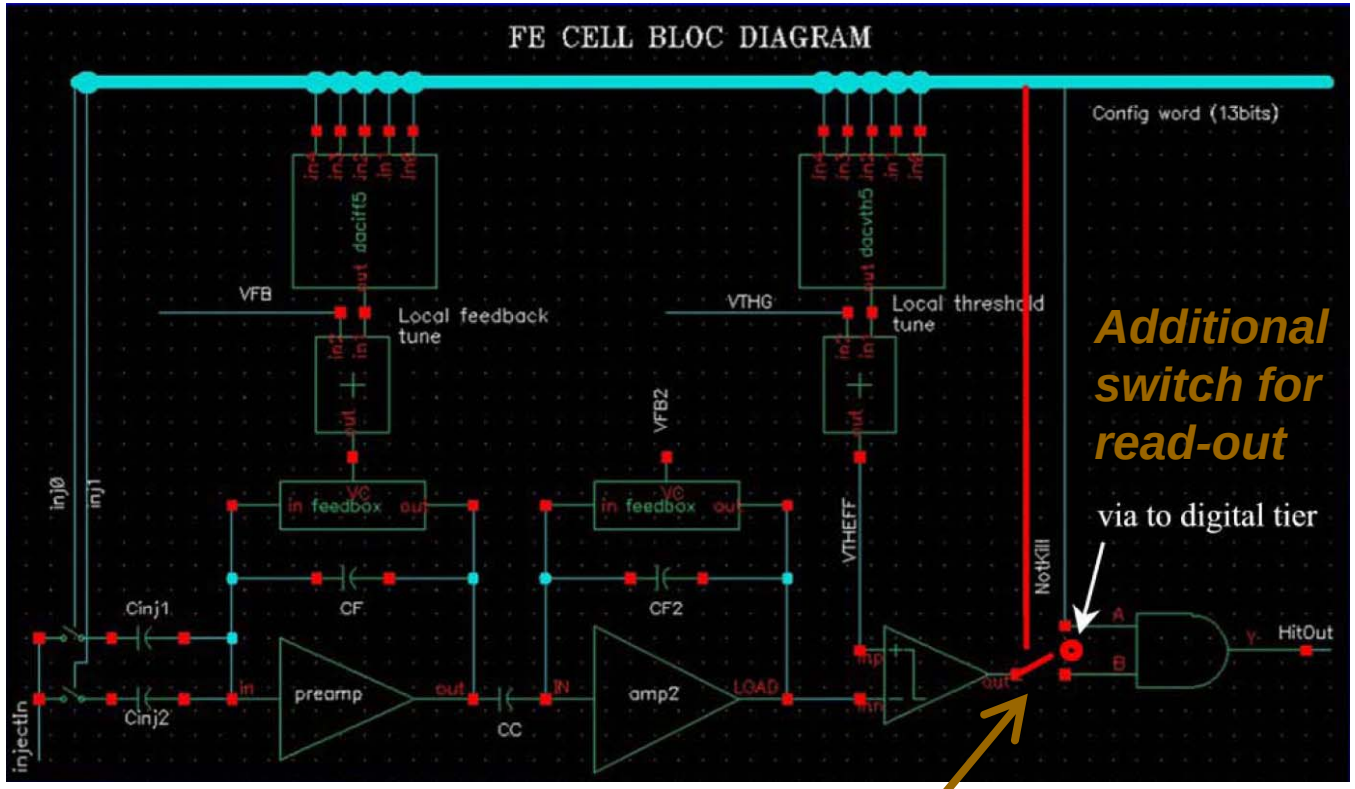
Chartered-Tezzaron MPW run

- Tier 1 (analog) is thinned to access Super-Contacts.
- I/O of the tiers are independent , each tier can be tested separately
- Analog tier has been kept kept as close as possible identical to FE_C4 , main change is the reduction to 5 metal layers



FE-TC4-AE analogue tier

- Based on FEI4_P1 pixel



Input signal from sensor, via Super-Contacts

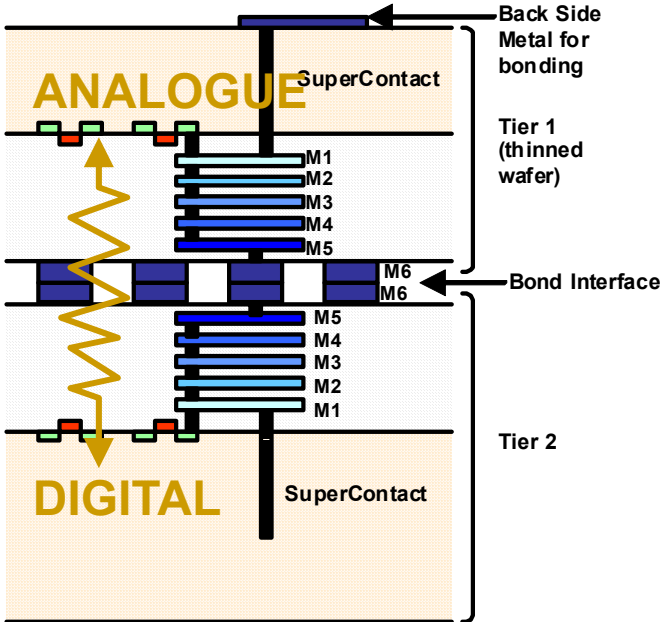
2 possible ways for discriminator output read-out:

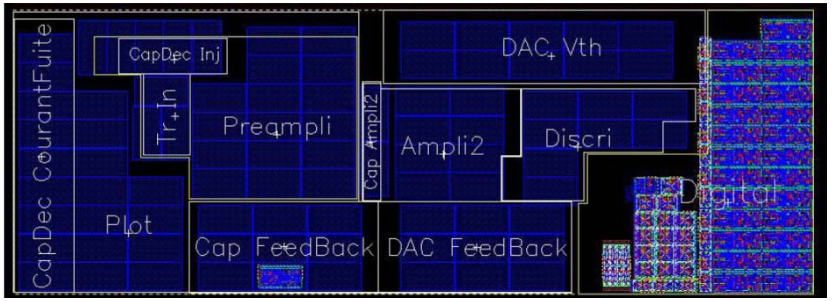
- ***With the simple read-out part existing yet into the pixel***
- ***With the tier 2 (via the Bond Interface)***

FE-TC4-DS digital tier dedicated for test

Parasitic coupling study between tier

- Analogue tier and digital tier are face to face (sensitive part facing digital part).
- FE-TC4-DS : dedicated for parasitic coupling studies between the 2 tiers.
- 3 functions :
  - Read the discriminator output
  - Generate noise (digital commutations) in front of 11 specific areas of the analogue pixel (preamplifier, feed-back, amplifier2, DAC…)
  - Test different shielding configurations.

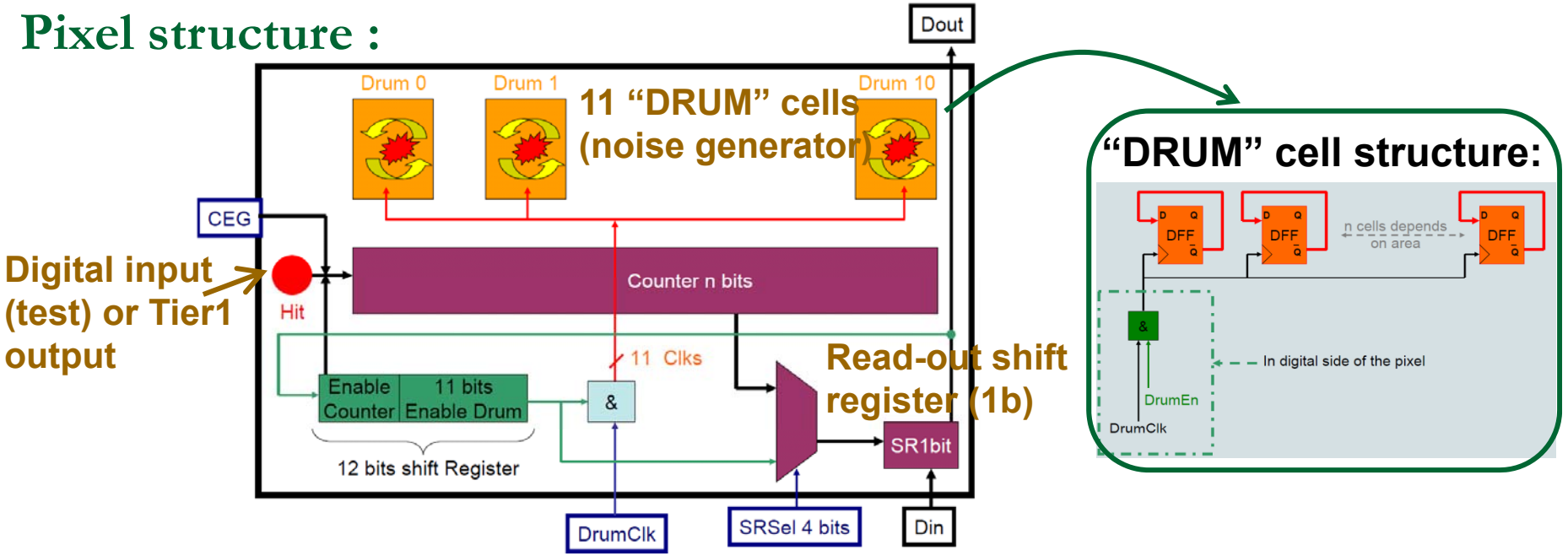




Analogue pixel layout : 11 specific areas

FE-TC4-DS digital tier dedicated for test

Pixel structure :



Shielding strategy :

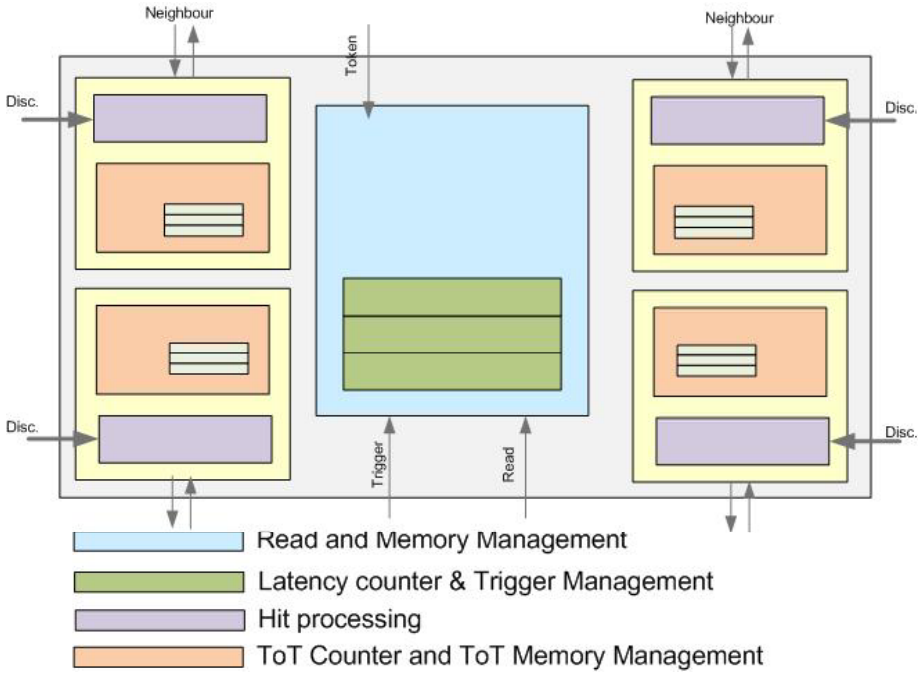
- 5 columns without any shielding (reference),
- 4 columns with shielding in metal 5,
- 2 columns with shielding in metal 3,
- 2 columns with both shielding.

FE-TC4-DC digital tier

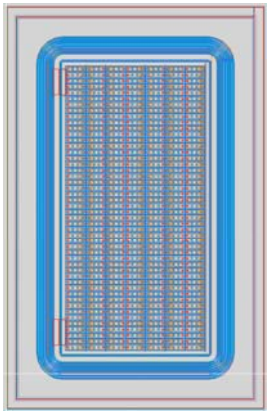
Complex read-out chip

Read-out chip similar to what is foreseen for FE-I4:

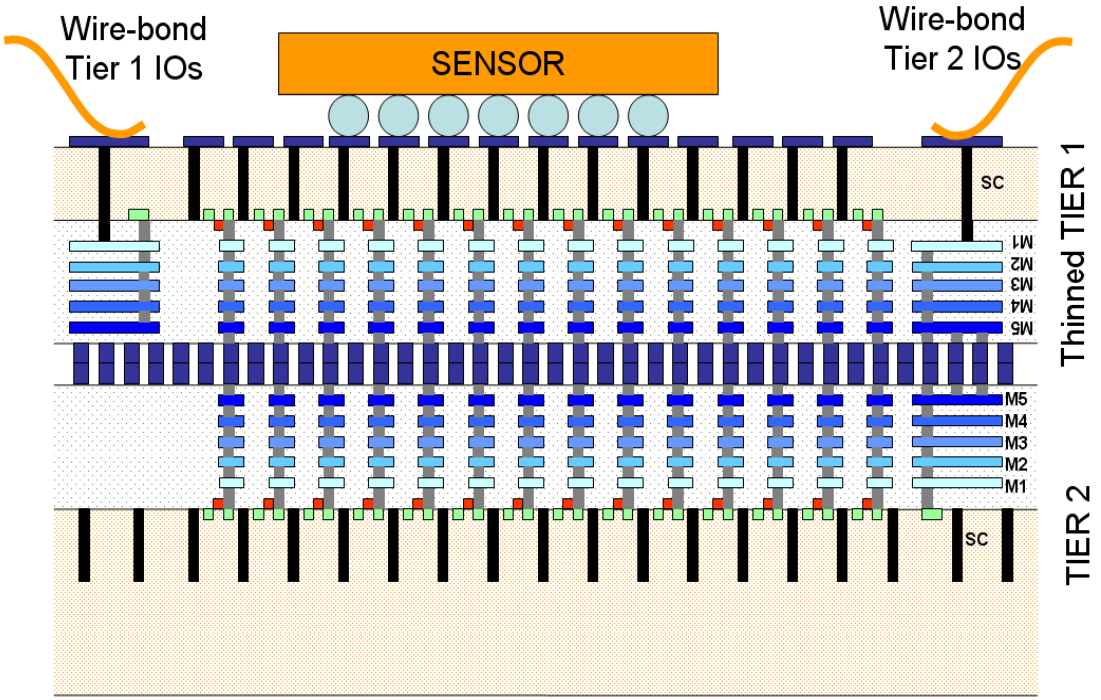
- **4-pixel region :**
  - 61 pixels/ column => implies 31 ‘4-pixel’ regions plus 2 dummy pixels per double-column.
- **Simplified periphery and read-out control logic :**
  - Some signals are provided from the outside (data read-out signals, signals for pixel hits communication to the periphery…



Final assembly with sensor



Sensor layout :
Anna Macchiolo, Max-Planck-Institut für Physik, Munich



Bonding foreseen to be done at IZM (Berlin) as for ATLAS modules

Due to geometric constraints, sensor matrix is reduced :

- Sensor matrix : 7 columns of 48 pixels
- Tier 1 and Tier 2 matrix : 14 columns of 61 pixels

Conclusions and future plans

- Benefits of 3D technology for hybrid pixel detectors appear evident :
  - Pixel size reduction
  - Technologies mixing
  - More functionalities can be implemented in front of the analogue pixel
- By the end of the year :
  - Tests will be performed on FETC4_P1
  - Design and production of FEC4_P2 (transistor optimization and few minor corrections) , submission beginning of November
  - Start working to design a full scale FETC4

Conclusions and future plans (con't)

- FE_C4 chip
  - Chip size the 18.8 x 20.1 mm (336 rows x 160 columns, EOC 1.95 mm)
  - Pixel pitch 50*125 µm, same technology as FE_TC4_P1
  - Bump bond pads compatible with 250 µm sensor pitch
  - Keep the possibility of different flavors in some columns
  - **Pros:** FE_I4 blocks reuse, compatibility with FE_I4 chip for sensors, bump bonding , module/stave integration, testing tools, software, mechanics
  - **Cons:** cost -> Needs 2 sets of mask (the chip cannot fit in ½ reticle)

Run foreseen by first half of 2010

ALL GROUPS INTERESTED IN SHARING THIS RUN ARE WELCOME

(50 % of the reticle area is available)