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3D electronics for hybrid pixel detectors

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Facing the future challenges of hybrid pixel vertex detectors is foreseen to be done by microelectronic technology shrinking. However, this straightforward approach has some disadvantages in term of performances and cost. Based on a previous prototype of the future ATLAS pixel read-out chip FE-I4, this paper presents design and test of a hybrid pixel read-out chip using 3 dimensional electronics technologies which enable to split pixel functionalities into two separate levels.

Summary

Hybrid silicon pixels detectors featuring high spatial resolution, very good signal to noise ratio and true two-dimensional information are currently used as vertex detectors in High Energy Physic experiments and especially in ATLAS and CMS detectors at the Large Hadron Collider (LHC).
Future requirements of post-LHC accelerators are, as usual, one step beyond the actual ones. Facing these new challenges could be addressed by 3D technologies which offer an alternative way of 2D shrinking with the advantages of technology mixing and cost effectiveness.
Starting from the FE_I4 prototype design (14×61 pixel matrix) in IBM 130 nm, which is a test pixel read-out chip for ATLAS upgrades, we developed 3D variants in Tezzaron-Chartered 130nm technology called FE_TC4.
In these variants, pixel functionalities are split into 2 levels (so-called tiers), the first one housing the analog pixel and sensor connections and the second one sheltering all digital related blocks. These two tiers are then connected face to face by copper bonds and the resulting pixel dimension before any real optimization was scaled down from 50×250µm to about 50×160µm.
One of these 3D circuits contains "special" digital blocks dedicated to the detailed study of the parasitic coupling between tiers, the other one has a more realistic digital design including the "4-pixel region" architecture which is foreseen for ATLAS pixel Front-End IC upgrades.
Silicon sensor has been also designed in order to address bump-bonding issues in this new type of chip stacks.
Design issues and complete tests results will be presented.

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