The Level 0 Trigger Decision Unit for the LHCb experiment

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Outline

The LHCb detector

Purpose

Dedicated to the b physics at the LHC

Features

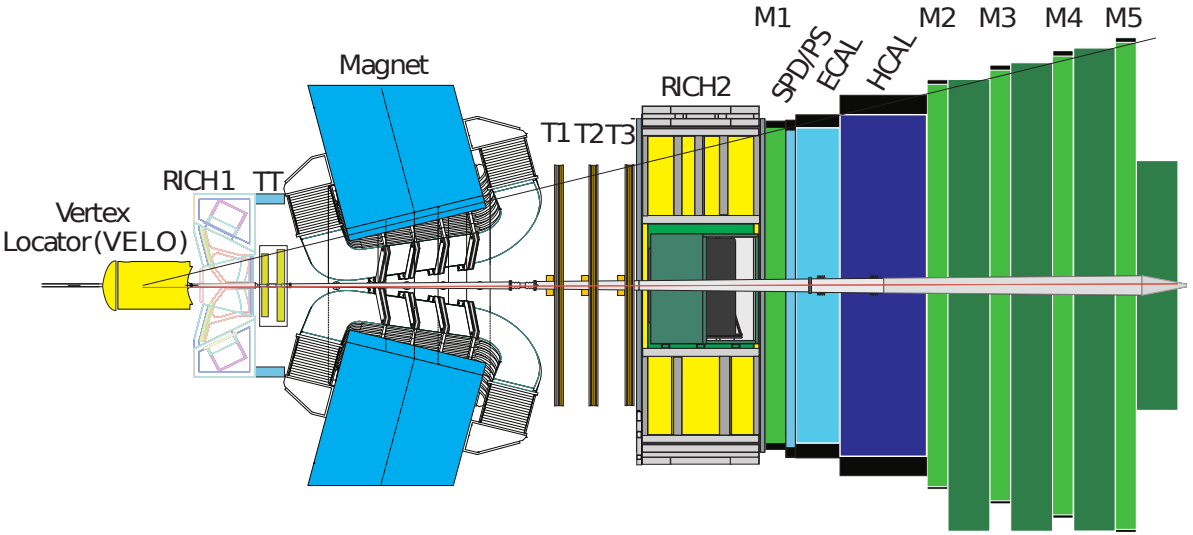
- Collision at 14 TeV
- b and $\bar{b}$ produced at small angles and correlated

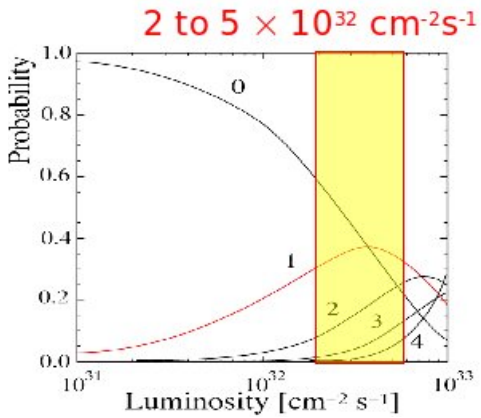
$\rightarrow$ forward spectrometer ($\theta \in 15/300 mrad$)

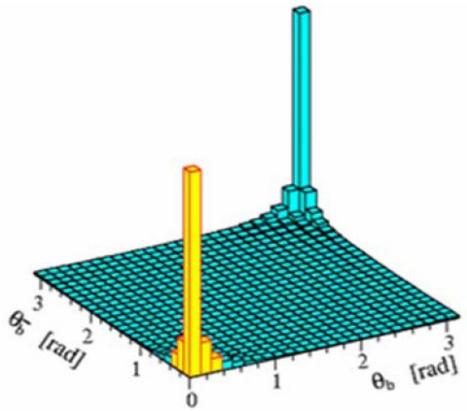
- Small branching ratios of interesting b decays

$\rightarrow$ 1Hz for a BR of 10^{-4} (over 10MHz of visible interactions)

- The trigger system is the key







LHCb

Two levels of trigger

L0 trigger

- Custom electronics
- Synchronous system (40MHz)
- Fixed latency ($4\mu s$)
- Use the fastest detectors
- Output rate $< 1MHz >$

High Level Trigger (HLT)

- PC farm ($\approx$ 2000 CPU)

1. Fast tracking

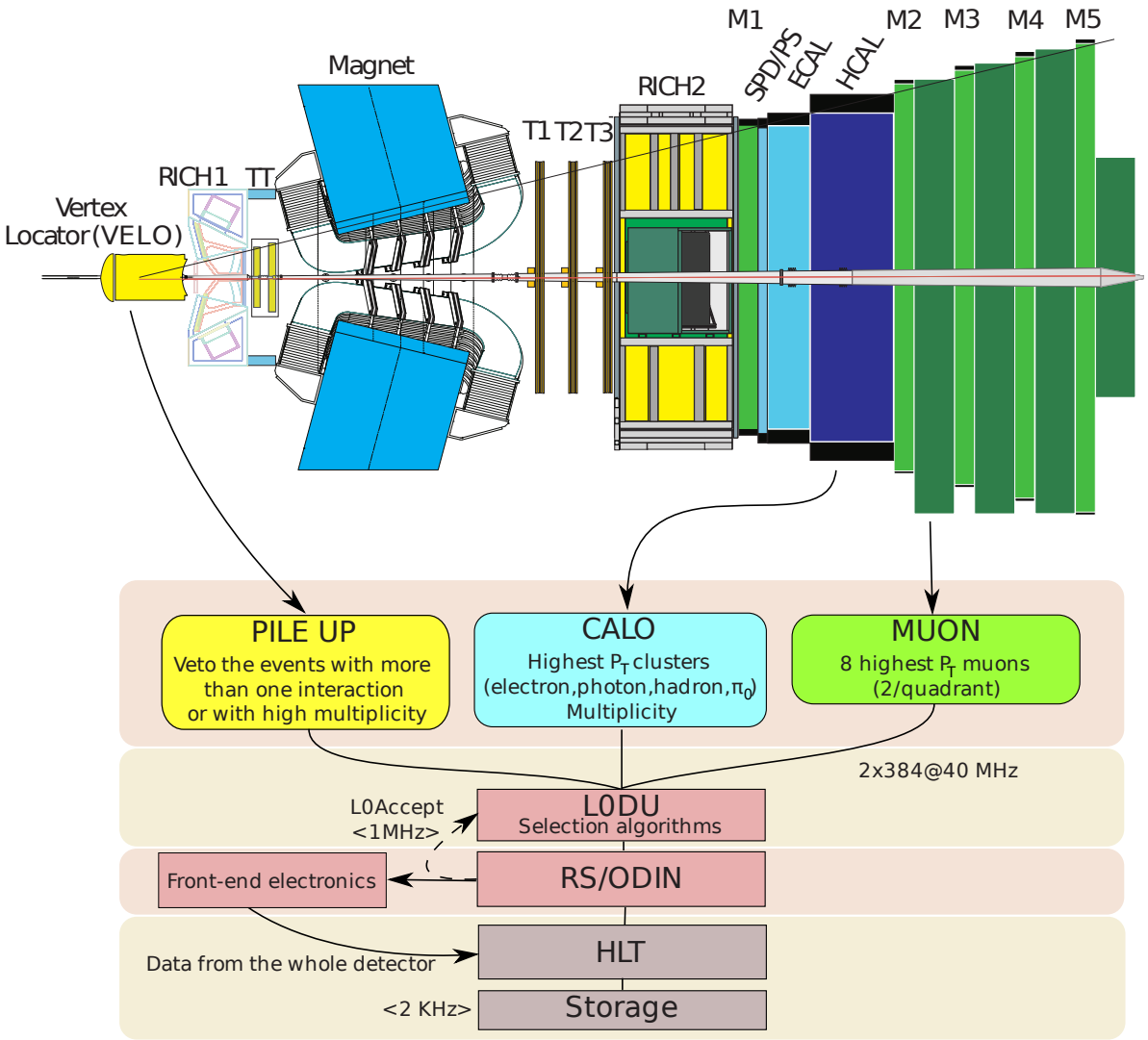
$\longrightarrow$ L0 Confirmation

$\longrightarrow$ impact parameter cuts

2. Almost full event reconstruction

- Storage at $< 2kHz >$

$\longrightarrow \approx 35kB$ by event

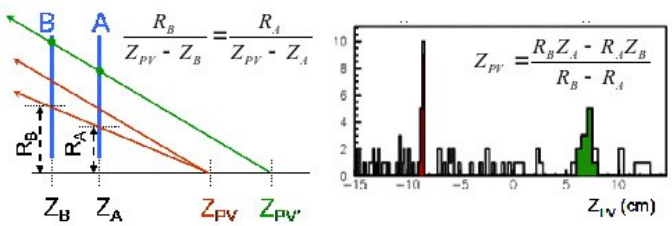


LHCb and its trigger system

The L0 Trigger

Subtriggers

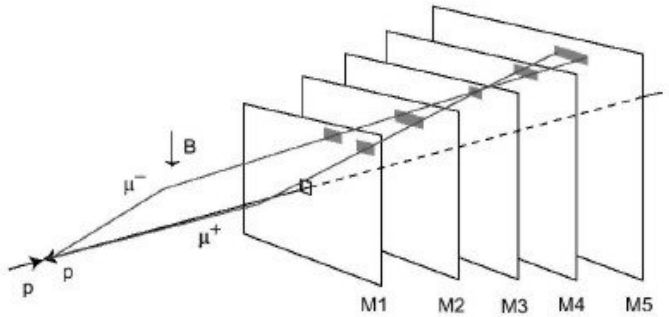
- Pile Up system
- → 2 silicon plane before the interaction point
- → Primary vertexes multiplicity (veto on pile-up events)
- Calorimeter trigger :
- → Highest E_T γ, electron, π^0, hadron
- → $\sum E_T$ and SPD multiplicity
- Muon trigger
- → Two highest p_T muons / quadrant



Pile Up Veto histograms

Two core boards

- The L0DU :
- → L0 Decision
- → Highly flexible triggering algorithms
- The Readout Supervisor (RS)
- → Broadcast the decision, the clock and synchronisation signals
- → Check the DAQ occupancy



Muon trigger

The L0DU environment

Inputs

- Concentrate the data from the L0 sub-triggers
- All inputs are optical :

→ 24 different clocks

- Optical TTC (Timing, Trigger and Control) input

→ LHC clock

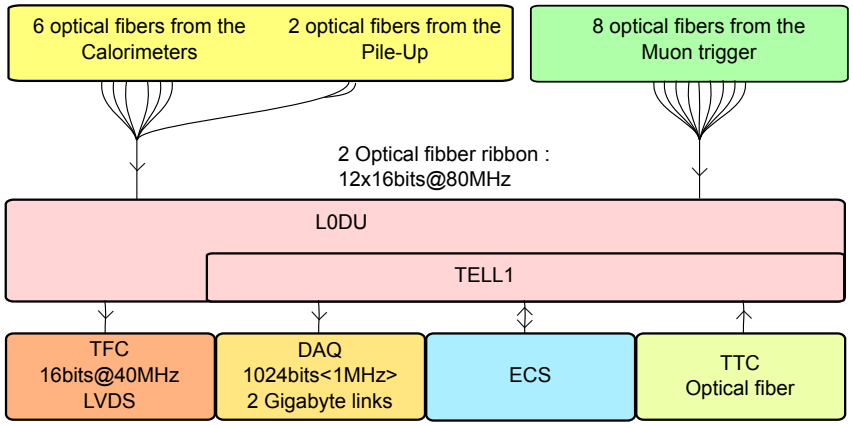
→ Synchronisation signals

Outputs

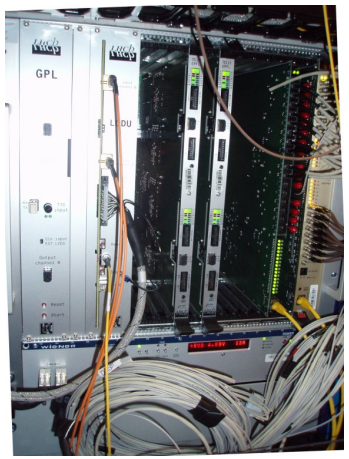
- Decision output to the Readout Supervisor (RS)
- Internal processing summary for the DAQ

Experimental Control System (ECS)

- Ethernet connection



L0DU interfaces



L0DU at the experimental site

The L0DU and TELL1 board

TELL1

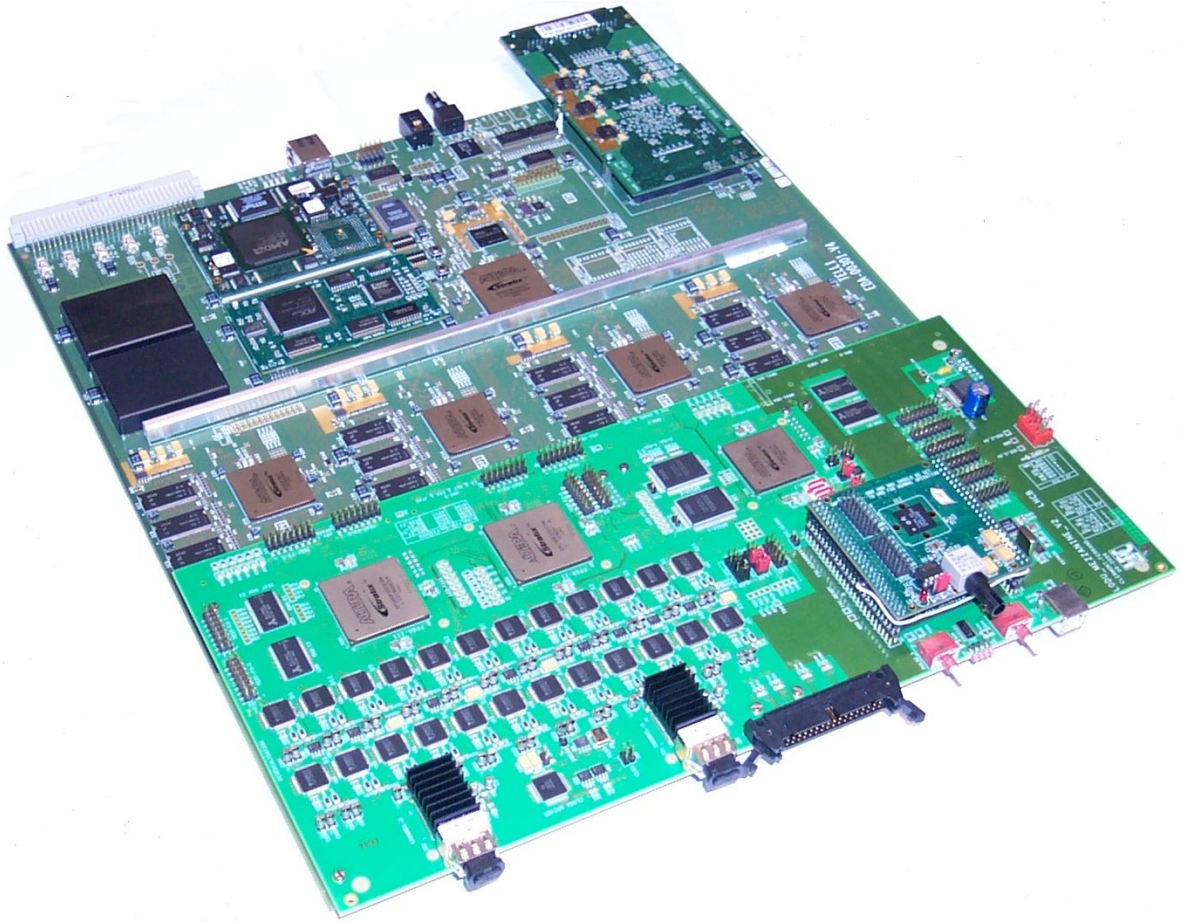
- Common interface board for LHCb
- Provide access to the ECS using a small embeded PC (CCPC)
- Provide DAQ output (Quad-Gigabyte board)

L0DU ECS

- Registers access : I^2C bus
- Firmware upgrade : JTAG bus

L0DU DAQ

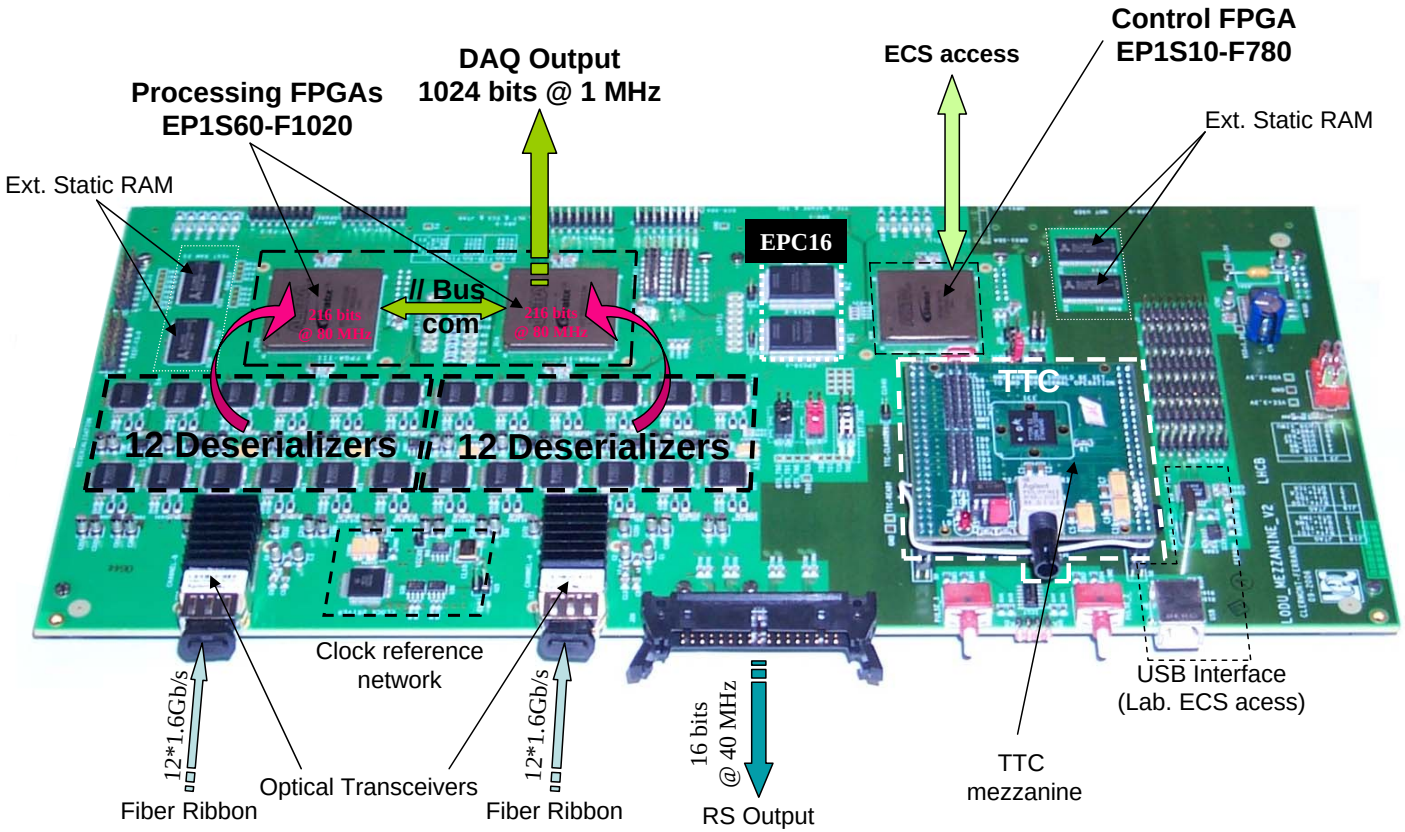
- TELL1 FPGA used to transmit the L0DU DAQ frame



L0DU and TELL1 boards

The L0DU mezzanine

16 layers 9U board



L0DU elements

The L0DU processing architecture

2 FPGA for the processing

- L0DU algorithms in FPGA1
- Monitoring in FPGA2
- 65% of the available logical ressources in FPGA1

Main characteristics :

- Fully configurable algorithm using 128 conditions
- Low dead time for algorithms changes
- 40MHz pipeline architecture

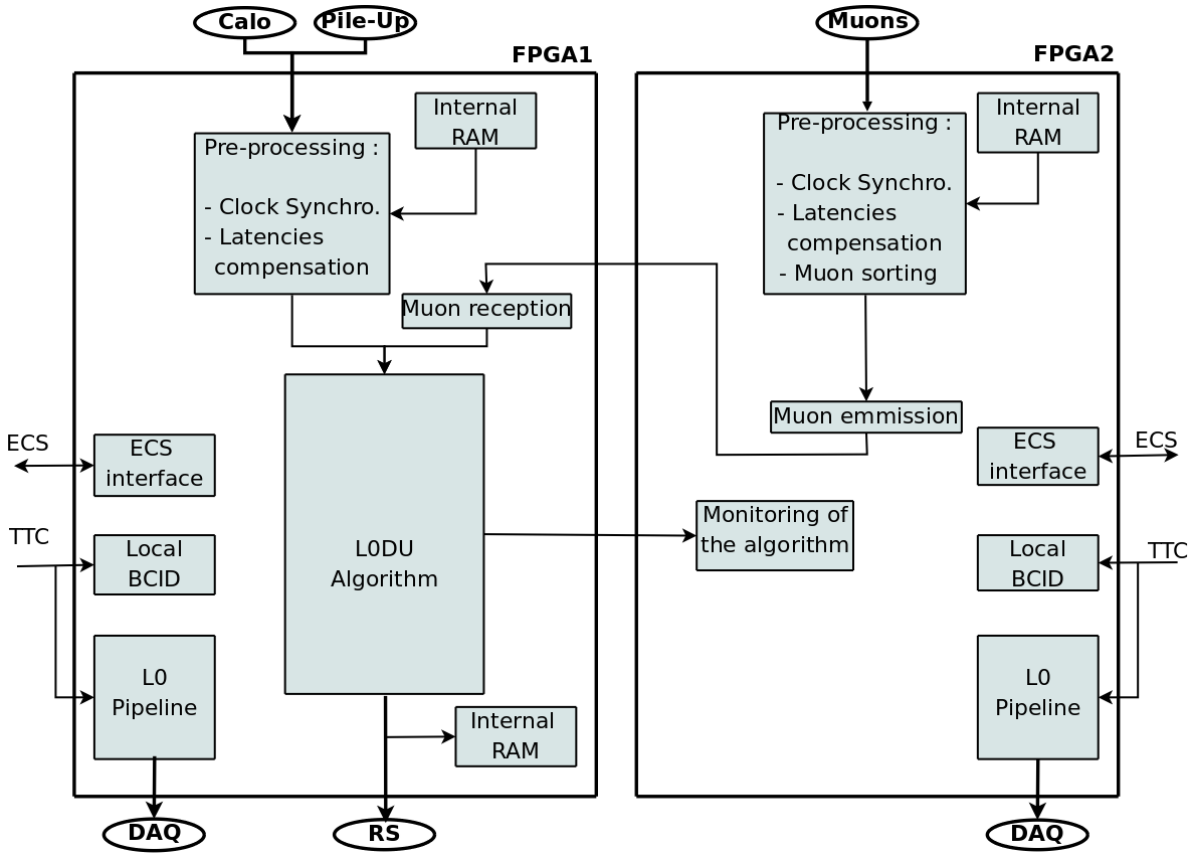


Figure: FPGA1 and FPGA2 processing

Two steps : pre-processing and L0DU algorithms

Pre-processing

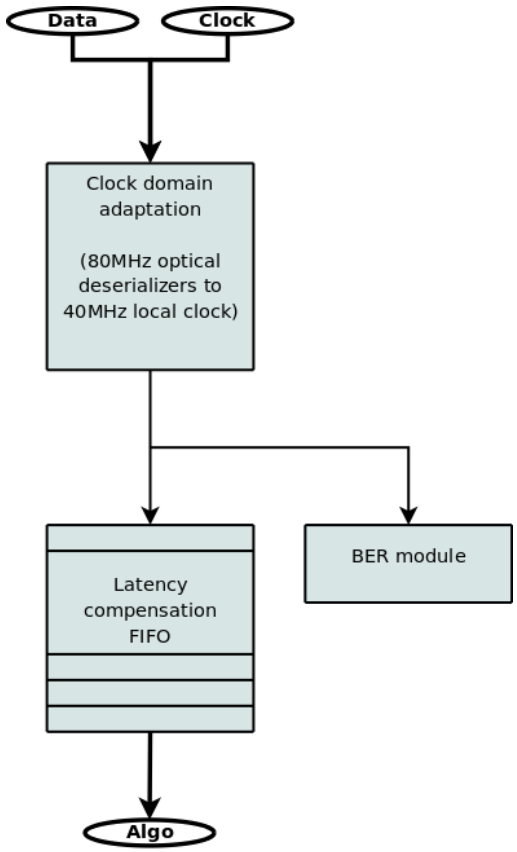
Pre-processing (for each input) :

- Clock domain adaptation

→ 24 input clocks at 80MHz with unknown phases

→ 1 local clock at 40MHz

- Data demultiplexing (16 to 32 bits)
- Compensate the difference between the L0 sub-trigger latencies
- BERT (Bit Error Rate Test) module for optical links



FPGA1 pre-processing for one input

Pre-processing : Clock domain adaptation

Purpose

- Adapt to the 40MHz local clock the data from the optical deserializers
- Demultiplex the data

Clock domain

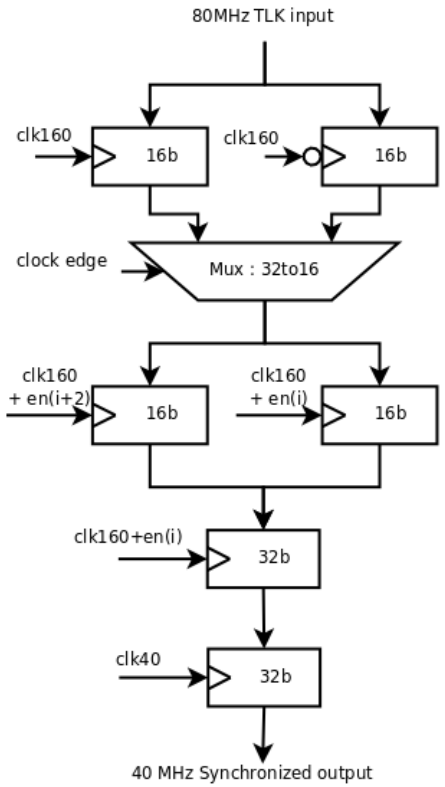
- 160MHz transition clock

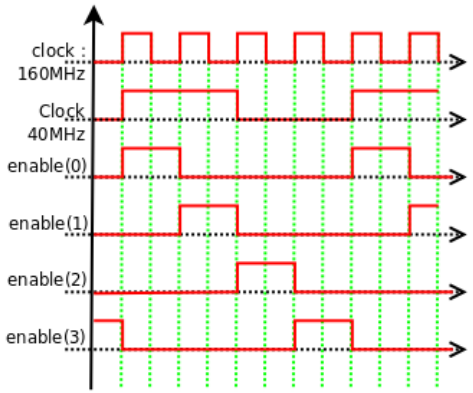
→ Acquisition phase step of 3.12 ns (rising and falling edge)

→ Use 2 dedicated clock network of the FPGA

Demultiplexing

- Dedicated bit in the data : MSB/LSB
- Translate the acquisition point to get the MSB at the right position





Clock domain adaptation principle

Pre-processing : Clock phase determination algorithms

1. Wait all clock domain adapter to be ready
2. Acquire 256 times 80MHz input clock at the rising and falling edges of the 160MHz clock with enable(0)
3. If more than 128 '1' at pt0 (rising edge) have been acquired then acquisition results for pt0 is setted to '1', same for pt1 (falling edge)
4. Same as 2. with enable(1)
5. Same as 3. with pt2 and pt3
6. Use a LUT to select the right phase of the clock

Acquisition results				Phase
enable(0)		enable(1)		
pt0	pt1	pt2	pt3	selected
0	0	0	0	ERR
0	0	0	1	2
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	ERR
0	1	1	0	0
0	1	1	1	1
1	0	0	0	3
1	0	0	1	2
1	0	1	0	ERR
1	0	1	1	2
1	1	0	0	3
1	1	0	1	3
1	1	1	0	0
1	1	1	1	ERR

Table: Clock phase selection LUT

The L0DU algorithms

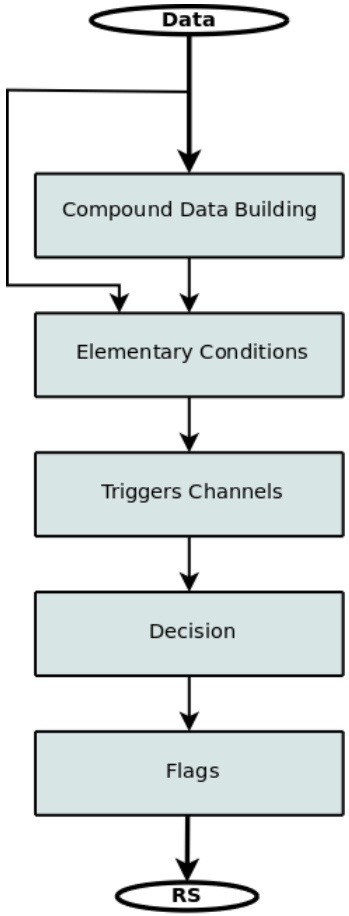
Algortihm

The L0DU algorithms makings involve multiple steps

Inputs

Extracted from the optical inputs data :

- The E_T and the address of the highest energy γ, electron, π_l^0, π_g^0, hadron
- The $\sum E_T$ in the calorimeter and the SPD multiplicity
- The first and second Pile-Up peak content and position
- The three highest p_T muons address and p_T



L0DU Algorithm

The L0DU algorithms

30 compound data

- Sum or difference of the E_T (resp. p_T) of up to 3 particles
- Mask on the address of a particle

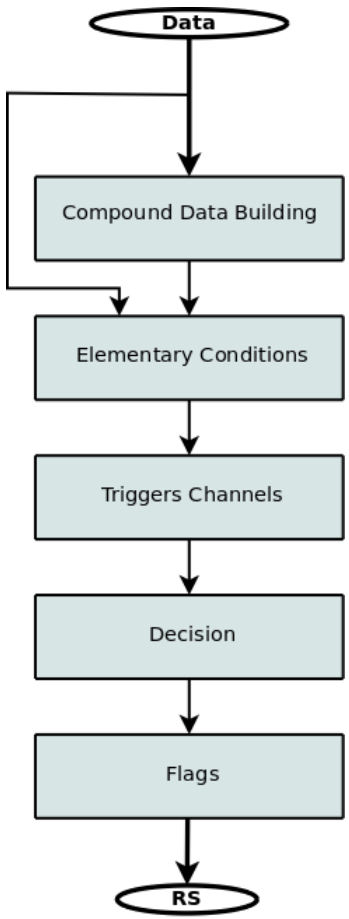
Example :
$E_T(electron) + E_T(\gamma)$
$Address(electron)\&0xFF$

128 elementary conditions

A threshold with an operator (=, $\neq$, > , <) on

- A data extracted from the inputs
- A compound data
- A RAM stocking a 8 bit value for each BCID (possible to account for beam/beam structure for example)

Example :
$E_T(electron) > 10$



L0DU Algorithm

The L0DU algorithms

32 trigger channels

An “and” network on the elementary conditions
Example :
$E_T(electron) > 10\, and\, E_T(photon) < 6$

1 decison

An “or” on the trigger channels

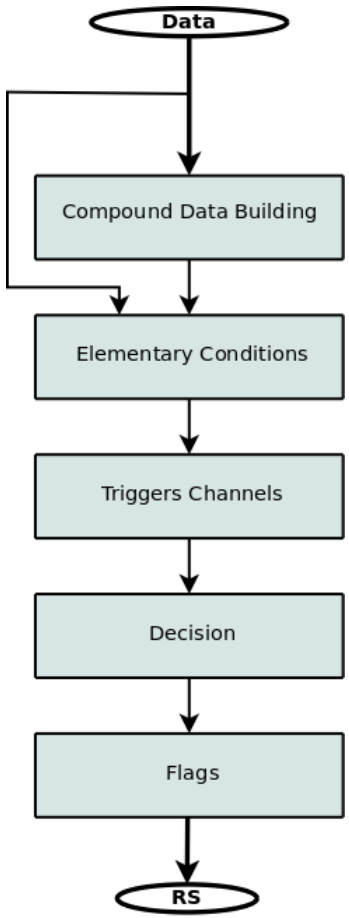
Decision Flags

Force trigger bit :

- Setted when an error is detected in links demultiplexing or time alignement, or if a status bit from a sub-detector is setted

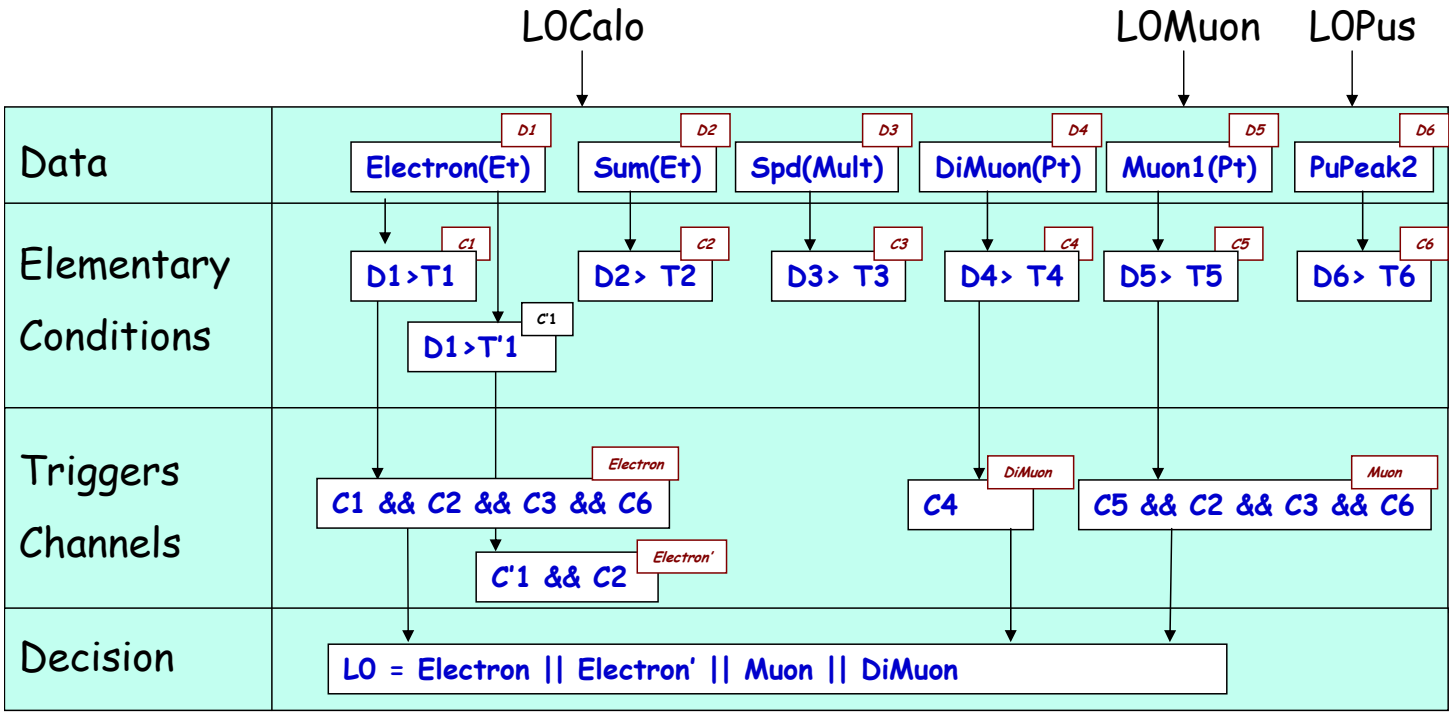
Timing trigger bit :

- Setted at ’1’ when a special series of 5 L0 decision is detected or in the decision of a simpler algorithm involving only $\sum E_T$



L0DU Algorithm

Algorithms : An example



Each trigger channel can be downscaled in steps of 0.1%.

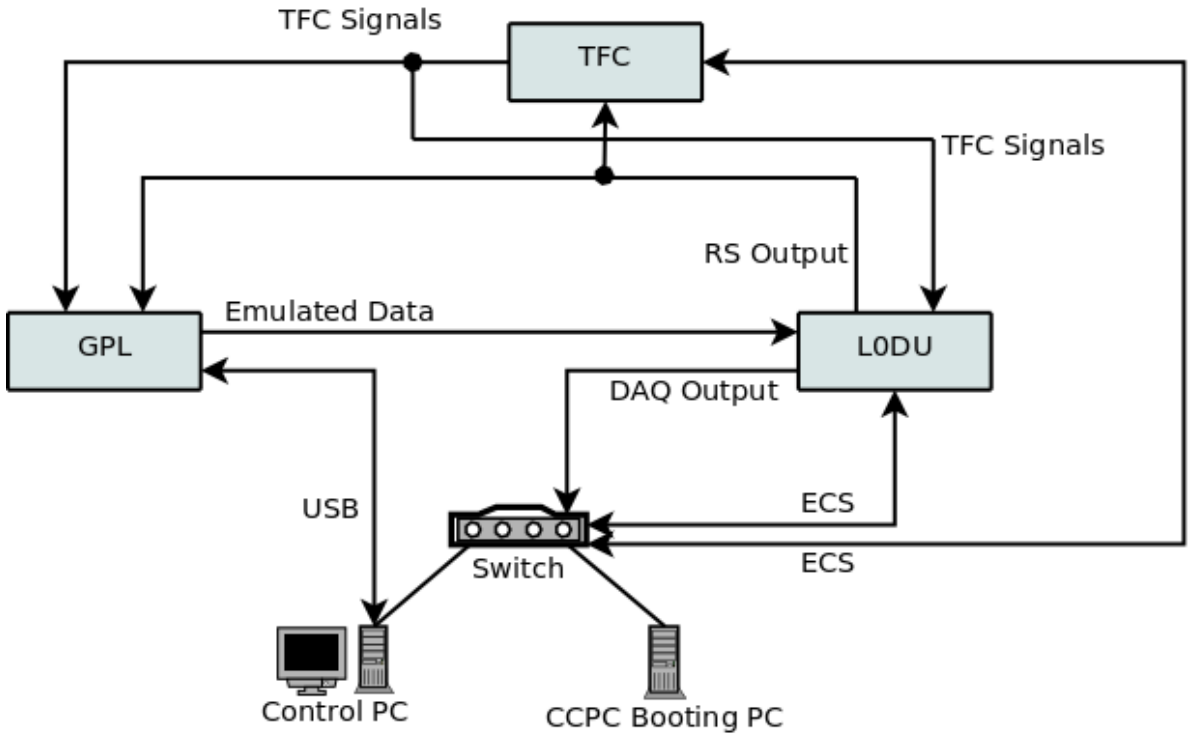
L0DU test bench

The test bench allows to :

- Stress the optical links
- Test the firmware

Main components :

- Stimuli pattern generator : the GPL board
- PC to control and program the boards
- TFC system for the clock and synchronisation signals distribution



L0DU test bench

The GPL board

The GPL board

- Built as a mirror board of the L0DU

→ 2 processing FPGA

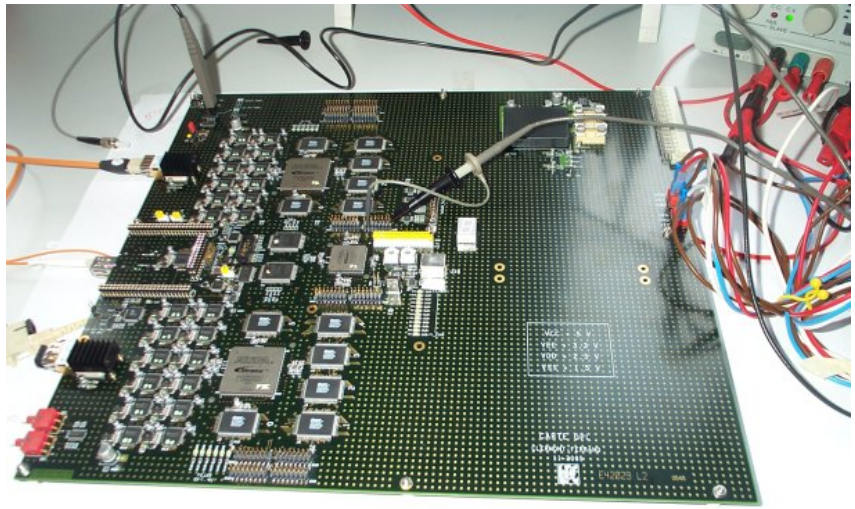
→ Same layout for the optical part

- Control : USB interface
- Test modes :

1. Send up to 10 LHC cycles of patterns
2. Send a continuous counter for the BERT

Hardware

- 16 layer boards
- 2 FPGA Stratix 1P1S40 and 1 1P1S10 from Altera
- Optical part : Texas instrument TLK



GPL board

Timeline

2002 First L0DU prototype

→ Concept board

→ No interfaces with the ECS and the TFC

2006 Second L0DU protoype

→ All functionalities implemented

→ FPGA ressources too limited

2007 Final L0DU prototype

Feb. 2007 Installation of the L0DU in the experimental area

Feb. 2007 Initial time alignment

Apr. 2007 First tests with the calorimeter trigger

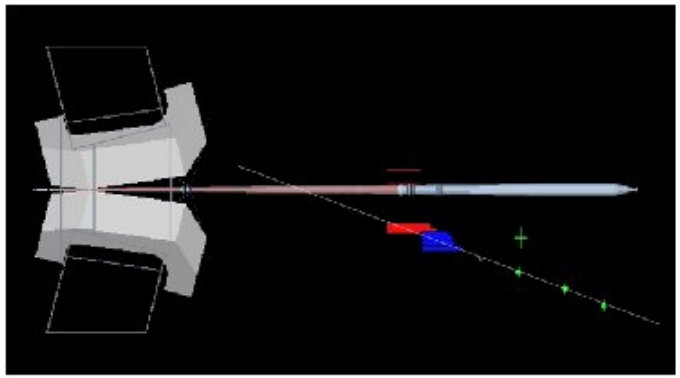
Apr. 2007 First tests with the muon trigger

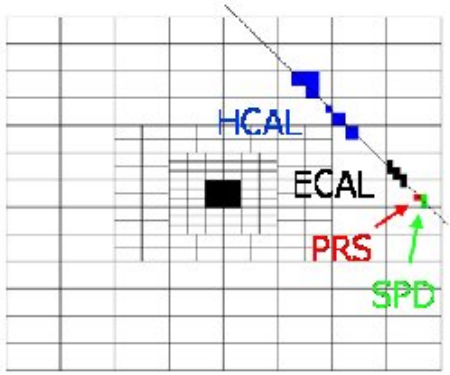
Dec. 2007 First cosmics taken with the calorimeter trigger

Apr. 2008 First cosmics taken with the muon trigger

Aug. 2008 First beam induced particles

Dec. 2008 First tests with the Pile-Up





Cosmics spotted in LHCb

Summary

- A very flexible L0 trigger board has been developped

→ Works since 2007

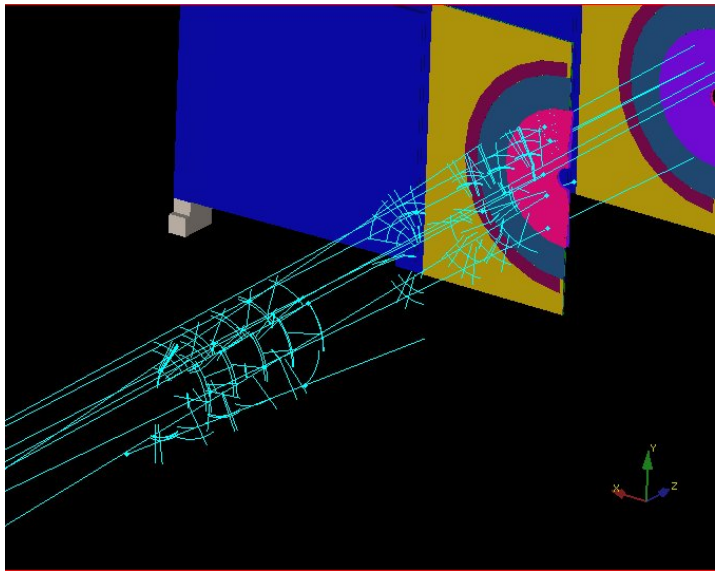
→ Small evolution since

- Extensively used at the experimental site

→ Commissioning of the detectors

→ Millions of cosmics have been recorded

- L0DU used to trigger on TED events and record very usefull Velo tracks
- First beam induced data triggered with L0DU on September 10, 2008
- Ready for the beam



Recorded Velo tracks