Contribution ID: **71** Type: **Oral**

LHCb Level 0 Decision Unit

Wednesday, 23 September 2009 11:00 (25 minutes)

The Level 0 Decision Unit (L0DU) is one of the main components of the first trigger level of the LHCb experiment. This 16 layers custom board receives data from the calorimeter, muon and pile-up sub-triggers and computes the level 0 decision, reducing the rate from 40MHz to 1MHz. The processing is implemented in FPGA using a 40MHz synchronous pipelined architecture. The L0DU algorithm is fully configured via the Experiment Control System without any firmware reprogramming. An overall L0DU latency of less than 450ns has been achieved. The board was installed in the experimental area in April 2007. It has played a major role in the commissioning of the experiment.

Summary

The trigger of the LHCb experiment is based on two levels. The first one, called level 0, makes use of custom electronics and should reduce the rate from 40MHz to 1MHz. The second trigger level, called High Level Trigger (HLT), is implemented on a farm of CPU.

The Level-0 Decision Unit (L0DU) is the central part of the first trigger level. The L0DU receives information from the calorimeter, muon and pile-up sub-triggers at 40MHz. The sub-triggers send their data via 17 high speed optical links transmitting at 1.6Gb/s. Each contains 16bits@80MHz of data with its particular clock. The L0DU is designed to cope with up to 24 such input links.

The L0DU computes the level 0 decision and sends it to the Readout Supervisor using a dedicated 40MHz LVDS link. The Readout Supervisor can veto the decision depending on the electronic workload. When an event is accepted, the L0DU sends an explanation block to the HLT. This block contains the kind of triggers fired by the event and is the starting point of the HLT processing.

The L0DU is plugged on a TELL1 board which is the standard Data Acquisition interface module used in LHCb. The TELL1 board interfaces the Timing and Trigger Control and the Experiment Control System (ECS) via a small embedded PC.

The L0DU is a full custom 16 layers board. The processing is implemented in 3 FPGA in BGA package using a 40MHz synchronous pipelined architecture. A smaller FPGA is dedicated to the synchronization and the ECS. The processing is done in two larger FPGA. It is split in two: a pre-processing block and a trigger definition block. The pre-processing block acquires and time-aligns the input data. It also handles specific counters to monitor the status of the links and check the time-alignments.

The trigger definition block implements up to 128 configurable comparisons. These elementary conditions are then combined using up to 32 fully configurable 'and'networks. This defines the trigger channels. The decision is finally built as the result of an 'or'network on the 32 trigger channels. This 'or'network is also configurable to enable or not any trigger channel. Between the 'and'and the 'or'networks, each trigger channel can be downscaled with a downscaling factor configurable in steps of 0.1%. The trigger definition block also implements its own counters to monitor the various trigger rates.

The overall L0DU latency is lower than 450ns. The trigger definition block is very flexible. It is fully set up via ECS. The L0DU can then cope with very different running conditions or physical priorities without any firmware reprogramming.

The L0DU board has been installed in the experiment in April 2007. It has played a major role in the commissioning of the experiment in general and of the level 0 trigger in particular. The first cosmic events were recorded in late 2007 triggering on calorimeter data. A cosmic trigger based on tracks reconstructed in the muon system was setup in spring 2008. Dedicated configurations of the L0DU also allowed triggering and recording beam dump events associated to the commissioning of the LHC itself in summer 2008.

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Session Classification: Parallel Session A3 - Trigger

Track Classification: Trigger