A latchup topology to investigate novel particle detectors

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Abstract

Here the latchup effect is described as a novel approach to detect and read out particles by means of a solid-state device exploiting latchup topology. The paper first describes the state-of-the-art of the project and its development over the latest years, then the present and future studies are proposed. An elementary cell composed of two transistors connected in a thyristor structure is shown. A first prototype uses MOS transistors, resulting an even more promising and challenging configuration than that obtained via bipolar transistors. A second version of the circuit exploits a commercial SiC MESFET as sensing device. As the MOS transistors are widely used at present in microelectronics, a latchup topology is proposed as a novel structure for future applications in particle detection, amplification of signal sensors and radiation monitoring.

I. INTRODUCTION

This paper presents a work that started just few years ago, when the authors – in particular A. Gabrielli and G. Villani - were investigating redundant logic circuits against Single Event Effects (SEE) [1] and studying new structure to reduce the in-pixel power consumption, respectively. In particular, SEE originate when an overthreshold charge is deposited in sensible nodes of microelectronics devices. Hence, while studying and investigating on these effects the two authors, independently of each other, had the idea to exploit one of the most dangerous of the SEE: the latchup effect [2]. The topology corresponding to this effect - a thyristor - could be exploited as a powerful means of achieving the precise detection and positioning of a broad range of ionising particles or, for example, the proposed device can only be used as a readout circuit for amplification and latching of a variety of signals provided by sensors for high-energy physics experiments. In fact, the circuit takes the function of the data acquisition chain that is to date designed within any pixel of pixel detectors widely used, for example, in experiments [3, 4, 5] of the Large Hadron Collider. Although the principle was already proved in the past [6, 7], a novel prototype has been designed, constructed and tested and some new results are presented below.

II. A FIRST PROTOTYPE

Figure 1 shows two MOS transistors instead of the bipolar devices that create the well-known latchup circuit. Figure 2 shows how the circuit has been implemented via commercial MOS components. In more detail, by connecting the MOS transistors extracted from CMOS inverters after having disconnected the power pin of the N-MOS and the ground pin of the P-MOS, the two individual transistors became available. In this way we exploited submicron MOS transistors without fabricating an integrated version of the cell, which is to be done in the next future in any case. Figure 3

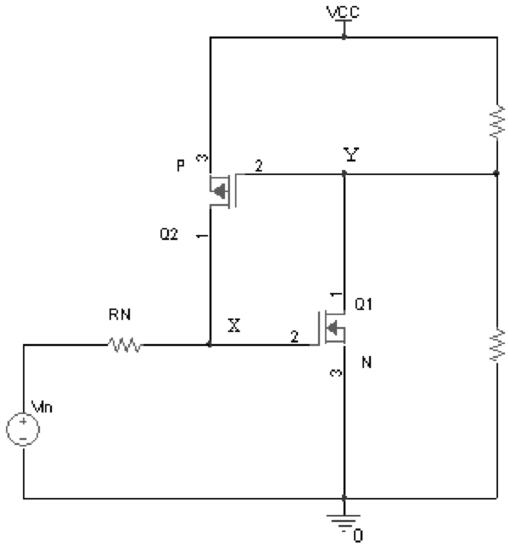

Figure 1: Latchup topology

shows a test board provided with many jumpers and variable resistors to easily configure and bias in several ways the circuit. Figure 4 shows an oscilloscope plot of the cell under test. By following the top graph from left to right, it is evident that initially the output signal is at high (supply) voltage. This indicates that the entire thyristor is off, waiting for an ignition. Then, an over-threshold spike is provided with the NMOS gate (bottom graph) and, as a consequence, the output voltage goes down to reach its standing value. Here the situation stabilizes and the circuit locks into a standing condition. Successively, a reset pulse not shown in the figure forces the circuit into the initial turned off condition. This pulse is provided through an additional MOS transistor that shorts the N-MOS's gate to ground. After having proved that the circuit effectively ignites depending on the input spike, we have

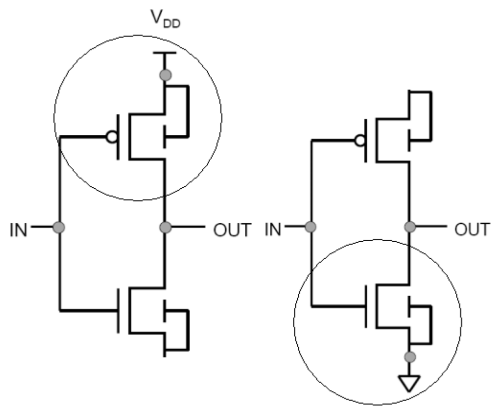

Figure 2: Transistors extracted from commercial inverters

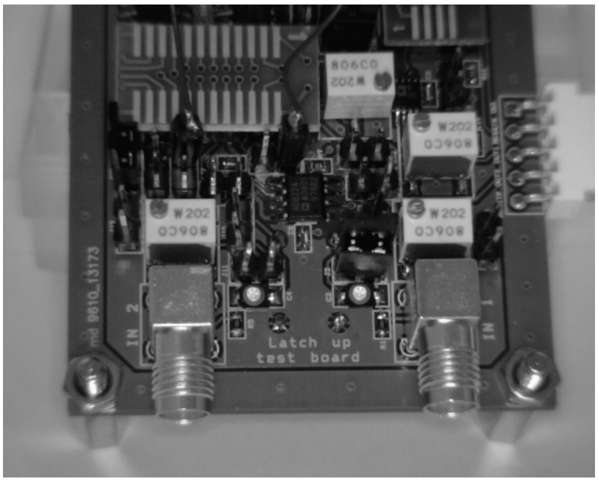

Figure 3: The board

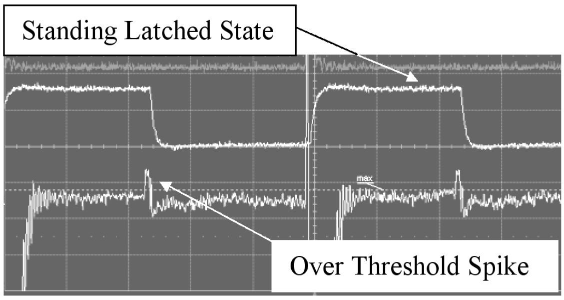

Figure 4: Oscilloscope plot at T=5µs

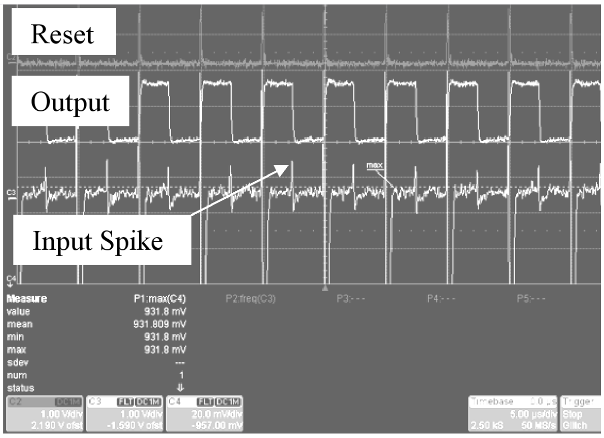

Figure 5: Cyclic latchup ignitions at T=5µs

measured the spike height, which is of the order of 10 mV and, and the input impedance of the circuit, which is of the order of 100 Ω. As the pulse width is about 100 ns, the injected charge in the transistor's gate is of the order of 10 pC (10mV / 100Ω × 100ns = 10pC). This is a rough estimation fully compatible with what was obtained in [6, 7].

Eventually, we measured the noise figure of the circuit in terms of spread in the ignition voltage. Hence, we have swept accurately the spike height, while measuring the ignition-to-non-ignition ratio over 200 cycles at a time. These measurements have been repeated several times to estimate the reliability and repeatability of the system. Moreover, the tests have been carried out by increasing and by decreasing this spike's height to measure the behavior of the circuit during rising and falling transition points. Figure 5 shows a

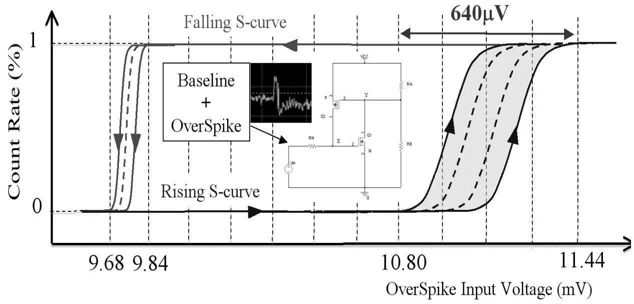

Figure 6: Noise curve

test configuration using a cyclic ignition of the system. Figure 6 summarizes all these measurements. It can be easily seen that the rising and falling curves of the noise transition – S-curves – are different in transition width, point and spread. However, the most significant part of the curve has been shaded to point out that the spread in the ignition point is about 640µV - i.e. spread of ignition threshold @ 50% of S-curve, let us say lower that 1mV, in any case -. So, both rising and falling transition spreads are very sharp since any transition curve owns a noise that can be estimated in of the order of 100µV. All in all, the whole power consumption of the cell is also very low, of the order of 1µW, when it is not ignited. This can be easily understood since the number of components inserted, basically two transistors plus one reset switch plus some resistors, is much smaller than that of the modern pixel circuits. Hence, it is reasonable to expect even better numbers and results for integrated versions of the latchup circuit.

The authors [see G. Villani et al., 8, 9] are investigating other types of latchup detector studies oriented to low-power applications and dosimetry. In fact, if just one or both transistors of the latchup cell are replaced with floating gate devices, not only the over spike input would be under control, but also the baseline over which this spike is added. Thus, being the charge injected within the floating gate removable via external radiation, the same latchup circuit could be applied as a dosimeter. In more detail, once a floating gate MOS has been programmed with a certain threshold, this threshold is swept back down depending on the total absorbed radiation dose, till the latchup process ignites spontaneously. Hence, if the threshold to absorbed dose ratio is known, it can be claimed that the cell ignites whenever a certain dose of radiation is absorbed: this is a dosimeter. This type of research is ongoing but the principle has already been proved [8, 9].

III. A SECOND PROTOTYPE

Figure 7 shows a circuit implementing a SCR topology using one P-channel MOS transistor and one N-channel MESFET component by CREE. Additionally the SCR is built via SiC instead of silicon. The reason of this choice relies in the high-temperature and high-radiation tolerance of the SiC. This could open new applications in these fields. Hence, we have here used the CREE 24010 MESFET component instead of the N-MOS. At first we have used a standard JFET Spice model to describe a linear behavior of the MESFET trying to simulate the whole circuit shown in Figure 7. The topology corresponds to the circuit shown in Fig. 1. The ignition is

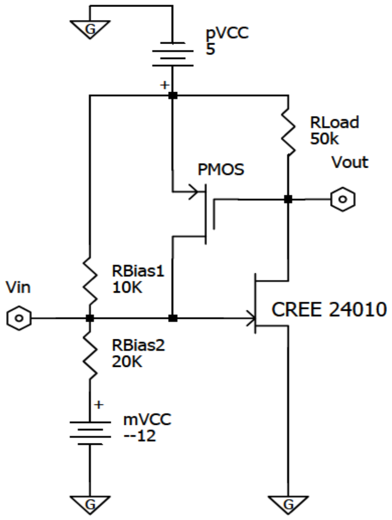

Figure 7: Actual circuit mounted on a test-board using the MESFET 24010

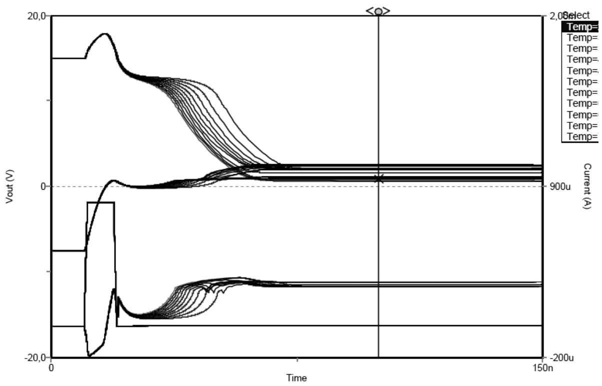

Figure 8: Simulation of a Temp. Montecarlo of the Latchup ignition of the above circuit

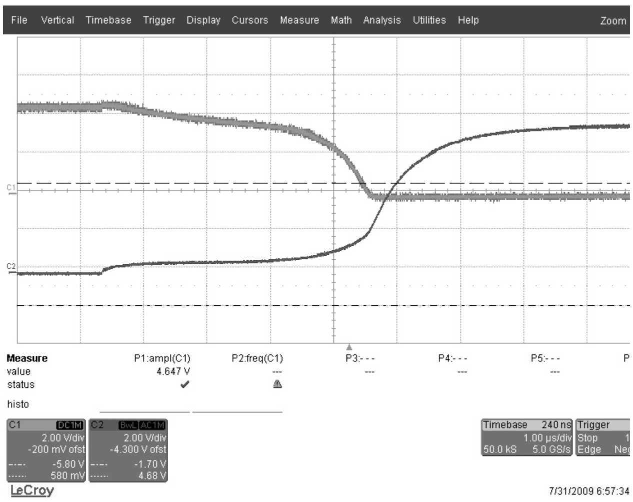

Figure 9: Oscilloscope plot

confirmed as it was investigated in the past provided a different and dedicated polarization. Figure 8 shows a Montecarlo Spice simulation of the circuit shown in Fig. 7. A sweep in temperature has been done. From top to bottom, first set of plots represent the output voltage on the MESFET's drain, a second set of plots describe the current on the MESFET and a single pulse simulates a given deposited charge at the MESFET's gate.

Figure 9 shows two oscilloscope plots of the same circuit tested on a board. The top graph represents the Vout in the circuit while the bottom plots is the MESFET's gate, or Vin pin. Even though the input spike is not visible, it is clear that the two curves cross each other as a confirmation of the circuit ignition. The voltage swing is of the order of 2 volts and the ignition time of the order of several □s. The sensitivity of the circuit will be a future business. For the time being the results confirm that also a MESFET component can be used into a latchup topology.

IV. Conclusion

This study indicates that a very simple circuit can operate like the more complicated structures used today in modern pixel detectors. An integrated device designed via modern CMOS technologies may work either as particle detector or as readout circuit for general sensors. The cell tested in laboratory was designed by exploiting commercial transistors connected to form a thyristor circuit. The circuit has a noise spread of the threshold lower that 1mV, power consumption due to leakage-biasing currents of the order of 1µW, estimated charge sensitivity of the order of 1pC and very good repeatability.

Future applications in high-energy physics and in radiation monitoring seem to be the most suitable for this type of device. In addition, for its high simplicity and, consequently, for its very low power consumption, it is also easily adaptable to a wide range of monitors, from portable devices to huge pixel detectors.

V. References

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